SANDIA REPORT

SAND99-0923

Unlimited Release

Printed May 1999

Wafer Fusion for Integration of Semiconductor Materials and Devices

RECEIVED

JUL 06 1999

OSTI

Kent D. Choquette, K. M. Geib, H. Q. Hou, A. A. Allerman, S. Kravitz,
D. M. Follstaedt, and J. J. Hindi

Prepared by

Sandia National Laboratories

Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia is a multiprogram laboratory operated by Sandia
Corporation, a Lockheed Martin Company, for the United States
Department of Energy under Contract DE-AC04-94AL85000.

Approved for public release; further dissemination unlimited.

Sandia National Laboratories

Issued by Sandia National Laboratories, operated for the United States Department of Energy
by Sandia Corporation.

NOTICE: This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government, nor any agency thereof, nor any of their employees, nor any of their contractors, subcontractors, or their employees, make any warranty, express or implied, or assume any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represent that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government, any agency thereof, or any of their contractors or subcontractors. The views and opinions expressed herein do not necessarily state or reflect those of the United States Government, any agency thereof, or any of their contractors.

Printed in the United States of America. This report has been reproduced directly from the best available copy.

Available to DOE and DOE contractors from
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Prices available from (703) 605-6000
Web site: <http://www.ntis.gov/ordering.htm>

Available to the public from
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Rd
Springfield, VA 22161

NTIS price codes
Printed copy: A03
Microfiche copy: A01

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

SAND99-0923
Unlimited Release
Printed May 1999

**Wafer Fusion for Integration of
Semiconductor Materials and Devices**

Kent D. Choquette, K. M. Geib, H. Q. Hou, A. A. Allerman,
S. Kravitz, D. M. Follstaedt, and J. J. Hindi

Photonics Research Department
Center for Compound Semiconductor Science and Technology
Sandia National Laboratories
P.O. Box 5800
Albuquerque, NM 87185-0603

Abstract:

We have developed a wafer fusion technology to achieve integration of semiconductor materials and heterostructures with widely disparate lattice parameters, electronic properties, and/or optical properties for novel devices not now possible on any one substrate. Using our simple fusion process which uses low temperature (400-600 °C) anneals in inert N₂ gas, we have extended the scope of this technology to examine hybrid integration of dissimilar device technologies. As a specific example, we demonstrate wafer bonding vertical cavity surface emitting lasers (VCSELs) to transparent AlGaAs and GaP substrates to fabricate bottom-emitting short wavelength VCSELs. As a baseline fabrication technology applicable to many semiconductor systems, wafer fusion will revolutionize the way we think about possible semiconductor devices, and enable novel device configurations not possible by epitaxial growth.

Acknowledgements:

The authors are indebted to a multitude of researchers formerly and presently at Sandia as well as elsewhere, including: J. Barton, O. Blum, M. H. Crawford, S. Farrens, B. E. Hammons, and B. Roberts.

This work was supported by the United States Department of Energy under Contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation for the United States Department of Energy.

WAFER FUSION FOR INTEGRATION OF SEMICONDUCTOR MATERIALS AND DEVICES

Table of Contents

1. INTRODUCTION.....	1
2. WAFER FUSION PROCEDURE.....	2
2.1. SURFACE PREPARATION.....	3
2.2. MECHANICAL TESTING.....	5
2.3. ANNEALING PRESSURE	5
2.4. ANNEALING TEMPERATURE.....	7
2.5. ANNEALING GAS	8
3. III-V/III-V SEMICONDUCTOR FUSION.....	10
3.1. GAAS/GAAS BONDING.....	11
3.2. GAAS/GAP BONDING	11
3.3. GAAS/INP BONDING.....	12
4. III-V/SI SEMICONDUCTOR FUSION.....	13
4.1. GAAS/SI BONDING.....	13
4.2. INP/SI BONDING	13
5. BOTTOM EMITTING VCSELS BY WAFER FUSION	14
5.1. WAFER BONDED VCSEL FABRICATION.....	15
5.2. VCSEL/ALGAAS BONDING.....	17
5.3. VCSEL/GAP BONDING.....	18
6. SUMMARY.....	19
APPENDIX A: Reprint of "Short wavelength bottom-emitting vertical cavity lasers fabricated using wafer bonding"	21
APPENDIX B: Reprint of "Short wavelength bottom-emitting VCSELS"	23

WAFER FUSION FOR INTEGRATION OF SEMICONDUCTOR MATERIALS AND DEVICES

Table of Figures

Figure 1. Sketch of wafer fusion procedure..	3
Figure 2. TEM cross section image of bonded GaAs/Si	4
Figure 3. Ultrasonic image of wafer bonded GaAs/Si showing defects at the bonded interface.....	6
Figure 4. Ultrasonic image of wafer bonded GaAs/Si showing a nearly defect-free interface.....	6
Figure 5. High resolution TEM image of GaAs/InP using N_2	9
Figure 6. High resolution TEM image of GaAs/InP using H_2	10
Figure 7. I-V characteristics of wafer fused homojunctions: (a) n-type GaAs/GaAs and (b) p-type GaAs/GaAs.....	11
Figure 8. I-V characteristics of wafer fused heterojunctions: (a) n-type GaAs/GaP and (b) p-type GaAs/P.....	12
Figure 9. Sketch of bottom emitting selectively oxidized VCSELs.....	14
Figure 10. Fabrication steps for wafer bonded bottom-emitting VCSELs.....	15
Figure 11. TEM images of wafer bonded VCSEL to AlGaAs.....	16
Figure 12. Characteristics of VCSELs bonded to AlGaAs substrate.	17
Figure 13. Threshold current versus size for VCSELs bonded to AlGaAs.....	18
Figure 14. Characteristics of VCSELs bonded to GaP substrate.....	19

1. Introduction

One of the principal roadblocks to development of many compound semiconductor device technologies has been the requirement for lattice matching between the various layers in the heterostructures. As a result, it is often very difficult if not impossible to integrate complementary technologies or materials. Sandia has historically played a leading role in alternative approaches for greater materials flexibility in device design, pioneering strained layer heteroepitaxy in the early 1980's and more recently strain-relief buffer layers. However these approaches are still subject to many limitations, particularly in the limit of large lattice mismatch ($>2\%$ or so) and thick layers. The difficulty is principally a product of the tendency for defects such as misfit dislocations to propagate through the heterostructure as it is grown, leading to reduced transport and optical efficiency.

Recently a new approach to this problem has been introduced, and has met with remarkable success in initial reports. The technique, wafer fusion, involves the atomic-scale fusion via covalent bonds of the two different materials with a combination of pressure and high temperatures. When successful, the resulting fused structure exhibits a nearly perfect array of misfit dislocations at the interface, with a frequency corresponding to the lattice mismatch between the materials. However, since the defects are not "grown-in" as in conventional strained-layer heteroepitaxy, they are confined at the interface and thus should have limited impact on device performance.

This assertion has been borne out in recent device demonstrations: AlGaInAs 980 nm lasers fused onto Si substrates and $1.3\text{ }\mu\text{m}$ vertical cavity lasers fabricated by fusing AlGaAs based mirrors onto AlInP active regions. For the latter, advantages to more conventional strategies employing dual dielectric mirror stacks include greater thermal conductivity and simplified electrical injection afforded by a semiconductor mirror with a large refractive index differential. Thus wafer fusion allows bringing together materials with desirable optical/electrical properties that would otherwise not be possible with conventional epitaxy. This new technology has the potential to redefine conventional design rules for compound semiconductor devices, enabling integration of a broad range of materials and device technologies based on substrates with highly disparate lattice parameters.

As a baseline device fabrication expertise applicable to virtually every group III-V, II-VI and IV semiconductor system, wafer fusion will revolutionize the way we think about semiconductor devices and systems design, enabling combinations of materials, heterostructures and devices previously thought impossible. For example, AlGaInP heterostructures on GaAs substrates have been used for VCSELs in the wavelength range 650-700 nm. Shorter wavelength operation of resonant-cavity devices such as visible VCSELs and

resonant-cavity light emitting diodes is made difficult by the unavailability of an acceptable materials option for the mirrors. A transparent substrate would significantly improve the light collection efficiency possible in the devices. Our approach here is to employ wafer fusion to integrate devices with short-wavelength active regions grown on a GaAs substrate, then wafer bonded to a transparent substrate for emission through this substrate.

Our approach in this research was to initially focus on the underlying materials issues associated with wafer fusion, with the ultimate objective of applying this novel technique to a wide range of different devices using novel materials and heterostructure systems. The wafer fusion process was investigated in detail, with primary emphasis on the dependence of fusion quality on epi/substrate surface preparation and the annealing parameters, including annealing temperature, pressure, and gas composition. Several strategic materials systems are investigated to demonstrate the feasibility of wafer fusion for integration of advanced compound semiconductor devices technologies. These include: GaAs/GaAs, GaAs/AlGaAs, GaAs/GaP, GaAs/InP, InP/Si, and GaAs/Si. We considered the integration of vertical cavity surface emitting lasers (VCSELs) as the primary technology driver in this research. Thus based on our wafer fusion studies, short-wavelength bottom emitting VCSELs wafer bonded to AlGaAs and GaP substrates were successfully demonstrated.

2. Wafer Fusion Procedure

We designed, constructed, and calibrated a 3 zone 4 inch diameter fusion system which has stringent temperature stability and a gas handling manifold for various gases including N₂ and forming gas. In addition, we designed sample holders which allow the application of pressure during the heat treatment process. The wafer fusion process was studied as a function of annealing temperature, applied pressure, and gas composition. Materials characterization techniques used included: scanning electron and transmission electron microscopies for characterization of the fused interface morphology and defect structure; wafer dicing and polishing to determine adhesion strength; and standard I-V techniques for characterization of diode behavior of the fused heterostructure. The feasibility and reproducibility of wafer fusion for manufacturing was also evaluated.

The sample holder was constructed of graphite, and consisted of two plates which are clamped together using four screws. To ensure the pressure is uniformly applied, a half sphere of graphite is placed between the plates. During annealing, the wafer bonded samples are held in contact with a pressure of approximately 60 to 120 N. The wafer bonded samples which varied in size (from 1x1 cm² up to a quarter of a 2 inch diameter wafer) were then placed into

Figure 1. Sketch of wafer fusion procedure: 1) trenches etched into one wafer, both wafers cleaned; 2) wafers clamped; 3) wafers annealed under N gas flow.

the pressure fixture, pushed into a room temperature furnace held at room temperature, and annealed at a higher temperature. After the annealing process, the furnace is turned off and allowed to come to 100 °C or the sample is pulled slowly from the furnace at temperature.

The primary result of this work is the development of a robust and reproducible wafer fusion process which differs from previously reported techniques. A schematic of the wafer bonding process is shown in Fig. 1. The wafer fusion is accomplished at 400-600°C in an atmosphere of dry N₂ for 2 hours with the wafers held in compression ($\approx$ 60 to 100 N) during the annealing. Contrary to earlier wafer bonding procedures our process does not use H₂ gas and is done at lower temperature. Further details are described below.

2.1. Surface Preparation

The surface preparation of the samples to be bonded was found to be critical for successful wafer fusion. Typically, the samples are cleaned in acetone and methanol, followed by rinsing 20 seconds in 1:20 NH₄OH:H₂O and blown dry. Upon contact the samples sometime have good adherence but not routinely.

We have also determined that patterning one of the wafers with trenches enhances wafer bonding. This arises due to the ability of gases to escape from the interfaces through the channels during annealing, as well as and from the reduced surface area that is subjected to strain.

Figure 2. TEM cross section image of bonded GaAs/Si showing an inclusion and dislocations into the substrates. The large gap at the interface is indicative of poor bonding; note this image corresponds to sample shown in Fig. 3.

A principle consideration for successful bonded is “PROTECT YOUR SURFACES AT ALL TIMES”. This begins from the moment you open the package until after you bring the pieces together. Contamination, particles, and surface damage will quickly turn a routine days work of bonding into a week worth of headaches, with the added expense of losing material due to its no longer being useful for bonding. When cleaving wafers always use a new clean wipe for every cut, place the wafers face down and cleave from the back. When handling, always use gloves and never touch the surface with tweezers. The dirtiest thing in the lab is yourself, therefore sometimes little things such as holding your breath while bonding can make a world of difference. Never leave a surface face up for very long before bonding, rather, always have a wafer carrier available that has the concave inside and place the wafer face down there. This protects the surface from being damaged due to it only touching the edges and keeps particles from falling on the surface. If possible always have a nitrogen gun available.

An important constraint on contact bonding is that the surface must be clean and particle free. A goniometer was used to measure contact angles of water on surfaces for surface tension measurements. The most noticeable results were for the very low contact angle for the hydrogen plasma exposed silicon wafers as opposed to the large contact angle of the HF etched silicon. Although this peculiar hydrophilic surface may be due to contamination, subsurface hydrogen

may be responsible for this hydrophilic nature of supposedly hydrogen terminated surfaces. Another interesting observation was obtained from a GaAs wafer that was measured after coming out of an MBE chamber with a freshly grown 1 μ m epilayer of GaAs. This surface was relatively hydrophilic similar to that obtained by an HCl cleaned GaAs surface. Surface angle measurements were noted to decrease with time after drop deposition due to evaporation. A black box with a light source was used to detect particles on the surfaces. Initially it was found that the cleaning of the surfaces, using DI water to rinse, would produce surfaces cluttered with particles. It was suspected that this could be coming from the DI water; however the use of a spinner and high water flow rates seemed to alleviate the problem.

2.2. *Mechanical Testing*

The bond strength was initially probed using adhesion and cleaving experiments. However the "tape" pulls and cleaving do not adequately test whether you have achieved a fused interface. Instead, we have found that the preparation steps for TEM samples are a better gauge of the interface strength. Specifically, the ability to saw a sample using the wafer saw, without the samples delaminating, was a quick test used to determine successful bonding.

Numerous bonded interfaces were also examined using cross section TEM; an example of GaAs/Si is shown in Fig. 2. In addition, we have used IR imaging and ultrasonic imaging to examine the bonded interface. In most cases the IR image agrees with the ultrasonic image; however, the latter appears to be the more sensitive technique. The ultrasonic imaging technique, done in collaboration with J. Gieske has shown to be a very sensitive probe to defects, such as voids, particulates, trapped gas, etc. which occur at the bonded interface. An example is shown in Figs. 3 and 4. The ultrasonic technique shows discontinuities at the interface as measured by differences in ultrasonic reflectance. Notice that many defects are detected in Fig. 3, while Fig. 4 shows a relatively defect-free interface. We have also observed differences in the bonded interfaces for surfaces pretreated with hydrogen versus oxygen plasmas.

2.3. *Annealing Pressure*

Initially wafer bonding without the use of external pressure was examined. For successful bonding the as-contacted wafers must adhere to each other very well. To examine this bond an IR source-camera setup is used. Past experience dictates that for successful contact bonds, the wafers must be very well polished, clean, and flat. Therefore, a routine roughness study was undertaken using profilometry and atomic force microscopy (AFM). The profilometry used 400

Figure 3. Ultrasonic image of wafer bonded GaAs/Si. A H_2 plasma pretreatment is followed by a 200°C anneal in N_2 , which is insufficient to eliminate defects at the bonded interface.

Figure 4. Ultrasonic image of wafer bonded GaAs/Si. A H_2 plasma pretreatment is followed by a 300°C anneal in N_2 , which produces a nearly defect-free interface.

μm scans with the roughness measured every $80\ \mu\text{m}$. This is an empirical standard and correlates with the suggestions in the operating manuals. For well polished silicon the roughness average was 2-3 nm. This material produced consistently good contact bonds. The mechanical grade GaAs wafers produced roughness values of 3-4 nm and after bonding these wafers less than acceptable results were obtained. This was evident by non contact or sparsely contacted areas over large sample sizes (e.g. quarter of 2 inch diameter wafer).

Epi-ready GaAs was found to have superior surface finish and produced excellent contact bonds. For all the profilometry after the instrument was adjusted, such as was regularly done during this time, the values obtained would change for a given wafer. Therefore rather than using absolute values for evaluation, comparison values were used on a day to day basis. To study roughness further, an AFM was applied to the task. Although no meaningful roughness results were obtained, the power spectrum analysis of the surface roughness did identify extreme amounts of noise located at 60, 120, and 240 Hz locations, strongly suggested it was due to mechanical "line" noise and its harmonics. This problem was isolated and corrected. Very little AFM work has been done since this correction, primarily due to the roughness constraints for pressure bonded wafers (as discussed below) were less strict.

Once the graphite pressure fixtures arrived dramatic improvements in the successful bonding yield was realized. The roughness constraints and even to some extent the particle contamination controls were relaxed. Material that was only partially or even not at all contact bonded could be annealed with the result of up to 100% of the area bonded as viewed by IR inspection. However, although the surfaces appeared to be adhered to one another the robustness of these bonds can be very strong or very weak depending on the material system used. Many surface preparations and anneal schedules have been used for various materials. Generally the surface cleaning is dictated by the material used and the anneal temperatures are inversely proportional to the difference of thermal expansion of the wafers.

Pressure was varied by adjusting the torque applied to each of the four screws in the sample holder. The applied torque was varied from a starting point of 20 oz-in to below 14 oz-in for substrates with a minimum area of 5x5mm. This range corresponds to a pressure of 200 to 50 N; the typical applied pressure was ≈ 180 N. (Some variation is seen between the nominally identical pressure fixtures.) The lower limit of fixture torque that allowed wafer bonded was not obvious but it is suspected that it can be lowered substantially. In general, the application of pressure during annealing greatly improves the bonding yield, particularly over simple contact bonding!

2.4. Annealing Temperature

A matrix was devised with one axis being temperature and the other pressure. The pressure was measured in torque values for the screws. The criteria for successful bonding was if the material could be sawn into 100um wide pieces. The annealing temperatures were reduced to 400 °C and the pressure used was 100 N or lower.

Lower temperatures below 400 °C resulted in bond failures. Samples bonded at 350 °C did not have sufficient strength to survive sawing. There are several other variables that can be tried, two of which are time and surface treatment.

Surface treatment variations was minimally pursued, it was found that wafers that were soaked in an ammonium sulfide solution provided a much stronger initial contact strength and stronger adhesion after the lower temperature anneals. For example, VCSEL material which does not provide adhered-as-contacted material due to roughness and/or stress, can be contact bonded with a sulfur treatment. This may be valuable when it comes to alignment and handling of the contacted material. Also the sulfur treated material did provide enough strength after low temperature anneal, 300 °C, for successful wafer sawing. However, during TEM preparation the bond fell apart and a mysterious "brimstone" was seen on the surface under magnification. Some etched under-cutting of the mirror stacks were seen due to the sulfur treatment but it was very minimal.

From our experiments, we found that high temperatures are not desirable primarily due to thermal expansion strain. In addition, wafer fusion at high temperature (≥ 700 °C) may likely be accompanied by undesirable dopant diffusion. The strain comes about due to the difference of thermal expansion coefficients, for example between Si and III-V semiconductors. Since the wafers are bonded at temperatures above 400 °C, once they are cooled to room temperature, the interfaces are subject to strain. The biggest coefficient mismatch arises between GaAs and Si, with a smaller difference apparent between Si and InP. This is consistent with the resulting bonding of GaAs/Si versus InP/Si: the former combination tends to delaminate over time (a few days) while the latter appears to be more robust.

However, it can also be argued that high temperatures are required for traditional wafer bonding where the wafers are brought together under ambient conditions and then annealed at higher temperatures. In this work we have been able to obtain only marginal success in overlapping these contradictory constraints, and only for the InP to GaAs system. For III-V semiconductor bonding, we found annealing temperature varying from 400-600 °C were satisfactory.

Room temperature bonding appears to be very difficult. Recent demonstrations of Si/Si bonding at room temperature have used a vacuum technique. The idea is straightforward, two wafers under UHV conditions are either, heated or subjected to ion sputter cleaning to remove the surface contamination and oxide and then the two wafers are brought together. In this manner, differences in the thermal expansion coefficients can be overcome, although no device demonstrations have been reported.

2.5. *Annealing Gas*

Conventionally, III-V wafer fusion is accomplished using a hydrogen ambient. The belief is that H can getter surface oxides, promoting intimate atomic contact at the fused interface. However, due to safety concerns, we

Figure 5. High resolution TEM image of GaAs/InP using N_2 during annealing.

wished to consider the use of an inert gas atmosphere during fusion annealing. Two samples were prepared, one annealed in nitrogen and the other in hydrogen. The nitrogen sample was annealed in the tube furnace and the hydrogen specimen was annealed in a rotating disk MOVPE reactor. Figs. 5 and 6 show the fused interface between GaAs/InP using nitrogen and hydrogen, respectively, as the ambient atmosphere during annealing. Comparison of the high resolution TEM images in Figs. 5 and 6 show no discernible difference in the interface morphology. Note that intimate atomic bonding is achieved with a disordered interface region approximately 3-5 monolayers thick but without evidence of an oxide layer. The bonded interfaces observed using N_2 gas are identical to those observed using H_2 during annealing. Thus we conclude that hydrogen is not necessary for the reduction of oxide in the interface, contrary to the literature. The majority of the wafer fusion experiments (and all of the device demonstrations) were accomplished using a dry nitrogen carrier gas during annealing.

Figure 6. High resolution TEM image of GaAs/InP using H_2 during annealing.

3. III-V/III-V Semiconductor Fusion

Wafer bonding is one technique to achieve hybrid integration of photonic and other device technologies. Thus the fusion of III-V semiconductors with dissimilar lattice constants will be required. In this work we considered the following systems: GaAs/GaAs, GaAs/AlGaAs, GaAs/GaP, and GaAs/InP. The structural and electrical properties were examined. To optimize the electrical properties of the fused interfaces, we examined the current-voltage (I-V) characteristics of wafer bonded samples. Samples doped n- and p-type were fused together and appropriate ohmic contacts were deposited. The samples were cut into 100 μm square mesas for electrical characterization.

Figure 7. I-V characteristics of wafer fused homojunctions for different annealing temperatures: (a) n-type GaAs/GaAs and (b) p-type GaAs/GaAs.

3.1. GaAs/GaAs Bonding

Homojunction bonding of GaAs proved very easy; fusion of GaAs/AlGaAs was also deemed straightforward. In spite of good mechanical properties as described in Section 2.1, the electrical properties were found to vary with annealing temperature. Fig. 7 illustrates the I-V characteristics from homojunctions formed between n- and p-type GaAs using various annealing temperature. Notice in Fig. 7(a) that annealing temperatures $\geq 600^\circ\text{C}$ are required to achieve ohmic behavior for n-doped interfaces, while in Fig. 7(b) annealing as low as 400°C is sufficient for p-doped interfaces. The non-ohmic behavior observed for 500°C annealing in Fig. 7(a) is indicative of a space-charge region at the interface, presumably arising from the interface disorder (see Figs. 5, 6, and 11).

3.2. GaAs/GaP Bonding

Wafer fusion between GaAs and GaP proved more difficult. It was found that careful surface cleaning and preparation was necessary for successful bonding. Moreover, the electrical properties of the fused interface were again found to be dependent upon bonding temperature. Fig. 8 illustrates the I-V characteristics from wafer fused heterojunctions between n- and p-type GaAs/GaP. For n-type heterointerfaces displayed in Fig. 8(a), non-ohmic

Figure 8. I-V characteristics of wafer fused heterojunctions for different annealing temperatures: (a) n-type GaAs/GaP and (b) p-type GaAs/P.

behavior is found at all annealing temperatures from 400-700 °C. However for the p-doped heterointerfaces in Fig. 8(b), we find that 600 °C anneals provide ohmic conduction. The band offsets between GaAs/GaP are nearly equal for the conduction and valence bands. Thus there is a strong dipole charge induced by the disordered interface for n-type interfaces. The space charge effects could be compensated by higher doping at the n-type GaAs/GaP interface, either during VCSEL growth or by shallow implantation after growth but prior to wafer bonding.

3.3. GaAs/InP Bonding

Strong wafer fused interfaces between InP and GaAs was achieved. Fig. 5 shows the interface which results when bonding in a nitrogen ambient. Notice that a disordered region of approximately 3-5 monolayers exists, but no defects are observed perpendicular to the fused interface. Note that GaAs bonded to InP represents the “prototype” wafer bonding system. Our results compare favorably with prior reports in this system.

4. III- V/Si Semiconductor Fusion

The integration of III-V semiconductor devices with Si is a powerful fabrication technology platform, enabling novel microsystem development. Thus we examined the fused interfaces of GaAs/Si and InP/Si.

4.1. GaAs/Si Bonding

Wafer fusion experiments of GaAs/Si were done in cooperation with researchers at the University of California-Davis. This work was done employing hydrogen and oxygen plasma pretreatments, where the fusion occurred in an inert atmosphere and without applied pressure. The purpose of these experiments was to determine if hydrogen atmospheres are necessary during the fusion, as it commonly done elsewhere. We have determined that clean surfaces in combination with plasma pretreatments are sufficient to achieve bonding of GaAs to Si, since both O_2 and H_2 bonding of GaAs/Si was achieved. In the cases where oxygen plasma pretreatments are used, a thin oxide layer was detected at the interface; using hydrogen plasma pretreatments enables oxide-free bonding interfaces, with few defects observed. However, the bond strength was typically not adequate using contact bonding, while higher temperature annealing provided marginal success.

Eventually we were able to achieve acceptable contact wafer bonding, followed by annealing for GaAs/Si. An example of a GaAs/Si bonded interface is shown in Fig. 2. GaAs/Si can not be annealed to as high as temperatures as the InP/Si due to the large difference in thermal expansion coefficients. The maximum temperature that was successfully used was 450 °C. GaAs/Si bonded samples were subjected to shear strength testing. The bonded interfaces held together with a pressure in excess of 1.6 MPa applied.

4.2. InP/Si Bonding

InP bonded to Si exhibited higher yield than GaAs/Si. For InP/Si, the maximum appropriate annealing temperature is approximately 500 °C. Above this temperature the wafers either delaminate or crack upon cooling. Lower temperatures (200-300 °C) did not achieve bonding. The samples that survive the anneal resulted in a highly stressed curved structure, with the silicon curved towards the InP (silicon in compression and InP in tension) and both pieces exhibited plastic deformation to some extent.

5. Bottom Emitting VCSELs by Wafer Fusion

For a device demonstration to show the potential of wafer fusion for hybrid integration, we pursued wafer fusion of GaAs/AlGaAs vertical cavity surface emitting lasers (VCSELs) to new host substrates. Bottom-emitting VCSELs which emit through a transparent substrate have several advantages over top-emitting VCSELs for some applications. These advantages include accessibility of the laser output at both facets, the ability to fashion optical elements such as collimating or focussing lenses into the substrate, and the suitability of this structure for flip-chip integration to microelectronic circuitry. Relatively long wavelength (e.g. 980 nm) VCSELs are required to emit through a GaAs substrate. Bottom-emitting VCSELs grown on GaAs substrates for emission at shorter wavelengths appropriate for Si photodetectors (e.g. 850 nm) rely upon etching deep via holes or removal of the substrate, both of which can lead to damage and compromise the underlying distributed Bragg reflector mirror. Bottom-emitting 850 nm VCSELs grown directly on transparent AlGaAs substrates require a thick GaAs buffer layers which reduces the output transmitted through the substrate.

The fabrication and performance of selectively oxidized 850 nm vertical cavity surface emitting laser (VCSEL) diodes which emit through transparent AlGaAs and GaP substrates was pursued. The short wavelength bottom-emitting VCSELs were fabricated by wafer fusion using an inert gas low temperature annealing process. The electrical characteristics of n- and p-type GaAs/GaAs and GaAs/GaP wafer bonded interfaces have been examined to optimize the annealing temperature. A significant reduction of the current-voltage characteristics of the VCSELs bonded to GaP substrates has been achieved whereby the bottom-emitting VCSELs show similar threshold voltage as compared to top-emitting lasers.

Figure 9. Cross section sketch of bottom emitting selectively oxidized VCSELs. The lasers are wafer fused to a transparent substrate such as GaP or AlGaAs.

Figure 10. Fabrication steps for wafer bonded bottom-emitting VCSELs bonded to GaP.

5.1. Wafer Bonded VCSEL Fabrication.

Our fabrication approach for bottom emitting short wavelength VCSELs is to optimize the VCSEL grown on a GaAs substrate, and then to wafer bond the VCSEL to a new host substrate, not necessarily pseudomorphic to GaAs. In Fig. 9 we show a sketch of the bottom-emitting VCSELs. Notice the fused interface is located outside of the cavity, in contrast to long wavelength wafer bonded VCSELs. The optimized wafer fusion process which is employed has enabled a significant reduction of the current-voltage properties, whereby the bottom-emitting VCSELs show similar threshold voltage as compared to top-emitting lasers. Moreover, wafer bonding VCSELs to GaP substrates allows the possibility of bottom-emitting visible VCSELs.

The fabrication procedure is depicted in Fig. 10. First, an 850 nm top-emitting VCSEL wafer with an n- or p-type top mirror is grown on a GaAs substrate. Next square mesas are formed by anisotropically etching deep trenches in the VCSEL wafer. The VCSEL samples are then flipped over and wafer bonded to GaP or $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$ substrates as described below. After bonding, the GaAs substrate is thinned by mechanical polishing and dry etching until the trenches are exposed thus defining the VCSEL mesas. The VCSELs are oxidized at 440°C in steam to produce quarter-wave thick buried oxide apertures next to

the active region for current and optical confinement. Finally, the anode and cathode electrical contacts are deposited.

The central fabrication process required for our short wavelength bottom-emitting VCSELs is the wafer fusion. The first step in wafer bonding is to thoroughly solvent clean both wafers. Next the wafers are subjected to an O_2 plasma, followed by rinsing in ammonium hydroxide. The samples are then put into contact and placed in a pressure fixture. The annealing for wafer fusion is accomplished at temperatures between 400-600 °C in dry N_2 for 2 hours with the wafers held in compression. Ideally, we wish to keep the annealing temperature relatively low, in order to avoid composition intermixing and dopant diffusion in the VCSEL. The VCSEL/AlGaAs interface is shown in Fig. 11. The fused interface exhibits disorder in the plane of the interface but is devoid of any apparent oxide layer or evidence of extended structural defects extending out of the plane of the fused interface. The structurally disordered interface can influence the electrical properties, as discussed in Section 3.

Figure 11. TEM images of wafer bonded VCSEL to AlGaAs. The inset shows a closeup of the bonded interface.

Figure 12. Characteristics of top- and bottom-emitting VCSELs bonded to AlGaAs substrate.

5.2. VCSEL/AlGaAs Bonding

Since we found early in our research that bonding GaAs/AlGaAs was fairly straightforward, we first tried bonding VCSELs to AlGaAs substrates. The disadvantage of this system is that the VCSEL wavelength cannot be shorter than approximately 830 nm, due to the limited composition of available AlGaAs substrates.

The device characteristics of top-emitting 850 nm VCSELs and bottom emitting wafer bonded lasers to AlGaAs using the same VCSEL wafer are compared in Figs. 12 and 13. Note that the calculated reflectivity of the output mirror of the top-emitting VCSEL (99.67%) is higher than the bottom-emitting VCSEL (98.8%) due to the contribution from the top semiconductor/air interface. Thus in Figs. 12 and 13 the threshold current is higher for the bottom-emitting VCSELs, which can be corrected using an appropriate mirror design. The ripple apparent in the light output arises from reflection feedback from the substrate and can be eliminated using anti-reflection coatings on the substrate. Compared to the top-emitting VCSELs, the output power is reduced by approximately 25% in the bottom-emitting lasers due to residual free carrier absorption in $\text{Al}_{0.08}\text{Ga}_{0.92}\text{As}$ substrate.

Figure 13. Threshold current versus oxide aperture size for top- and bottom-emitting VCSELs bonded to AlGaAs.

Fig. 13 shows a comparison of the size dependence of the threshold current. In spite of the greater scatter in the threshold current due to substrate reflection for the bottom emitting VCSELs in Fig. 13, a similar trend with aperture size is observed. The voltages plotted in Fig. 12 for VCSELs are nearly identical, indicating that the bonded n-GaAs/n-AlGaAs interface has not adversely effected electrical transport (see also Fig. 7(a)).

5.3. VCSEL/GaP Bonding

Bonding VCSELs to GaP substrates is attractive since GaP is transparent to even visible wavelengths. Because of the non-ohmic I-V characteristics exhibited by n-type GaAs/GaP (see Fig. 8(a)), we focussed our efforts on bonding “p-up” VCSELs to p-type GaP. However the space charge effects which produce large parasitic voltage drops could be compensated by higher doping at the n-type GaAs/GaP interface, either during VCSEL growth or by shallow implantation after growth but prior to wafer bonding.

The device characteristics of a 5x5 μm oxide apertured bottom-emitting VCSEL that is wafer bonded to a GaP substrate is plotted in Fig. 14. The threshold current is again higher for the bottom-emitting VCSEL in Fig. 14 due

Figure 14. Light, voltage vs. current characteristics of an as grown top-emitting VCSEL and bottom-emitting VCSEL bonded to GaP.

to greater mirror loss. However, the bottom-emitting VCSEL achieves higher maximum output power, indicating minimal loss in the GaP substrate. The threshold voltage is similar for the two devices, indicating that the bonded interface has not adversely effected electrical transport, as expected from Fig. 8(b). However, the differential resistance is higher for the bottom-emitting VCSEL, due to a missing ohmic p-contact to the GaP. Nevertheless, the threshold voltage is reduced dramatically compared to our first VCSELs bonded to n-type GaP which exhibited threshold voltages of ≥ 9 V.

6. Summary

We have developed a robust and reproducible wafer fusion process which differs from previously reported techniques. The wafer fusion is accomplished at 400-600°C in an atmosphere of dry N₂ for 2 hours with the wafers held in compression during the annealing. Contrary to earlier wafer bonding procedures our process does not use H₂ gas and is done at lower temperature. We have successfully demonstrated wafer bonding of GaAs/GaAs, GaAs/AlGaAs, GaAs/GaP, GaAs/InP, InP/Si, and GaAs/Si.

We have also employed this fabrication technique to produce 850 nm bottom-emitting VCSELs by wafer bonding to AlGaAs and GaP transparent substrates. The optimum annealing temperature was determined by examining the I-V characteristics of bonded heterointerfaces. The top- and bottom-emitting VCSELs showed comparable laser characteristics. A dramatic reduction of the threshold voltage was achieved by avoiding excessive space-charge effects at the

GaP bonded interface. Bottom emitting short wavelength VCSELs may be important to future VCSEL applications, such as the use of large 2-dimensional VCSEL arrays for free space interconnects. The demonstration of wafer bonding VCSELs to GaP substrates will enable bottom-emitting visible VCSELs for other emerging applications.

**APPENDIX A: Reprint of “Short wavelength bottom-emitting vertical
cavity lasers fabricated using wafer bonding”**

♦ K. D. Choquette, K. M. Geib, B. Roberds, H. Q. Hou, and B. E. Hammons,
Electron. Lett. **34**, 1404 (1998).
♦

Short wavelength bottom-emitting vertical cavity lasers fabricated using wafer bonding

K.D. Choquette, K.M. Geib, B. Roberds, H.Q. Hou, R.D. Twisten and B.E. Hammons

Selectively oxidised 850nm vertical cavity surface emitting laser diodes which emit through transparent *n*-type GaP and AlGaAs substrates are reported. The short wavelength bottom-emitting lasers are fabricated using a low temperature inert gas wafer fusion process. Compared to top-emitting lasers, the bottom-emitting lasers bonded to *n*-type AlGaAs substrates show comparable electrical characteristics, while lasers bonded to *n*-type GaP substrates exhibit higher series resistance and voltage.

Bottom-emitting vertical cavity surface emitting lasers (VCSELs) which emit through a transparent substrate have several advantages over conventional top-emitting lasers, such as accessibility of the laser output at both facets, the ability to fashion optical elements such as collimating lenses into the substrate, and the suitability of this structure to flip-chip bonding for hybrid microelectronic integration. Relatively long wavelength (e.g. 980nm) VCSELs are required to emit through a GaAs substrate. Bottom-emitting VCSELs grown on GaAs substrates for emission at shorter wavelengths appropriate for Si photodetectors (e.g. 850 nm) rely on etching deep via holes [1] or the removal of the substrate [2], both of which can lead to damage and may compromise the underlying distributed Bragg reflector mirror. Bottom-emitting 850nm VCSELs grown directly on transparent AlGaAs substrates require a thick GaAs buffer layer which reduces the output transmitted through the substrate [3]. We report high performance 850 nm selectively oxidised VCSELs bonded to GaP and AlGaAs transparent substrates using wafer fusion to enable emission through the substrate.

Fig. 1 Sketch of bottom-emitting selectively oxidised 850nm VCSEL array wafer bonded to AlGaAs or GaP transparent substrate

Fig. 2 Transmission electron micrograph of bottom-emitting VCSEL wafer bonded to AlGaAs substrate which shows fused interface

In Fig. 1, we show a cross-sectional view of the bottom-emitting VCSELs. First, an 850nm top-emitting VCSEL wafer with an *n*-type top mirror is grown on a *p*-type GaAs substrate. Next, square mesas are formed by anisotropically etching deep trenches in the VCSEL wafer. The VCSEL samples are then flipped over and wafer bonded to *n*-type GaP or Al_{0.1}Ga_{0.9}As substrates using the

process described in the following. After bonding, the GaAs substrate is thinned by mechanical polishing and dry etching until the trenches are exposed, thus defining the VCSEL mesas. The VCSELs are oxidised at 440°C in steam to produce quarter-wave thick buried oxide apertures next to the active region for current and optical confinement [4]. Finally, the anode and cathode electrical contacts are formed by simultaneously depositing a film of Ti/Au on the mesa tops and the transparent substrate followed by rapid thermal annealing.

The wafer bonding between the 850nm VCSEL wafer (with a 10nm thick cap of GaAs) and the GaP or Al_{0.1}Ga_{0.9}As substrate is accomplished at 440°C in dry N₂ for 4h with the wafers held in compression. The transmission electron microscope image in Fig. 2 shows a disordered interface region devoid of any apparent oxide layer between the VCSEL and the AlGaAs substrate, with no evidence of defects extending out of the plane of the fused interface. The bonded interface in Fig. 2 is similar to those obtained between GaAs/InP using H₂ gas and higher annealing temperatures [5].

interface has not adversely affected electrical transport. Compared to the top-emitting VCSELs, the output power is reduced by approximately 25% in the bottom-emitting lasers, due to residual free carrier absorption in the MGaAs substrate.

Fig. 3a and b show the characteristics of broad area bottom-emitting VCSELs bonded to *n*-AlGaAs and *n*-GaP. The ripple apparent in the light output arises from reflection feedback from the substrate and can be eliminated using anti-reflection coatings on the substrate. Although similar light output is observed in Fig. 4a and Fig. 4b, the electrical characteristics differ significantly. The *n*-GaAs/*n*-GaP wafer bonded interface within the VCSEL in Fig. 4b produces an increase in the applied voltage and different resistance at threshold. These effects are likely to be due to the lower electron mobility in GaP, the non-ohmic GaP contact, and possibly to an excessive space charge region at the fused interface. Further characterisation of *n*- and *p*-type GaP bonded to GaAs is underway.

In summary, short wavelength bottom-emitting VCSELs have been demonstrated using wafer bonded AlGaAs and GaP transparent substrates. The bottom-emitting VCSELs that are wafer bonded to *n*-type AlGaAs exhibit a performance comparable to top-emitting devices. Bottom-emitting VCSELs that are wafer bonded to *n*-type GaP require a higher applied voltage, but enable fabrication of bottom-emitting visible VCSELs.

Acknowledgment: Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation for the United States Department of Energy under Contract DE-AC04-94AL85000.

© IEE 1998

28 May 1998

Electronics Letters Online No: 19981002

K.D. Choquette, K.M. Geib, B. Roberds, H.Q. Hou, R.D. Twisten and B.E. Hammons (Center for Compound Semiconductor Technology, Sandia National Laboratories, Albuquerque, NM 87185, USA)

E-mail: kdchoqu@sandia.gov

References

- 1 KOYAMA, F., KINOSHITA, S., and IGA, K.: 'Room-temperature continuous wave lasing characteristics of a GaAs vertical cavity surface-emitting laser', *Appl. Phys. Lett.*, 1989, **55**, pp. 221-222
- 2 FATHOLLAHNEJAD, H., MATHINE, D.L., DROOPAD, R., MARACAS, G.N., and DARYANANI, S.: 'Vertical-cavity surface-emitting lasers integrated onto silicon substrates by PdGe contacts', *Electron. Lett.*, 1994, **30**, pp. 1235-1236
- 3 KOHAMA, Y., OHISO, Y., and KUROKAWA, T.: '0.85µm bottom-emitting vertical-cavity surface-emitting laser diode arrays grown on AlGaAs substrates', *Electron. Lett.*, 1994, **30**, pp. 1406-1407
- 4 CHOQUETTE, K.D., SCHNEIDER, R.P., JR., LEAR, K.L., and GEIB, K.M.: 'Low threshold voltage vertical-cavity lasers fabricated by selective oxidation', *Electron. Lett.*, 1994, **30**, pp. 2043-2044
- 5 LO, Y.H., BHAT, R., HWANG, D.M., KOZA, M.A., and LEE, T.P.: 'Bonding by atomic rearrangement of InP/InGaAsP 1.5µm wavelength lasers on GaAs substrates', *Appl. Phys. Lett.*, 1991, **58**, pp. 1961-1963
- 6 CHOQUETTE, K.D., CHOW, W.W., HADLEY, G.R., HOU, H.Q., and GEIB, K.M.: 'Scalability of small-aperture selectively oxidized vertical-cavity lasers', *Appl. Phys. Lett.*, 1997, **70**, pp. 823-825

APPENDIX B: Reprint of "Short wavelength bottom-emitting VCSELs"

K. D. Choquette, J. S. Barton, K. M. Geib, A. A. Allerman, and J. J. Hindi, *Proc. SPIE* **3627**, 99 (1999).

Short wavelength bottom-emitting VCSELs

Kent D. Choquette, Jonathon S. Barton, Kent M. Geib, Andy A. Allerman, and Jana Jo Hindi

Center for Compound Semiconductor Science and Technology
Sandia National Laboratories, Albuquerque, NM 87185-0603

ABSTRACT

The fabrication and performance of selectively oxidized 850 nm vertical cavity surface emitting laser (VCSEL) diodes which emit through transparent GaP substrates is reported. Emission through the substrate is advantageous for many VCSEL configurations, such as for the incorporation of optical elements in the substrate or flip-chip integration to microelectronic circuitry. The short wavelength bottom-emitting VCSELs are fabricated by wafer fusion using an inert gas low temperature annealing process. The electrical characteristics of n- and p-type GaAs/GaAs and GaAs/GaP wafer bonded interfaces have been examined to optimize the annealing temperature. A significant reduction of the current-voltage characteristics of the VCSELs bonded to GaP substrates has been achieved whereby the bottom-emitting VCSELs show similar threshold voltage as compared to top-emitting lasers.

Keywords: vertical cavity surface emitting lasers (VCSELs), wafer bonding, wafer fusion, bottom-emitting.

1. INTRODUCTION

Bottom-emitting vertical cavity surface emitting lasers (VCSELs) which emit through a transparent substrate have several advantages over top-emitting VCSELs for some applications. These advantages include accessibility of the laser output at both facets, the ability to fashion optical elements such as collimating or focussing lenses into the substrate, and the suitability of this structure for flip-chip integration to microelectronic circuitry. For VCSELs grown on GaAs substrates, a relatively long wavelength (≥ 880 nm) is required to emit through the substrate. Bottom-emitting VCSELs grown on GaAs substrates for emission at 850 nm rely upon etching via holes through the substrate [1] or removal of the substrate [2], both of which can compromise the performance of the VCSEL. We have previously described bottom-emitting 850 nm VCSELs wafer fused to AlGaAs substrates [3]. Bottom-emitting 850 nm VCSELs grown directly on transparent AlGaAs substrates typically require a GaAs buffer layers which reduces the output transmitted through the substrate [4]. Furthermore, moving to shorter wavelengths is not practical due to the limited composition range of the available AlGaAs substrates.

Herein we discuss the fabrication and performance of selectively oxidized 850 nm VCSELs which emit through transparent GaP substrates. Our fabrication approach is to optimize the VCSEL grown on a GaAs substrate, and then to wafer bond the VCSEL to a new host substrate, not necessarily pseudomorphic to GaAs [3]. In Fig. 1 we show a sketch of the bottom-emitting VCSELs. Notice the fused interface is located outside of the cavity, in contrast to long wavelength wafer bonded VCSELs [5]. The optimized wafer fusion process which is employed has enabled a significant reduction of the current-voltage properties, whereby the bottom-emitting VCSELs show similar threshold voltage as compared to top-emitting lasers. Moreover, wafer bonding VCSELs to GaP substrates allows the possibility of bottom-emitting visible VCSELs.

Figure 1. Cross section sketch of bottom emitting selectively oxidized VCSELs: The lasers are wafer fused to a transparent substrate such as GaP or AlGaAs.

2. WAFER FUSION

The central fabrication process required for our short wavelength bottom-emitting VCSELs is the wafer fusion [6]. Our first step in wafer bonding is to thoroughly solvent clean both wafers. Next the wafers are subjected to an O_2 plasma, followed by rinsing in ammonium hydroxide. The samples are then put into contact and placed in a pressure fixture. The annealing for wafer fusion is accomplished at temperatures between 400-600 °C in dry N_2 for 2 hours with the wafers held in compression. Ideally, we wish to keep the annealing temperature relatively low, in order to avoid composition intermixing and dopant diffusion in the VCSEL. The resulting wafer fused interface exhibits disorder in the plane of the interface but is devoid of any apparent oxide layer or evidence of extended structural defects extending out of the plane of the fused interface [3,6]. The structurally disordered interface can influence the electrical properties, which we discuss next.

To optimize the electrical properties of the fused interfaces, we examined the current-voltage (I-V) characteristics of wafer bonded samples. GaAs and GaP substrates (doped $1 \times 10^{18} \text{ cm}^{-3}$) were fused together and appropriate ohmic contacts were

Figure 2. I-V characteristics of wafer fused homojunctions for different annealing temperatures: (a) n-type GaAs/GaAs and (b) p-type GaAs/GaAs.

Figure 3. I-V characteristics of wafer fused heterojunctions for different annealing temperatures: (a) n-type GaAs/GaP and (b) p-type GaAs/P.

deposited. The samples were cut into 100 μm square mesas for electrical characterization. In Fig. 2 we show the I-V characteristics from homojunctions formed between n- and p-type GaAs. Notice in Fig. 2(a) that annealing temperatures $\geq 600^\circ\text{C}$ are required to achieve ohmic behavior for n-doped interfaces, while in Fig. 2(b) annealing as low as 400°C is sufficient for p-doped interfaces. The non-ohmic behavior observed for 500°C annealing in Fig. 2(a) is indicative of a space-charge region at the interface, presumably arising from the interface disorder.

Fig. 3 shows the I-V characteristics from wafer fused heterojunctions between n- and p-type GaAs/GaP. For n-type heterointerfaces displayed in Fig. 3(a), non-ohmic behavior is found at all annealing temperatures from 400 – 700°C . However for the p-doped heterointerfaces in Fig. 3(b), we find that 600°C anneals provides ohmic conduction. The band offsets between GaAs/GaP are nearly equal for the conduction and valence bands. Thus there is a strong dipole charge induced by the disordered interface for n-type interfaces. Because of the non-ohmic I-V characteristics exhibited by n-type GaAs/GaP, we focussed our efforts on bonding “p-up” VCSELs to p-type GaP. However the space charge effects could be compensated by higher doping at the n-type GaAs/GaP interface, either during VCSEL growth or by shallow implantation after growth but prior to wafer bonding.

3. VCSEL FABRICATION

The VCSEL fabrication sequence is schematically depicted in Fig. 4 [3]. First, an 850 nm top-emitting (“p-up”) VCSEL wafer is grown on an n-type GaAs substrate. The VCSEL sample is then wafer bonded to a p-type GaP substrate using a 600°C anneal. Next the GaAs substrate is thinned to $< 10\ \mu\text{m}$ thickness by mechanical polishing and reactive ion etching (RIE). Note it is not necessary to completely remove the substrate. Square mesas are patterned and dry etched into the VCSEL epitaxy to expose the oxidation layers. The VCSELs are oxidized at 440°C in steam to produce quarter-wave thick buried oxide apertures next to the active region for current and optical confinement [7]. Finally, Ge/Au/Ni/Au is deposited for the n-contact on the VCSEL, followed by rapid thermal annealing. An ohmic contact, such as Ti/Pt/Au, was not deposited onto the GaP substrate for the VCSELs characterized below.

Figure 4. Fabrication steps for wafer bonded bottom-emitting VCSELs.

Figure 5. Light, voltage vs. current characteristics of an as grown top-emitting VCSEL and bottom-emitting VCSEL bonded to GaP.

4. VCSEL CHARACTERISTICS

The device characteristics of a $5 \times 5 \mu\text{m}$ oxide apertured bottom-emitting VCSEL that is wafer bonded to a GaP substrate is plotted in Fig. 5. We show a comparison of a top-emitting and bottom-emitting lasers fabricated from the same VCSEL wafer. Note that the calculated reflectivity of the output mirror of the top-emitting VCSEL (99.67%) is higher than the bottom-emitting VCSEL (98.8%) due to the contribution from the top semiconductor/air interface for the former. Thus the threshold current is higher for the bottom-emitting VCSEL in Fig. 5 due to greater mirror loss, which can be corrected using an appropriate mirror design. Note also the bottom-emitting VCSEL achieves high maximum output power, indicating minimal loss in the GaP substrate. The threshold voltage is similar for the two devices, indicating that the bonded interface has not adversely effected electrical transport, as expected from Fig. 3(b). However, the differential resistance is higher for the bottom-emitting VCSEL, due to the missing ohmic p-contact to the GaP. Nevertheless, the threshold voltage is reduced dramatically compared to our previous VCSELs bonded to n-type GaP which exhibited threshold voltages of $\geq 9 \text{ V}$ [3].

5. CONCLUSION

We have fabricated 850 nm bottom-emitting VCSELs by wafer bonding to GaP transparent substrates. The optimum annealing temperature was determined by examining the I-V characteristics of bonded heterointerfaces. The top- and bottom-emitting VCSELs showed comparable laser characteristics. A dramatic reduction of the threshold voltage was achieved by avoiding excessive space-charge effects at the GaP bonded interface. The demonstration of wafer bonding VCSELs to GaP substrates will enable bottom-emitting visible VCSELs for emerging applications. This work was supported by the United States Department of Energy under Contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation for the United States Department of Energy.

REFERENCES

- [1] F. Koyama, S. Kinoshita, and K. Iga, *Appl. Phys. Lett.* **55**, 221 (1989).
- [2] H. Fathollahnejad, D. L. Mathine, R. Droopad, G. Maracas, and S. Daryanani, *Electron. Lett.* **30**, 1235 (1994).
- [3] K. D. Choquette, K. M. Geib, B. Roberds, H. Q. Hou, and B. E. Hammons, *Electron. Lett.* **34**, 1404 (1998).
- [4] Y. Kohama, Y. Ohiso, and T. Kurokawa, *Electron. Lett.* **30**, 1406 (1994).
- [5] J. J. Dudley, D. I. Babic, R. Mirin, L. Yang, B. I. Miller, R. J. Ram, T. Reynolds, E. L. Hu, and J. E. Bowers, *Appl. Phys. Lett.* **64**, 1463 (1994).
- [6] Y. H. Lo, R. Bhat, D. M. Hwang, M. A. Koza, and T. P. Lee, *Appl. Phys. Lett.* **58**, 1961 (1991).
- [7] K. D. Choquette, K. L. Lear, R. P., Schneider, Jr., K. M. Geib, J. J. Figiel, and R. Hull, *Photon. Tech. Lett.* **7**, 1237 (1995).

15	MS0603	Kent Choquette (1712)
1	MS9018	Central Technical Files (8940-2)
2	MS0899	Technical Library (4916)
1	MS0619	Review & Approval Desk (00111)
1	MS0188	LDRD Office (4001)