**DEWPOINT
Final Report**

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Microelectronics Packaging Program
Lawrence Livermore National Laboratory**

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Microelectronics Packaging Program
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Overview of the DEWPOINT Program Relating to Microchannel Heatsink Cooling

The DEWPOINT (Directed Energy POver INTEgration) program was aimed at providing the large amounts of electric power required for a laser or accelerator based in space, or on an aircraft or satellite platform. This is our final report on our efforts as a part of this program which was cancelled before completion. This report summarizes the entire scope of effort funded by this program. It also includes some related information on cryogenically cooled microchannel heatsinks which was funded internally by LLNL.

Specifically, the DEWPOINT program was to provide the electrical power for the proposed Neutral Particle Beam weapon system of the Strategic Defense Initiative. The Neutral Particle Beam called for a space-based accelerator driven by radio frequency power sources. The radio frequency solid-state power amplifiers generate waste heat which must be dissipated [1].

Our part of the DEWPOINT program was focused on providing a microchannel heatsink cooling system for the RF power amplifier chips. This effort at the Lawrence Livermore National Laboratory Microelectronics Center as a part of the DEWPOINT project was directed from Los Alamos National Laboratory by Don Reid and Andrew Young. We also had extensive interactions with Robert Regan and others at GTE Systems Technology Laboratory, Waltham, MA, where the hybrid amplifier module (HAM) containing the solid state triode chips were combined with RF circuit components. The bonding of the HAM aluminum nitride substrate to the silicon microchannel heatsink became a major effort in the latter part of the program. We also had interactions with Edward Piechowiak and Robin Hamilton of Westinghouse Electric Corporation Defense and Electronics Center, Baltimore, MD, where the HAM units and the cooling system were integrated into an RF power supply. The information exchange with Chris Piaseczyk and co-workers at Grumman Aerospace who were providing the overall space or air platform systems design was also very useful. The DEWPOINT program had a large number of other contractors as well with whom we had interesting but lesser amounts of contact.

On the spacecraft, liquid hydrogen is present as fuel for the reactive flight control engines. As a part of an overall flow control system, the pressurized hydrogen is also available for cooling. Proposed hydrogen flow system designs required the cryogenic fluid to be supercritical by the time it reached the RF amplifier section. The configuration of the MCHS is based on the assumption, that liquid hydrogen is available at 35 K and 35 atm.

One of the early design challenges was related to available volumetric flow rate of the hydrogen for the microchannel heatsink cooling system. In the proposal effort [2], based on numbers available in [1], it was assumed that large enough flows were available to have an optimal heatsink design based on predicted thermal resistances. In these early stages of the heatsink effort, the attention was centered on a cooling system design with 30:1 aspect ratio heat sink and a flow of 14.4 l/min per square centimeter of cooled area of supercritical hydrogen at 35 atm and 35 °K inlet temperature. This heatsink design had a predicted thermal resistance of $6.38 \times 10^{-6} \text{ m}^2 \cdot ^\circ\text{C/W}$, which for a heat load of 500 W/cm^2 would correspond to a surface temperature rise of 32 K and the LH2 temperature rise of 5.8 K.

At these large flow rates, heatsink performance was optimal, and because the surface temperature rise was small, several materials could have been qualified for the heatsink structure. Hydrogen diffusion studies on aluminum nitride and silicon were originally conducted on the basis that they were potential heatsink materials. Metals were also considered for applications in the heatsink fin structure.

Simpler models of the heatsink thermal performance were also acceptable. Because of a small temperature rise in the supercritical hydrogen, the hydrogen thermophysical properties were assumed to be constant down the microchannel length.

Several iterations were required before the corresponding number used by space platform systems designers for the supercritical hydrogen volumetric flow rate was obtained, but it was immediately clear that the space system designers were assuming a much smaller flow rate per HAM. The final resolution of the issue [3] was that each HAM was allocated $680.27 \times 10^{-6} \text{ kg/s}$ of supercritical hydrogen as the mass flow rate (0.742 l/min of volumetric flow). This flow rate number was based on the design of a 500 kW RF

power amplifier requiring 735 HAM 's which each dissipate 680 W. The heated area of these HAM's, based on a inline 16 chip chip layout design, was 0.09 m width by 0.16e-02 m of heated channel length. Correcting for this area ($1.44\text{e-}04 \text{ m}^2$ or 1.44 cm^2) to compare to the volumetric flow rate assumed in the proposal calculations, we find that this final flow rate was 3.6% of the flow assumed in the proposal. When the Grumman space platform systems designers were informed of the possible consequences of such limited flow, they were willing to grant flow increase to the heatsink cooling based on an overall efficiency study, but it was clear that greatly reduced flow rates should be the basis of the heatsink design.

Designing for greatly reduced flow rates had several very significant implications. First, heatsink thermal performance became very critical. Silicon became the only material choice for the heatsink fin structure. As is typical of single crystal materials there is a factor of 8 to 10 increase in the thermal conductivity of silicon as one cools the material from room temperature to about 75 °K. Polycrystalline aluminum nitride or copper were much less satisfactory as a fin structure material.

Also, the optimum aspect ratio for the heatsink, that is the ratio of the fin height to width, was such that preferential etching of silicon became the only way to manufacture heatsinks for use with the supercritical hydrogen as the coolant.

Finally, the thermal resistance due to the temperature increase of the supercritical hydrogen became a large factor in the overall thermal resistance, and the effect of this fluid temperature rise could not be ignored in the design calculations. A new design code was written to estimate the heatsink surface temperature rise as a function of the coolant flow rate and the applied heat flux. This code divided the channel length into many increments and calculated a surface temperature and coolant temperature with updated thermophysical properties at every increment of channel length.

Silicon heatsinks typical of prior design for water and cryogenic cooling had a pressure capacity of about 20 atm. We made an effort as a part of the DEWPOINT program to raise this level to 50 atm, so there would be a safety factor at the intended 35 atm operating pressure. Changes in the system requirements, and calculations which showed adequate thermal performance at lower pressures led

to a lowering of the pressure requirement, although significant understanding had been achieved as to how to raise the silicon heatsink pressure capacity.

As the design of the GTE HAM proceeded, they settled on a single layer aluminum nitride substrate design. The substrate design included vias to ground through the substrate to the heatsink and substrate bond layer. Part of the LLNL responsibility was to attach the HAM to the heatsink. We devised a foil bonding technique to accomplish this, though to have a production process with a better accept rate, more process development would be required.

The costs associated with using supercritical hydrogen as the coolant for the HAM development tests was viewed as prohibitive as these tests were planned. Estimates of heatsink performance so that acceptable maximum surface substrate temperatures could be maintained by cooling the heatsink with large amounts of liquid nitrogen. The final focus of the program was on the HAM development tests with liquid nitrogen cooling, and so work was done to show that the large heat loads produced by the RF power chips could be dissipated without choking the heatsink coolant flow.

In retrospect, it became clear that the logical way to attach the HAM modules to the heatsinks would be in four chip rather than 16 chip unit. The value added in the HAM module production and cost of the heatsink was large enough that losing 16 chips or one large heatsink because one chip was faulty would be an unacceptable loss. This change of design concept was never implemented in actual hardware, although trial heatsink designs were produced.

Design Calculations for Microchannel Heatsink with Cryogenic Cooling

The concept of the microchannel heat sink [4] derives from the observation that the coolant is responsible for most of the thermal resistance in a heatsink. The thermal conductivity of liquids is typically two to three orders-of-magnitude lower than that of metals or semiconductors which usually make up the heatsink structure. In a MCHS the thermal resistance of a forced convection heat transfer structure is minimized by maximizing the heat transfer coefficient at the structure-to-coolant interface and maximizing the surface area

over which the heat transfer occurs. This is done by fabricating a structure with a base where the heat flux is applied, and with many fins which project into the coolant flow. Figure 1 shows a schematic of a microchannel cross-section, while figure 2 show the details of the glass flow manifold.

Using a cryogen such as liquid nitrogen as the coolant in silicon microchannel heatsinks takes advantage the order-of-magnitude increase in the thermal conductivity of silicon at these lower temperatures. The thermal conductivity of silicon increases from 148 W/m²K at 300 °K to 1340 W/m²K at 80 °K. Figure 3 shows a plot of the thermal conductivity of silicon as a function of temperature [5].

The operation of electronic devices at cryogenic temperatures offers potential benefits for a wide range of applications. For example, microwave circuits using high-temperature superconductors [6], UHF power static induction transistors [7] and MOSFET n-channel devices [8].

The thermal resistance of a MCHS is the temperature difference between the heated surface and the coolant divided by the heat load per unit area. There are three major factors that contribute to the thermal resistance: that due to thermal conduction from the top of the fin to the heated surface, that due to the fact that the fluid increases in temperature as it absorbs heat (caloric heating), and that due to convection between the fin wall and the heat transfer fluid.

The thermal resistance due to conduction is minimized by having the shortest possible length from the heat source to the heatsink, and by using high thermal conductivity material to bond the active device to the heatsink structure. The thermal resistance due to caloric heating is minimized by using a coolant with larger thermal capacity and by using high flow rates. The thermal resistance due to convection is typically the largest of the three factors and depends on the thermal conductivity of the fin and coolant materials, and the heat transfer coefficient between the two. The design of the heatsinks for the DEWPOINT application differs from the typical circumstances in that the convective and caloric contributions to the overall thermal resistance are approximately equal. The heat transfer coefficient is expressed it in terms of the (dimensionless) Nusselt number

$$h = \frac{(Nu)k_c}{D}$$

where h is the heat transfer coefficient, D is the hydraulic diameter, and k_c is the thermal conductivity of the coolant.

The greater the surface area of the heatsink, the more heat may be transferred. However, for the microchannel heatsink walls, or fins, each additional increment of length becomes less effective. When one chooses a minimum area effectiveness for longer lengths, optimized designs which account for the coolant and wall material are possible. The optimum channel height to width, assuming that the fin and channel widths are equal, is to first order,

$$\frac{H}{w_c} = \left(\frac{k_w}{Nu * k_c} \right)^{\frac{1}{2}}$$

For a silicon structure with liquid nitrogen as the coolant, and for equal channel and fin widths, this optimum aspect ratio is found to be in the range of 55 to 70. These aspect ratios acted as the starting point for optimization studies in silicon heatsinks using supercritical hydrogen as the coolant. Supercritical hydrogen thermophysical properties were held constant at the inlet values for this optimization study. The thermophysical properties were taken from [9]. Figure 4 shows the predicted heatsink performance as a function of aspect ratio. While the 50:1 aspect ratio heatsink had the superior performance, it is noted that the 30:1 aspect ratio heatsink had nearly identical thermal performance, particularly in the low flow regime. These heatsink performance predictions have been experimentally verified for many flow conditions, including the use of cryogenic coolants [10,11].

Based on the update in systems requirements directing efforts to the low flow regime, calculations of predicted performance, and on an assessment of our manufacturing capabilities, the standard heatsink design for the DEWPOINT program was chosen.

The reference heatsink design had an aspect ratio of 30:1. The fin and channel height was 0.90 mm in a silicon substrate of 1.5 mm thickness. The fin and channel widths were 30 μ m each.

Silicon microchannel heatsink structures may be typically either sawn or etched. For large aspect ratios use of the preferential orientation etch method in silicon is preferred. The DEWPOINT hydrogen heatsinks were fabricated in single crystal silicon using a preferential etch method. To our knowledge, this was the first production use of this technique to construct silicon heatsinks.

Design Calculations for Microchannel Heatsink with Coolant Thermophysical Property Update

For more accurate predictions of the heatsink surface temperature, required for predictions of RF chip performance, and the exit temperature of the hydrogen, for system design considerations, a new design code was developed.

In this new design code, the heated channel length was divided into a integer number of segments. Starting with the coolant in its inlet flow condition, the coolant temperature rise, and surface temperature is calculated for each segment, with the coolant and surface temperatures acting as the input for the next segment length. The fluid velocity and pressure is also increment down the channel length. The thermophysical properties of the supercritical hydrogen coolant as a function of temperature and pressure were taken from [9] as before. Polynomial functions of the coolant thermophysical properties were derived and used to interpolated the coolant properties at intermediate points. Because no smoothing of the temperature gradient occurs, accounting for longitudinal and lateral thermal spreading due to solid conduction in the finned structure, the code is thought to be conservative.

The code input for the reference 30:1 aspect ratio DEWPOINT heatsink is found as the first item in appendix I. The temperature of the inlet supercritical hydrogen is given as 35 °K, with a flow rate of $0.1817\text{e-}04 \text{ m}^3/\text{s}$. The heat flux at this heatsink surface is given as $6.87\text{e+}06 \text{ W/m}^2$. The heatsink heated surface area is based on an assumed pad for 16 chips. This pad is 90 mm wide by 1.6 mm in the flow direction. The 16 chips are assumed to dissipate approximately 67 watts each, for 1 kW of dissipated heat. The channel length is conceptually divided into 30 segments for purposes of the calculations.

The corresponding code output for the above input in the next item in appendix I. Here it is seen that the volumetric flow rate as given above corresponds to a mass flow rate of $1.0\text{e-}03$ kg/s/W. This is 47% larger than the final minimum flow rate we were asked to assume, $0.68\text{e-}03$ kg/s/W. The conductive thermal resistance from various bonding and electrically isolating layers on the heatsink surface is seen to be 23% of the initial convective thermal resistance. The final thermal resistance, for the 30th segment on the second page of the output, is calculated to be $0.46\text{e-}05$ m²°K/W. The coolant exit temperature is 96°K, with a heatsink surface temperature of 127°K.

A FORTRAN listing of the heatsink calculation code is available through the author. A detailed description of the codes parameters is beyond the scope of this report, but the code structure and variable names should be easily interpreted.

A design code such as this should be calibrated against experiments using hydrogen as the cryogenic coolant in a heatsink. In advance of planned experiments which would have been part of the DEWPOINT program, a preliminary validation of the design code predictions was made using thermal finite element analysis. Figure 5 shows the temperature contours of the finite element analysis. Here the geometry is more complete with the chip modeled as the top part, with the gold bond layer and the aluminum nitride substrate seen as well. The finned heatsink structure on the bottom completes the geometric description.

With an chip size of 3.43 mm by 1.6 mm, and 67 W per chip as heat dissipated, the heat flux at the chip surface is $1.31\text{e+}07$ W/m², which corresponds to the total heat flux at the heatsink surface as given for the design calculations. Based on the heatsink calculations a heat transfer coefficient of 17850 W/m²°K is used with a coolant temperature of 90°K. The maximum chip temperature is given as 147°K, with an average maximum heatsink surface temperature of 129°K, within 2°K of the design code calculations.

There is a 13°K temperature change across the 0.5 mm thick aluminum nitride substrate at this heat flux.

Given the number of interpretive assumptions which must be made to link the design code calculations to the finite element analysis, such good agreement may be partly serendipitous, but definitely supports the contention that the design code has comparative finite element validation within its required accuracy of about 10%.

One of the most important predictions of the design code is seen in figure 6, where the heatsink surface temperature is plotted as a function of mass flow rate. The mass flow rate of interest, in the range of 0.001 to 0.0005 kg/s, is precisely the range where the heatsink surface temperature is most sensitive to flow rate. At 0.001 kg/s the heatsink surface temperature is 127 °K, still within an allowable range for the chip operating temperature. But at the mass flow rate of 0.00068, the system low flow design point, the heatsink surface temperature is 174 °K, a temperature too high to take best advantage of the chip's performance improvement at cryogenic temperatures. At still smaller flows the temperature continues to rise rapidly, to a heatsink surface temperature of 265 °K at a mass flow rate of 0.00046 kg/s. At large flow rates the heatsink surface temperature drops more gradually, with a heatsink surface temperature of 92 °K at a mass flow rate of 0.002 kg/s.

The effect of coolant pressure on the heatsink surface temperature is much less dramatic. Figure 7 shows this effect for the heatsink mass flow rate at 0.00068 kg/s. The unusual behavior of heatsink surface temperature rising and falling slightly over a narrow range of coolant pressures is explained by the values of the hydrogen heat capacity as a function of pressure and temperature in this range, as seen in figure 8.

Liquid Nitrogen Operation of the DEWPOINT Microchannel Heatsink and Critical Heat Flux

As the program progressed it became clear that it would be useful to be able to test the HAM RF power amplifier circuits at cryogenic temperatures but in liquid nitrogen or neon, rather than supercritical hydrogen. The facility and safety issues associated with using hydrogen as the coolant made it reasonable to do the many component and RF system tests with relatively inexpensive liquid

nitrogen as the coolant, and the few system verification tests using supercritical hydrogen.

Figure 9 shows the predicted heatsink surface temperature with liquid nitrogen cooling with a heat flux of $9.8425 \times 10^6 \text{ W/m}^2$. This heat dissipation rate is 40 greater than the design heating rate of $6.87 \times 10^6 \text{ W/m}^2$ to account for various possibilities such as less efficient chip power transformation in the component and network design process.

This demonstrates that liquid nitrogen cooling can maintain the heatsink surface temperature at 110 °K at the design heat flux by using comparatively larger flow rates of liquid nitrogen. The aspect of the RF power tests that cannot be duplicated by liquid nitrogen testing is the 35 °K turn on temperature for the chip circuits. This feature of chip operation could be studied using neon or helium as the heatsink coolants.

Recent work with liquid nitrogen cooled microchannel heatsinks has also demonstrated that these heat fluxes are well within measured critical heat fluxes. The critical heat fluxes are those heat dissipation rates at which the nitrogen begins to boil in the microchannels to the point where flow is blocked, and the temperature rises so quickly that the heatsink fails. By reducing the inlet liquid nitrogen temperature to 10 °K less than the saturation temperature, heat fluxes of greater than $20.0 \times 10^6 \text{ W/m}^2$ may be safely dissipated [12].

High Pressure Operation of Microchannel Heatsinks

Our previous experience with failure pressures in sawn heatsinks showed that for channel depths of 445 μm in 610 μm thick wafers the failure pressure was 21.5 atm (2.15 MPa). For sawn heatsinks with a channel depth of 865 μm in wafers of 1.5 mm the failure pressure was approximately the same, 21.7 atm. Etched heatsinks with the same channel depth and wafer thickness had a failure pressure of 32 atm. Different flow fixturing for the different tests leads to the possibility of different amounts of bending stresses in the heatsinks. However, the bending stresses are thought to be a second order effect, and the pressure results support the idea that

the failure is precipitated by crack growth events, and that attempts to produce heatsinks with higher pressure ratings should focus on increasing the energy required for crack propagation through the finned structure.

Two methods for elevating heatsink failure pressures have been pursued. In both methods the fracture energy is increased by misaligning the cleavage planes between the heatsink wafer and its reinforcing layer. The first uses a silicon direct bonding technique to bond a 1.0 mm wafer to a 0.5 mm wafer. The channels may then be sawn or etched into the 1.0 mm wafer. In the second method a gold-gold compression bond is used to bond a 0.5 mm thick reinforcing segment of silicon to the top of a heatsink. Tests of silicon direct bond heatsinks have shown improved failure pressures, 40 and 45 atm in sawn heatsinks. We are confident that improved pressure performance up to the 70 atm goal with etched heatsinks can be obtained by silicon layer reinforcement.

Liquid Nitrogen Flow and Test Facilities for Microchannel Heatsink Cooling

Originally we had planned to develop supercritical hydrogen flow facilities at LLNL's Site 300. This was part of the original cost estimate, and some effort was expended in the design of the facility. As the DEWPOINT program matured, this effort was a lesser priority. Other hydrogen test facilities were located, and our test effort were focused around using liquid nitrogen as the coolant.

Liquid nitrogen flow and test facilities were enhanced at LLNL as a part of the DEWPOINT program. The vacuum chamber for the heatsink tests was enlarged to allow for the presence of the HAM module and the related test circuitry. Figure 10 shows an end-on sketch of the vacuum chamber, with the heatsink mounting features in the middle, and the inlet, outlet, and diagnostic ports at the chamber boundary.

Figure 11 is a sketch of the liquid nitrogen inlet port, showing the thermocouple and pressure transducer couplings into the coolant flow. The liquid nitrogen delivery system was insulated and capable of delivering liquid nitrogen up to pressures of 200 psi (1.38 MPa),

Figure 12 is a sketch of the heatsink mounting fixture, to which the HAM module with heatsink would be clamped.

An computerized, automatic data-taking capability was also developed. The nitrogen coolant was expanded and heated in the heat exchanger, at the nitrogen was vented to the atmosphere. The required safety notes, safety procedures, and environmental impact statements were written and approved.

To lower the cost of the facility development, existing equipment was used as much as possible.

Hydrogen Diffusion and Aluminum Nitride Thermal Conductivity Experiments

At the beginning of the DEWPOINT program, aluminum nitride (AlN) was considered both as a heatsink and manifold material. The reason for this was largely based on GTE's choice of AlN as their HAM substrate. The diffusion of hydrogen through AlN was considered a potential problem for hydrogen leakage because AlN is a sintered material with a residual porosity. To be useful as a heatsink material, its thermal conductivity at cryogenic temperatures had to be known for design purposes. An experimental project was undertaken to resolve these issues.

The results of these experimental efforts were reported in [13].

At 97 °K, the thermal conductivity of aluminum nitride was measured at 66 W/m²°K with a standard deviation of 9 W/m²°K. With the greater lowered supercritical hydrogen flows, the higher thermal conductivity of single crystal silicon was required in the heatsink design, so aluminum nitride was abandoned as an alternative material for the finned structure.

Using helium gas, as a conservative estimate of the hydrogen diffusion behavior, the permeability coefficient for aluminum nitride was measured at room temperature. At 75 hours this coefficient was calculated to be 1.5e-21 m²/Pa*s. By comparing with permeation rates for other materials, it was concluded that aluminum nitride was a suitable material for the containment of hydrogen. Aluminum

nitride was planned to be used as the manifold material in the heatsink cooling system.

Heatsink and Manifold Design

The heatsink design parameters, such as the dimensions of the cooled area and the heatsink surface area, were decided upon by GTE after consultation with LLNL. Figure 13 shows the information received from GTE, which came originally via facsimile transmission 12 June 1992. As is evident in the figure, the heatsink design is based on cooling a 16 chip RF amplifier module. The chip spacing was according to GTE requirements for chip bond pads and other component attachments.

Figure 14 shows the layout of the heatsink as they were fabricated by preferential etching in a silicon wafer. Units in the sketch are in inches. This layout does not account for the orientation flat present in the wafer, used to define the $\langle 110 \rangle$ orientation in the wafer, for purposes of the photolithography mask alignment. The real presence of the flat in the wafers reduced the edge margin on one of the heatsinks, and this coupling with the fact that the silicon wafer edges were beveled, reduced the number of useful second heatsinks from each wafer processed. The beveling seemed to not only remove edge material but increase the defect density in the remaining material. The beveling was done on the wafers as part of a normal wafer polishing procedure.

Figure 15 is a reduced size copy of the drawing used to define the final heatsink part. In order to speed the heatsink production process, glass coolant manifolds were used for the heatsink to be used in the HAM module testing program. We have had considerable experience with the bonding of the Corning 7740 borosilicate glass to silicon. Figure 16 shows the configuration of the glass manifold. In order to reduce breakage in the heatsinks due to the forces used to clamp them to the flow fixture, a silicon backside reinforcing plate was used. Figure 17 details the plates dimensions. Figure 18 is the assembly drawing of the heatsink structure as it was produced, except that it shows a double layer aluminum nitride substrate to be supplied by GTE. We only used the double layer aluminum nitride substrate for preliminary bonding tests. All the actual HAM modules with chips were of the single layer substrate design which came later.

Figure 19 is a layout of a proposed photolithography mask design for a heatsink to cool GTE's 16 chip, 1.2 kW HAM module. There is only one 16 chip heatsink, but two other smaller heatsinks are present which were included as possibilities should a new 4 chip heatsink cooling system be desired. The splay alignment and depth measurement boxes are also seen in the mask layout. Figure 20 shows a proposed design for an aluminum nitride manifold to be part of the 1.2 kW heatsink design. It was also intended to have two HAM modules mounted top and bottom to it.

The integration of the heatsink and GTE HAM into the Westinghouse RF power system was an issue not fully clarified when the program ended.

Heatsink Manufacture

The technical basis for anisotropic or preferential etching in single crystal $\langle 110 \rangle$ silicon is described in [14, 15]. In order to produce the 30:1 aspect ratio heatsinks designed for use with supercritical hydrogen cooling, preferential etching was the only method known.

The basic process started with the procurement of a suitable 100 mm diameter single crystal silicon ingot. Ingots where the crystal axis is in the $\langle 110 \rangle$ orientation, a requirement of the preferential etching method, are special order items. Most silicon ingots for electronic chip production are in the $\langle 111 \rangle$ or $\langle 100 \rangle$ orientation. The ingots procured for the DEWPOINT program were bought from Freiburger Elektronikwerkstoffe of Germany. Since then I understand that a US silicon ingot producer has come back into the market for specialty ingots such as this. The ingot was then sliced into wafers and polished. The final polished thickness was specified at 1.5 mm (0.060 inch).

Photolithography was then used to pattern the wafers to determine the wafer crystal orientation. This splay pattern was etched into the wafer using KOH to determine the crystal orientation to within 0.1 of a degree. This is a much tighter requirement than is commonly encountered in silicon material processing in the electronic industry, where use of the orientation flat is considered adequate for most applications.

With the splay pattern etch as a reference, the pattern for the heatsink was exposed on the wafer using photoresist, the protective layer of silicon nitride was selectively removed, and the etch process was begun. The etch rate of the heated KOH was monitored using measurement boxes also etched into the wafer. The wafer was periodically inspected for defects and etch depth. 70 hours was a average etch time.

Appendix II describes in much greater detail the photolithography and etch processes.

After the etch process was completed, the protective layer of silicon nitride was removed everywhere, and the heatsink was sawn from the wafer.

The heatsink was bonded to the glass manifold, as well as the silicon reinforcing layer using a "reflow" bonding technique. The glass and silicon were placed in the appropriate bond position in a programmable furnace. The material was heated to 825 °C, just below the softening point of the Corning 7740 borosilicate glass. The temperature was held for 30 minutes, and then the assembly was cooled very slowly.

The resulting heatsink unit was measured against dimensional tolerances, and pressure tested for final acceptance.

Summary of Heatsinks Delivered

Table 1 is the heatsink inventory as of 24 November 1992, at the end of the heatsink production program.

Aluminum Nitride Substrate to Heatsink Bonding

The final manufacturing effort for LLNL in the DEWPOINT program was the bonding of the aluminum nitride HAM substrate to the heatsink cooled surface. A large transition in this effort occurred with GTE's decision to go with a single layer substrate. This reduced the weight and complexity of the HAM design, and used the heatsink to substrate bond as part of the electrical ground plane.

The RF power amplifier chips were bonded to the substrate at 400 °C. This bond used a gold/silicon eutectic bonding technique, with the bond temperature slightly above the eutectic temperature. Experiments were performed on a gold/gold self diffusion bond, but in order to reduce assembly thermal stresses, a lower temperature gold/tin eutectic bond was used. As a consequence, the chips were first bonded to the substrate, and then the substrate with chips was bonded to the heatsink, as the higher temperature processes had to occur first.

A foil bonding technique and apparatus was devised to bond the substrates with chips to the heatsink. The concept here was to use a thin film or foil of malleable metal as a pressure boundary. High pressure is introduced on one side of the foil, and it is pressed against the substrate with chips. The substrate is subsequently pressed against the heatsink, which is supported on the back side to react against the pressure. The foil conforms to the surface against which it is pressed, so that the pressure is uniformly distributed, and the higher chip areas do not see high stresses. In the actual chip bonds a polyimide film material was used to separate the copper foil from the top of the chips and chip pads. Figure 21 shows an exploded view of the foil bonder with the heatsink and substrate in position for a bond.

Various forms of a gold/tin eutectic bond were attempted. In the first, alternating layers of gold and tin were sputtered on the heatsink and substrate bond surfaces, then the surfaces were held together in the foil bonder, and the assembly was heated to a temperature that was above the 281 °C eutectic temperature, typically in the range of 300 to 320 °C.

The first difficulty noted was that the usual titanium or tungsten stick layers, used to promote adhesion between the silicon heatsink surface and the bonding layers, was not working as well as had been expected based on previous experience. It appeared that the tin was reacting with the titanium and that the gold was diffusing into the silicon. A less reactive, higher diffusion barrier stick layer was developed. It consisted of a titanium nitride stick layer. This stick layer shifted the failure from at the silicon surface to the bondline between the silicon and aluminum nitride bond layers. It should be noted that both stick layers worked well with the aluminum nitride substrate.

In order to reduce sputtering times and residual stresses in the bond layers, the sputtered gold tin layers of approximate eutectic composition was replaced with thin gold layers sputtered to each bond surface. A eutectic composition gold/tin foil was placed between the gold bond layers in the foil bonder and bond strength was measured.

While some bonds appeared to be adequate at this point, most of the bonds showed lack of flow in the gold bond layers. This led to a small percentage of the surface actually being in contact and bonded. By replacing the nitrogen process gas in the foil bonder with the more inert argon, this problem was resolved, and bonds with excellent strength were obtained.

Now a new problem emerged. In the bonding of actual substrates it was noted that now too much bond material flow occurred. The bond material was meant to flow into the substrate via holes to ground the topside substrate circuitry, but with the improved bond process, the material flowed too much, and the gold material was overflowing to the point that the excess material was shorting out the signal lines on the substrate top surface. In many of the via holes, contact with the KAPTON polyimide material blocked the gold/tin material flow once the flow material contacted this separation layer between the copper foil of the bonder and the chips. In order to take advantage of this phenomenon, a thin layer on polyimide was bonded to the substrate top surface, and the bond was attempted. This method resulted in the production of three high quality heatsink to HAM module bonds.

Appendix III gives greater detail on the exact process "recipe" used to produce the gold/tin eutectic heatsink to substrate bonds.

An investigation of the stresses in the microchannel heatsink with liquid nitrogen cooling [16] shows that they are well within the design operational limits. The fact that the residual stresses due to the manufacturing processes tend to cancel out the thermal stresses due to operational thermal gradients is particularly significant.

DEWPOINT Heatsink Effort Conclusions

The heatsink effort was a small but significant part of the overall DEWPOINT program. Many technical innovations and concepts were developed and tested as a part of this program effort to cool RF power amplifier chips to cryogenic temperatures.

As the mass flow rate of the supercritical hydrogen emerged as a critical heatsink design issue, the thermal performance of the heatsink at lower cryogenic coolant flows became the focus of the design.

The choice of materials was limited to single crystal materials, such as silicon, which have an order of magnitude rise in thermal conductivity at cryogenic temperatures.

In the prediction of heatsink performance, the temperature rise of the coolant cannot be ignored. A new computer code was written to predict performance of the heatsinks at cryogenic temperatures and account for the thermophysical property changes in the supercritical hydrogen coolant as a function of temperature and pressure.

We were able to show that liquid nitrogen cooling could be used for specification of the RF power amplifier matching circuit components. With liquid nitrogen cooling the RF power chips could be operated in the same 80 to 130°K temperature range, as would be the case for heatsinks with supercritical hydrogen cooling, and the circuit characteristics of the additional resistor, inductor, and signal line components could be incrementally changed for circuit compatibility. This cooling capability was possible because much larger liquid nitrogen mass flow rates in the experimental facility were possible, as compared to the corresponding design mass flow rate for supercritical hydrogen.

The liquid nitrogen microchannel heatsink flow facility was augmented for the testing of the RF power chips, and procurement was planned for use of the required RF test electronic equipment.

High pressure capability (35 atm) for the silicon microchannel heatsinks was shown to be a possibility, as was the use of aluminum nitride as the coolant manifold material.

27 single crystal silicon heatsinks were available for the DEWPOINT program use as the result of a successful manufacturing effort. This effort used preferential etching in KOH to produce high aspect ratio microchannel heatsinks for use with supercritical hydrogen or liquid nitrogen cooling. This was the largest production effort of etched heatsinks ever made, in the knowledge of the authors.

Special bonding fixtures were developed to bond heatsinks to the GTE hybrid amplifier modules, with chips already present on the aluminum nitride substrates of the modules. Sputtered thin films with a gold/tin eutectic foil were part of the bonding process. Three such units were delivered for RF chip and component testing.

The DEWPOINT program ended before the HAM/ heatsink assemblies could be tested in the liquid nitrogen heatsink flow system, although some tests were performed on these units with liquid nitrogen pool cooling at GTE. A number of technical difficulties hindered and raised the cost of concluding the program with a successful component test as was desired.

Much of what has been learned here, could be applied to new related technical efforts when the need arises. No insurmountable technical roadblocks were encountered which would have precluded the successful completion of the program, had additional resources been available. However, many technical details of the cooling system configuration remain unresolved.

Acknowledgements

The DEWPOINT team members included Robert Riddle, Lee Evans, and Tim Graff. Help from Anthony McCarthy, Wayne Bonde and Manuel Herrera is also gratefully acknowledged. Tony Bernhardt was the project originator and is the LLNL Microelectronics Center Program Manager, the program area where the project was completed.

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Appendices

Appendix I. Input and Output files for the Microchannel Heatsink Design Calculations, with Update of Supercritical Hydrogen Thermophysical Properties.

Appendix II. Heatsink Manufacturing Procedures.

Appendix III. Heatsink to Substrate Bond Procedures.

Heatsink Inventory

Dewpoint style (all etched)

<u>Mfg. date</u>	<u>ID#</u>	<u>Press. test (psi)</u>	<u>Wafer #</u>	<u>Comment</u>
9/92	DP-1	ok-holes too small	10	w/ weight
"	DP-2	*	10	w/o weight
"	DP-3	*	31 (11)	w/weight
"	DP-4	250	31 (11)	w/o weight
"	DP-5	ok	17	w/o weight
"	DP-6	250	17	w/o weight
"	DP-7	230	13	w/o weight
"	DP-8	250	13	w/o weight
"	DP-9	240	20	w/o weight
"	DP-10	*	20	w/o weight
10/92	DP-11	230	19	w/o weight
"	DP-12	250	19	w/o weight
"	DP-13	250	22	w/o weight
"	DP-14	250	25	w/o weight
"	DP-15	250	25	w/o weight
"	DP-16	*	15	w/o weight
"	DP-17	ok-leaks to 8 torr	15	w/o weight (perf. test)
"	DP-18	230	21	w/o weight
"	DP-19	*	30	w/o weight
"	DP-20	230	21	w/o weight (perf. test)
"	DP-21	230	22	w/o weight
"	DP-22	*	30	w/o weight
"	DP-23	235	6	w/o weight
"	DP-24	230	16	w/o weight
"	DP-25	230	2	w/o weight
11/92	DP-26	failed@200	2	w/o weight
"	DP-27	228	3	w/o weight
"	DP-28	230	3	w/o weight
"	DP-29	228	4	w/o weight
"	DP-30	228	4	w/o weight
"	DP-31	failed@220	23	w/o weight
"	DP-32	failed@232	23	w/o weight
"	DP-33	228-leaks 1.4 torr	27	w/o weight (perf. test)
"	DP-34	failed-leaks	27	w/o weight
"	DP-35	223	29	w/o weight
"	DP-36	225	29	w/o weight
"	DP-37	failed@170	24	w/o weight
"	DP-38	223	24	w/o weight (perf. test)

*missing from 182, presumably failed

Summary: 38 heatsinks altogether- 22 good, 11 failed, 4 good but for performance test only and 1 good but has small holes.

11/24/92

Figure 1

Figure 2

Silicon Thermal Conductivity

Predicted MCHS Performance with
Supercritical Hydrogen Coolant

DEWPOINT MCHS: h=17850,A1N
time= 1.00000E+02 fringes of temperature
dsf = 1.00000E+00

minval= 1.07E+02
maxval= 1.47E+02
fringe levels

Predicted Maximum Heatsink Surface
Temperature vs H2 Mass Flow, 35 atm

Heatsink Surface Temperature as a
Function of Coolant Pressure

Heat Capacity of Hydrogen as a Function of Temperature and Pressure

Predicted Heatsink Performance for Comparison to Hydrogen Flows

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Microchannel Heatsink and Manifold

Chip Layout Length: 3.27"

Cooled Area: 0.541" x 3.40"

MCHS Area: 0.787" x 3.60"

MCHS Thickness: 0.060"

Manifold Area: 0.787" x 3.60"

Cross Sectional Diagram

DEWPOINT1 Heatsink Layout on a 4 Inch Wafer:

Channel and Fin Width: 30 microns (0.00118 in)

Cooled Area: 0.541 in by 3.40 in.(13.74 mm X 86.38 mm)

Desired Channel Height: 900 microns (0.035 in) for a 30:1 Aspect Ratio

RAR 6/12/92

NOTES

UNLESS OTHERWISE SPECIFIED:

1. ALL DIMENSIONS ARE IN INCHES. TOLERANCES $\pm .005$ "
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
3. SURFACE TEXTURE PER ANSI B46.1-1978.
4. $\sqrt{16}$ ALL MACHINED SURFACES
5. BREAK SHARP EDGES .010 $\pm .005$ R OR CHAMFER
6. BAG AND TAG WITH LLNL DWG. NO. AND REV. LTR.
7. PROTECT PART AND FINISHED SURFACES DURING HANDLING & SHIPPING

NO REQ		PART / LLNL STK NO		P110 SILICON		SPEC NO		ITEM	
DWN		TIM GRAFF		7/92		CLASSIFICATION		MAJOR UNIT	
CHK						THIS DOCUMENT IS THE PROPERTY OF THE UNIVERSITY OF CALIFORNIA		DEWPOINT 375W MODULE	
APVD						LAWRENCE LIVERMORE NATIONAL LAB		SUBASSEMBLY	
CLASSIFIED BY						REPRODUCTION PROHIBITED WITHOUT PERMISSION OF THE MECHANICAL ENGINEERING DEPARTMENT.		FIN STRUCTURE	
TITLE						DRAWING NO		SERIAL	
						AAA 92-106205-00			
LTR		DWN		CHK		APVD		DATE	
ZONE						SCALE		SHEET 1 OF 1	

NOTES

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TOLERANCES $\pm .005$ "
2. DIMENSIONING AND TOLERANCING PER
ANSI Y14.5-1982.
3. SURFACE TEXTURE PER ANSI B46.1-1978.
4. $\sqrt{125}$ ALL MACHINED SURFACES
5. BREAK SHARP EDGES .010 $\pm$ .005 R OR
CHAMFER
6. BAG AND TAG WITH LLNL DWG. NO. AND
REV. LTR.
7. PROTECT PART AND FINISHED SURFACES
DURING HANDLING & SHIPPING

SECTION A-A

NO REQ		PART / LINE STK NO		CORNING 7740 BOROSILICATE GLASS		SPEC NO		ITEM	
DWN		TIM GRAFF		7/92		CLASSIFICATION		MAJOR UNIT	
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TITLE						DATE		MANIFOLD	
						DRAWN BY AAA		DRAWING NO	
						DATE		AAA 92-106204-00	
						SCALE		SHEET 1 OF 1	

LTR DWN CHK APVD DATE ZONE CHANGE

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2. DIMENSIONING AND TOLERANCING PER
ANSI Y14.5-1982.
3. SURFACE TEXTURE PER ANSI B46.1-1978.
4. $\sqrt{125}$ ALL MACHINED SURFACES
5. BREAK SHARP EDGES $.010 \pm .005$ R OR
CHAMFER
6. BAC AND TAG WITH LLNL DWG. NO. AND
REV. LTR.
7. PROTECT PART AND FINISHED SURFACES
DURING HANDLING & SHIPPING

DATE	CHK	APVD	DATE	ZONE	CHANGE

P100 SILICON		SPEC NO		ITEM
NO REQD	PART / LLNL STX NO	DESCRIPTION / MATERIAL		
DWN	TIM GRAFF	7/92	CLASSIFICATION	
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4. $\sqrt{125}$ ALL MACHINED SURFACES
5. BREAK SHARP EDGES .010 $\pm$ .005 R OR CHAMFER
6. BAG AND TAG WITH LLNL DWG. NO. AND REV. LTR.
7. PROTECT PART AND FINISHED SURFACES DURING HANDLING & SHIPPING

ALUMINUM NITRIDE SURFACE SPECS:
FINISH OF 0-4 MICRONS MAX.
FLATNESS OF 40 MICRONS MAX.
BOW OF .0005"/INCH MAX.

REV	DATE	BY	CHK	APPD	ZONE
1					

NO REQ	PART / LLNL STX NO	DESCRIPTION / MATERIAL	SPEC NO	ITEM
		BACKSIDE REINFORCING PLATE		4
		MANIFOLD		3
		FIN STRUCTURE		2
		SUBSTRATE		1

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HEATSINK ACTIVE AREA

HEATSINK NOTES:
FIN WIDTH 35 MICRONS (0.001378")
CHANNEL WIDTH 25 MICRONS (0.0009843")
DESIRED CHANNEL DEPTH 900 MICRONS (0.035")
FOR A 30:1 ASPECT RATIO

NOTES

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TOLERANCES $\pm .005"$
2. DIMENSIONING AND TOLERANCING PER
ANSI Y14.5-1982
3. SURFACE TEXTURE PER ANSI B46.1-1978
4. $\sqrt{125}$ ALL MACHINED SURFACES
5. BREAK SHARP EDGES .010 $\pm .005$ R OR
CHAMFER
6. BAG AND TAG WITH LLNL DWG. NO. AND
REV. LTR.
7. PROTECT PART AND FINISHED SURFACES
DURING HANDLING & SHIPPING

NO. RECD		PART / LLNL STK NO		100MM P110 SILICON WAFER		SPEC NO		ITEM	
DWN	TIM GRAFF	10	92	CLASSIFICATION		DEWPOINT 1.2KW MODULE			
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2. DIMENSIONING AND TOLERANCING PER
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3. SURFACE TEXTURE PER ANSI B46.1-1978.
4. $\frac{125}{\sqrt{}} \sqrt{}$ ALL MACHINED SURFACES
5. BREAK SHARP EDGES $.010 \pm .005$ R OR
CHAMFER
6. BAG AND TAG WITH LLNL DWG. NO. AND
REV. LTR.
7. PROTECT PART AND FINISHED SURFACES
DURING HANDLING & SHIPPING
8. SURFACE SPECS:
FINISH OF 4 MICROINCHES MAX.
FLATNESS OF 40 MICROINCHES MAX.
BOW OF .0005"/INCH MAX.

NO. REQD.		PART / LLNL STX NO.		ALUMINUM NITRIDE		SPEC NO.		ITEM	
DWN		TIM GRAFF		CLASSIFICATION		ALCON UNIT		DEWPOINT 1.2KW MODULE	
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Engineering Note

Lee Evans

DATE 22 FEB 1993

SUBJECT

DEWPOINT heatsink to substrate foil bond fixture

mchstpu:9/18/92 30:1 Supercritical Hydrogen for DEWPOINT
1.500e-03 wt, wafer thickness m
0.900e-03 hc, channel height m
0.30e-04 wc, channel width m
0.30e-04 wf, fin width m
35.0 tempi, °K
0.1817e-04 flow, m**3/s
9.0e-02 flowid, m
13.75e-03 flolen, m
1500 nc, number of channels(i5)
30 ns, number of segments for calculations
6.87e+06 heatfl
9.0e-02 heawid, m width of the heated area
1.6e-03 healen, m length of the heated area
0.5e-04 treinf, m thickness of the Si reinforcing layer
0.5e-07 tsiol, m thickness of the glass insulating layer
0.1e-05 taubnd, m thickness of the Au bond layer
0.1e-05 tdevs, m thickness of the device substrate

mchstpu:9/18/92 30:1 Supercritical Hydrogen for DEWPOINT

wafer thickness(m)= 0.1500E-02 height of cooling channel(m)= 0.9000E-03
channel width(m)= 0.3000E-04 fin width(m)= 0.3000E-04
conductivity of the coolant(W/mK)= 0.8609E-01 and the wall mat'l= 0.9304E+03
wc/hc= .033 hD/k= 7.749 phi= 22.961
total coolant flow(m**3/s)= 0.1817E-04 l/min= 0.1090E+01 gpm= 0.2880E+00
flow width(m)= 0.9000E-01 flow length(m)= 0.1375E-01
heated width(m)= 0.9000E-01 heated length(m)= 0.1600E-02
flow velocity(m/s)= 0.4486E+00 Re= 0.2137E+03 Pr= 0.1330E+01
number of channels= 1500 xnc=1500.000
heat flux= 0.6870E+07 flow/chan= 0.1211E-07
mass flow rate= 0.9999E-03 (mass flow rate)/W= 0.1011E-05
heated area= 0.1440E-03 total heat flux= 0.9893E+03
pressure drop(pa)= 0.2312E+04 (psi)= 0.3353E+00
thickness:devs,m)= 0.1000E-05 bond = 0.7871E-38 SiO2 layer 0.5000E-07
hydraulic diameter(m)= 0.5806E-04 charateristic length(m)= 0.1120E-02
fin effectiveness= 0.8289E+00 alphaetaf= 0.2537E+02
optimums:aspect ratio= 0.36E+02 channel width(m)= 0.92E-04 channel height= 0.44E-02
coolant temperature rise(deg C/W)= 0.6343E-04
convective thermal resistance= 0.3431E-05
conductive thermal resistance= 0.7766E-06
caloric thermal resistance= 0.4139E-06
tc= 0.350E+02°K ts= 0.578E+02°K thermal res.= 0.332E-05m^2(°K)/W
rhoc= 0.550E+02kg/m^3 cpc= 0.190E+05J/kg°K velc= 0.449E+00m/s Re= 0.214E+03
tc= 0.368E+02°K ts= 0.606E+02°K thermal res.= 0.346E-05m^2(°K)/W
rhoc= 0.509E+02kg/m^3 cpc= 0.218E+05J/kg°K velc= 0.485E+00m/s Re= 0.239E+03
tc= 0.384E+02°K ts= 0.631E+02°K thermal res.= 0.360E-05m^2(°K)/W
rhoc= 0.469E+02kg/m^3 cpc= 0.246E+05J/kg°K velc= 0.527E+00m/s Re= 0.262E+03
tc= 0.398E+02°K ts= 0.656E+02°K thermal res.= 0.374E-05m^2(°K)/W
rhoc= 0.429E+02kg/m^3 cpc= 0.268E+05J/kg°K velc= 0.576E+00m/s Re= 0.284E+03
tc= 0.411E+02°K ts= 0.679E+02°K thermal res.= 0.389E-05m^2(°K)/W
rhoc= 0.392E+02kg/m^3 cpc= 0.281E+05J/kg°K velc= 0.630E+00m/s Re= 0.305E+03
tc= 0.424E+02°K ts= 0.701E+02°K thermal res.= 0.404E-05m^2(°K)/W
rhoc= 0.357E+02kg/m^3 cpc= 0.282E+05J/kg°K velc= 0.692E+00m/s Re= 0.326E+03
tc= 0.436E+02°K ts= 0.725E+02°K thermal res.= 0.421E-05m^2(°K)/W
rhoc= 0.327E+02kg/m^3 cpc= 0.263E+05J/kg°K velc= 0.756E+00m/s Re= 0.346E+03
tc= 0.449E+02°K ts= 0.750E+02°K thermal res.= 0.437E-05m^2(°K)/W
rhoc= 0.299E+02kg/m^3 cpc= 0.251E+05J/kg°K velc= 0.826E+00m/s Re= 0.367E+03
tc= 0.463E+02°K ts= 0.775E+02°K thermal res.= 0.454E-05m^2(°K)/W
rhoc= 0.274E+02kg/m^3 cpc= 0.232E+05J/kg°K velc= 0.900E+00m/s Re= 0.387E+03
tc= 0.478E+02°K ts= 0.801E+02°K thermal res.= 0.470E-05m^2(°K)/W
rhoc= 0.252E+02kg/m^3 cpc= 0.215E+05J/kg°K velc= 0.979E+00m/s Re= 0.406E+03
tc= 0.494E+02°K ts= 0.827E+02°K thermal res.= 0.484E-05m^2(°K)/W
rhoc= 0.232E+02kg/m^3 cpc= 0.200E+05J/kg°K velc= 0.106E+01m/s Re= 0.420E+03
tc= 0.511E+02°K ts= 0.851E+02°K thermal res.= 0.495E-05m^2(°K)/W
rhoc= 0.215E+02kg/m^3 cpc= 0.186E+05J/kg°K velc= 0.115E+01m/s Re= 0.428E+03
tc= 0.530E+02°K ts= 0.875E+02°K thermal res.= 0.502E-05m^2(°K)/W
rhoc= 0.200E+02kg/m^3 cpc= 0.175E+05J/kg°K velc= 0.124E+01m/s Re= 0.427E+03
tc= 0.550E+02°K ts= 0.897E+02°K thermal res.= 0.506E-05m^2(°K)/W
rhoc= 0.186E+02kg/m^3 cpc= 0.165E+05J/kg°K velc= 0.132E+01m/s Re= 0.414E+03
tc= 0.571E+02°K ts= 0.921E+02°K thermal res.= 0.509E-05m^2(°K)/W
rhoc= 0.175E+02kg/m^3 cpc= 0.157E+05J/kg°K velc= 0.141E+01m/s Re= 0.390E+03
tc= 0.593E+02°K ts= 0.941E+02°K thermal res.= 0.506E-05m^2(°K)/W
rhoc= 0.164E+02kg/m^3 cpc= 0.151E+05J/kg°K velc= 0.150E+01m/s Re= 0.421E+03
tc= 0.616E+02°K ts= 0.966E+02°K thermal res.= 0.509E-05m^2(°K)/W
rhoc= 0.155E+02kg/m^3 cpc= 0.147E+05J/kg°K velc= 0.160E+01m/s Re= 0.414E+03
tc= 0.640E+02°K ts= 0.990E+02°K thermal res.= 0.509E-05m^2(°K)/W
rhoc= 0.146E+02kg/m^3 cpc= 0.144E+05J/kg°K velc= 0.169E+01m/s Re= 0.407E+03
tc= 0.665E+02°K ts= 0.101E+03°K thermal res.= 0.508E-05m^2(°K)/W
rhoc= 0.137E+02kg/m^3 cpc= 0.141E+05J/kg°K velc= 0.180E+01m/s Re= 0.400E+03
tc= 0.690E+02°K ts= 0.104E+03°K thermal res.= 0.506E-05m^2(°K)/W
rhoc= 0.130E+02kg/m^3 cpc= 0.139E+05J/kg°K velc= 0.190E+01m/s Re= 0.393E+03
tc= 0.715E+02°K ts= 0.106E+03°K thermal res.= 0.502E-05m^2(°K)/W
rhoc= 0.123E+02kg/m^3 cpc= 0.138E+05J/kg°K velc= 0.201E+01m/s Re= 0.385E+03

tc= 0.741E+02°K ts= 0.108E+03°K thermal res.= 0.498E-05m²(°K)/W
rhoc= 0.117E+02kg/m³ cpc= 0.137E+05J/kg°K velc= 0.211E+01m/s Re= 0.378E+03
tc= 0.768E+02°K ts= 0.111E+03°K thermal res.= 0.493E-05m²(°K)/W
rhoc= 0.112E+02kg/m³ cpc= 0.137E+05J/kg°K velc= 0.221E+01m/s Re= 0.370E+03
tc= 0.794E+02°K ts= 0.113E+03°K thermal res.= 0.487E-05m²(°K)/W
rhoc= 0.108E+02kg/m³ cpc= 0.137E+05J/kg°K velc= 0.229E+01m/s Re= 0.363E+03
tc= 0.821E+02°K ts= 0.115E+03°K thermal res.= 0.482E-05m²(°K)/W
rhoc= 0.103E+02kg/m³ cpc= 0.138E+05J/kg°K velc= 0.239E+01m/s Re= 0.355E+03
tc= 0.848E+02°K ts= 0.118E+03°K thermal res.= 0.476E-05m²(°K)/W
rhoc= 0.981E+01kg/m³ cpc= 0.139E+05J/kg°K velc= 0.252E+01m/s Re= 0.348E+03
tc= 0.875E+02°K ts= 0.120E+03°K thermal res.= 0.471E-05m²(°K)/W
rhoc= 0.899E+01kg/m³ cpc= 0.140E+05J/kg°K velc= 0.275E+01m/s Re= 0.341E+03
tc= 0.902E+02°K ts= 0.122E+03°K thermal res.= 0.467E-05m²(°K)/W
rhoc= 0.949E+01kg/m³ cpc= 0.142E+05J/kg°K velc= 0.260E+01m/s Re= 0.334E+03
tc= 0.929E+02°K ts= 0.125E+03°K thermal res.= 0.463E-05m²(°K)/W
rhoc= 0.920E+01kg/m³ cpc= 0.144E+05J/kg°K velc= 0.268E+01m/s Re= 0.327E+03
tc= 0.956E+02°K ts= 0.127E+03°K thermal res.= 0.462E-05m²(°K)/W
rhoc= 0.893E+01kg/m³ cpc= 0.140E+05J/kg°K velc= 0.276E+01m/s Re= 0.321E+03

HEATSINK MANUFACTURING PROCEDURES

WAFER PROCESSING FOR KOH ETCHING

SEPTEMBER 1992

WAFERS

Should be double-polished <110>, 4" in diameter. If the heatsinks being manufactured are long (greater than 3") the wafers should not be bevelled at the edges. The bevelling takes an extra 0.2" from the edge of the wafer. The bevelling normally aids handling of the wafer since it removes the sharp edges but in this case the loss in diameter is too severe to permit.

NITRIDE

The nitride should be deposited at Stanford in the "tylannitride". Almost any recipe will work fine. The recipe used on 8/25/92 was "nitride1" with a deposition time of 35 minutes. This gave a uniform deposition of 1300Å of nitride. Stanford already has the right boat to fit in the tube which will accept 60 mil wafers. The boat can hold about 24 wafers. It is particularly important to have pinhole-free nitride, otherwise the splay and heatsink etches will ruin the heatsink.

It is generally helpful to carry out each procedure on a dummy wafer to check out machine condition, etc.

SPLAY PATTERNING

The photoresist procedures are as follows:

The photoresist (PR) is AZ1350Z

1. Singe the wafers for 30 minutes in the 120C oven.
2. Put wafer cassette in HMDS beaker for at least 3 minutes.
The HMDS acts as a stick layer for the photoresist. The HMDS contains Xylene.
3. Blow the wafers off with the air gun.
4. Spin PR in the SOLITEC with the following parameters:

Resist pour speed:	300rpm	Time:	3 seconds
Spread speed:	300rpm	Time:	5 seconds
Spin speed:	3000rpm	Time:	30 seconds
5. Softbake for 20 minutes in 90C oven.
6. Clean resist residue from SOLITEC.
7. Expose Splay pattern on Quintel. Clean the mask thoroughly in advance. Use 8 seconds exposure time. You may also use pieces of ultra-thin plastic (<1 mil) on the mask or on the wafer to prevent the mask from pulling resist from the wafer. If these pieces stick to the

wafer they should be removed with a tweezers prior to postbake. "Scotch" tape has also been successfully used.

8. Develop the wafers on the SOLITEC with the following parameters:

Spray speed: 300rpm Time: 80 seconds

Rinse speed: 300rpm Time: 30 seconds

Spin speed: 3000rpm Time: 30 seconds

9. Wipe the back-side of the wafers with a wet cloth to remove the layer of crud.

10. Postbake for 30 minutes at 120C.

11. Visually inspect the wafer to look for defects. The light of the microscope objective may be used to quickly scan the parts.

SPLAY DESCUM

Use the March asher machine in the sputtering room. Set the pressure to 100mT using the oxygen flow button (numbered 1). Set the power to 150W for 3 minutes. This is sufficient to remove a thin surface layer of resist from many wafers simultaneously.

Additional notes 9/15/92 rar

1. Turn the machine on- switch is on the back right side.
2. Place wafers in quartz tray. Move tray with special handle.
3. Put pump switch on "auto" to vent and open the chamber.
4. Close chamber with wafers inside, and change pump switch to "man" to pump down.
5. When the pressure goes to 20 mTorr (gage upper r.h.s.) hit #1 on panel to flow oxygen gas. The pressure gage should go to 100 mTorr with the gas flowing.
6. Turn the main power switch on, and then the RF power on.
7. Power level increase to 150 W, adjust C1 and C2 to zero out reflected power. This matches the load circuit with the power circuit.
8. Set the timer to allow to descum for 3 minutes.
9. Turn off procedure: RF off, Power off, gas off, vent using "auto". Takes part out and pump done to leave chamber under vacuum. When the pressure level is less than 1 mTorr, turn the machine off.

SPLAY PLASMATHERM

Two wafers may be simultaneously etched in the plasmatherm. Be sure to use covers on the wafers over the areas where the heatsinks will be. Use the following conditions to etch the nitride.

Pressure: 50mT

Flow: 50 sccm SF6 (gas 4)

Power: 150W

Time: 3 minutes

The dektak may be used to determine the etch depth into the silicon. It should measure a total of about 4 microns including the resist.

This step removes the silicon nitride (Si_3N_4) where the photoresist is not present.

1. Toggle switch to "hoist up".
2. Open "vent" on left hand panels to fill chamber with N_2 .
3. Hit both "hoist operate" buttons simultaneously to lift up.
4. Put two wafers in and cover with a Si partial wafer as a mask.
The leaves the center of the wafer with the Si_3N_4 intact even if there was inadvertent PR liftoff.
5. Hoist down toggle.
6. Hit hoist operate buttons.
7. Turn off vent
8. Turn on Rough pump. { Sometimes it is necessary to stick a screwdriver in the hoist control to get the interlock light to turn on. }
9. When pressure shows less than 1 torr, turn off the mechanical pump.
10. Turn the blower on and open the gate valve.
11. Turn the pressure set to 50 mTorr.
12. Put toggle switch #4 (SF6 etchant) on to auto in LHS control panel to turn on the mass flow.
13. In the panel for etchant control, put toggle on for etchant #4.
14. Turn the RF power generator on { most bottom switch }
15. RF power set to 150 W.
16. Make sure the flow indicator shows 50 sccm and pressure 50 mTorr.
17. Turn RF power on, using the top switch in panel with gages for applied and reflected power.
18. Set the time for 3 min.
19. When done, turn the power RF power off { left hand side of LHS upper panel }
20. Turn off mass flow, pressure set, RF power set.
21. Turn off blower, close gate valve, turn off #4 interlock toggle switch.

22. Open vent, wait 1 and 1/2 minutes to lift hoist.
23. At the end of the run, turn off the RF generator and leave chamber under vacuum.

RESIST STRIP

Remove the resist on the wafers using R10 (5 min at heatsetting 3 or 4, nominally 50 °C). An acetone spin on the SOLITEC is also permissible since the KOH will also remove any excess resist.

HF DIP

The wafers should be dipped in BOE for 1 minute prior to insertion in the KOH bath. (Optional to remove oxide on Si surface,

KOH SPLAY ETCH

Insert the wafers in the KOH etch bath in the packaging lab. The temperature should be 50C. The etch rate is 17 microns per hour. An overnight etch is preferred. 50C is the preferred temperature since higher temperatures seem to cause more defects in the wafer.

SPLAY DEPTH MEASUREMENT

Use the heidenhein to measure the depth in the open rectangle of the splay pattern. This should be recorded for each wafer.

HEATSINK PATTERNING

1. Singe the wafers for 30 minutes in the 120C oven.
2. Put wafer cassette in HMDS beaker for at least 3 minutes.
3. Blow the wafers off with the air gun.
4. Spin PR in the SOLITEC with the following parameters:
  - Resist pour speed: 300rpm Time: 3 seconds
  - Spread speed: 300rpm Time: 5 seconds
  - Spin speed: 3000rpm Time: 30 seconds
5. Softbake for 20 minutes in 90C oven.
6. Clean resist residue from SOLITEC.
7. Expose heatsink pattern on Quintel. The mask should be the one with the see through ferric oxide masking material. Clean the mask thoroughly in advance. Use 8 seconds exposure time. You may also use pieces of ultra-thin plastic (<1 mil) on the mask or on the wafer to prevent the mask from pulling resist from the wafer. If these pieces stick to the wafer they should be removed with a tweezers prior to postbake.

NOTE CAREFULLY: The mask has to be centered on the wafer to provide for optimum results. This is why the see through mask is preferred.

8. Develop the wafers on the SOLITEC with the following parameters:

Spray speed: 300rpm Time: 80 seconds

Rinse speed: 300rpm Time: 30 seconds

Spin speed: 3000rpm Time: 30 seconds

9. Wipe the back-side of the wafers with a wet cloth to remove the layer of crud.

10. A very thorough inspection is required here. Look for the following:

A. breaks in the heatsink fin lines; as long as there are less than about 4 lines broken this is acceptable.

B. holes in the resist on the rim of the heatsink. These are not acceptable

C. Scan the heatsinks using the light from the microscope to detect defects.

All rejected wafers should have the resist stripped and the photoresist patterning procedure started again.

9. Postbake for 30 minutes at 120C.

HEATSINK DESCUM

Use the thingy machine in the sputtering room. Set the pressure to 100mT using the oxygen flow button (numbered 1). Set the power to 150W for 3 minutes. This is sufficient to remove a thin surface layer of resist from many wafers simultaneously.

HEATSINK PLASMATHERM

Two wafers may be simultaneously etched in the plasmatherm. Use the following conditions to etch the nitride.

Pressure: 50mT

Flow: 50 sccm SF6 (gas 4)

Power: 150W

Time: 3 minutes

The dektak may be used to determine the etch depth into the silicon. It should measure a total of about 4 microns including the resist.

RESIST STRIP

Remove the resist on the wafers using R10. An acetone spin on the SOLITEC is also permissible since the KOH will also remove any excess resist.

The concept of the joining or bonding of the sputtered surfaces is built around essential physical requirements. For the heatsink bonding surface the silicon base region must be conditioned so as to have a high sticking coefficient. Then there must be a stick layer to act as a diffusion barrier between the silicon base material and the gold bond layer. The importance of the stick layer and its integrity cannot be minimized. Solubility and diffusion across the stick layer bonding materials, and the resulting formation of silicides can greatly reduce the integrity of the bond. Diffusion of gold along silicon crystal stacking faults could degrade the structural integrity of the heat sink itself. The integrity of this stick layer starts with a reliable and repeatable cleaning procedure and in the durability of a diffusion/stick layer. This cleaning procedure is described below. The diffusion layer described is TiN^x , and offers excellent diffusion properties for Au/Sn to Silicon bond interface.

Assembly and Cleaning

- #1 Heavily contaminated surfaces.
  - should be rinsed free with DI water
  - should be blown free with dry, clean N₂
  - soaked in DI water with wetting agent (phosphate free) for 5 to 10 min. Microclean is OK
  - should be wiped clean with soft lint free cloth (always use fresh surface away from the cut edges of wipe)
  - should be rinsed with pressure sprayed DI water and blown dry (dry clean N₂)
- #2 Stored wafer
  - Should be rinsed with pressure sprayed DI water and blown dry (dry clean N₂)
- #3 Removal of oil, hydrocarbons, and polymers
  - Surfaces should fully wetted with Acetone for 3 min.
  - Acetone and its residue should be removed with Isopropyl alcohol
  - should be rinsed with pressure sprayed DI water
  - should be soaked in DI water for 5 min. (agitate) to remove metal residues
  - should be rinsed with pressure sprayed DI water and blown dry (dry clean N₂)

- #4   Drying sample
should be placed in a vacuum oven at 120° C for 1 hr. (you should not consider the oven as a storage step without returning to step #2)
- #5   Plasma ashing
sample should be ashed in an O₂ plasma for 3 to 5 mins. With a chamber pressure of 100 mTorr and a power setting of 150 watts. (The asher is an easily contaminated machine, by nature and by the wide range of use. It is how ever one of the better ways to remove hydrocarbons and water from sample.)
Note: typically an oxygen plasma is black, It is the contaminates which contribute to the visible plasma. The visible plasma should be there as startup but a black plasma should become apparent before completion. Failure to do so could contribute to sample contamination rather than removal.
- #6   Sputtering Vacuum
Loading of the vacuum chamber should be done as quick as possible and directly from the asher. System pump down should be as described (Roughing pressure should stay well into the viscous flow, above 100 mTorr,) to minimize back streaming. Assure the heat load on the cryo does not exceed the operational paremeters. Long pump down times and loss of the cryo-head temperature will contaminate the sample.
- #7   Sputtering Stick layer
The conditioning of the stick layer target should be done first and the back etch of the sample second.
This procedure is open to arguments but it is my opinion that the back etch needs to be more closely coupled to the deposition and not the issue of cross contamination of the stick layer target. This should assure a higher energy on the sample, with a higher number of nucleation sites, faster crystalline growth, higher energy bounds and a higher sticking coefficient.

HF DIP

The wafers should be dipped in BOE for 1 minute prior to insertion in the KOH bath.

KOH HEATSINK ETCH

Insert the wafers in the KOH etch bath in the packaging lab. The temperature should be 50C. The etch rate is 17 microns per hour. For the Ultra-thin heatsink design, 70 hours are required to etch the patterns. The standard way to insert the wafers is to ensure that the trench lines are vertical, pointing up/down in the bath.

SPLAY DEPTH MEASUREMENT

Use the heidenhein to measure the depth in the open area near the splay pattern. This should be recorded for each wafer. The splay pattern itself will be deeper because of the first etch. On 60 mil wafers, we are shooting for 1200 microns depth in these open areas, which gives about 35 mils trench depth.

The DEWPOINT Foil Bonder

The bonder fixtures consists of four stainless steel stacked plates. The heatsink fits loosely into a machined opening of the alignment plate and on top of the base pressure plate. A machined groove in the alignment plate locates the substrate to the heatsink and precisely aligns them under the pressure diaphragm. The diaphragm keeper and lower pressure seal plate is bolted through the alignment plate into the base plate securing the fixture assembly. A thin diaphragm or foil of (.002") copper is then captured by the upper pressure plate, manifold, and O-Ring seal. After final alignment, the upper plate is bolted to the base assembly.

A gas (argon) from a high pressure source (100 psi) is connected to the diaphragm manifold and exerts pressure on the foil. The diaphragm transfers this pressure as a uniform force over the substrate top surface. The amount of bonding force is set by controlling the pressure, and can be continuously measured during the bonding procedure.

Small leaks in the diaphragm do not effect the force applied by the foil, as long as the pressure supply can be regulated. However, even small gas flows at leaks would tend to cool areas and produce a non-uniform temperature profile of the bond area. The integrity of the foil diaphragm may be monitored insitu by the measurement of the flow of gas to the high pressure manifold. The foil diaphragm is also carefully checked for tears or defects before installation in the bonder.

A low pressure flow of an inert or reducing gas (argon) is introduced through a port, in the lower pressure seal plate, into a manifold around the bond area. Venting of the bond area provides positive pressure of an inert gas to prevent contamination and oxidation or other reaction of the bond surfaces. It also prevents pressure buildup below the diaphragm.