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Channel Control ASIC for the CMS Hadron Calorimeter Front End Readout Module

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Abstract

The Channel Control ASIC (CCA) is used along with a custom Charge Integrator and Encoder (QIE) ASIC to digitize signals from the hybrid photo diodes (HPDs) and photomultiplier tubes (PMTs) in the CMS hadron calorimeter. The CCA sits between the QIE and the data acquisition system. All digital signals to and from the QIE pass through the CCA chip. One CCA chip interfaces with two QIE channels. The CCA provides individually delayed clocks to each of the QIE chips in addition to various control signals [1]. The QIE sends digitized PMT or HPD signals and time slice information to the CCA, which sends the data to the data acquisition system through an optical link.

I. Introduction

The CCAs and QIEs are mounted on the Hadron Calorimeter Front End Module as shown in Figure 1.

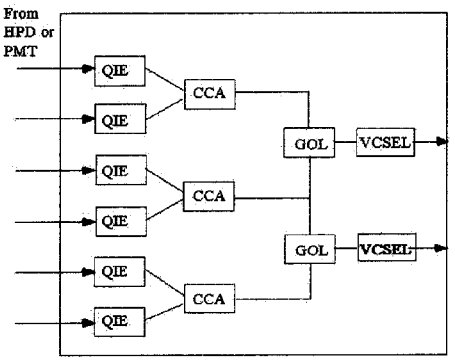

Figure 1: Front End Module block diagram

Each CCA has two channels for control of two QIEs. For efficient use of the optical fibres, three CCAs feed data to two gigabit optical links, (GOLs) that drive vertical cavity surface emitting lasers (VCSELs). Figure 2 shows the front side of the Front End Module. The VCSELs are mounted on the back of the board.

The CMS QIE is a full custom BiCMOS ASIC designed by Tom Zimmerman and Jim Hoff at Fermilab. The QIE has an embedded non-linear FADC that digitizes signals over a wide dynamic range. The QIE operates in a 4-step pipeline mode. Data is output as a 2-bit exponent and a 5-bit mantissa along with the time slice information, which is referred to as CapID, as shown in Figure 3. Choice of the PMT or the HPD input is made by connecting power to either the PMT or the HPD input amplifier in the QIE.

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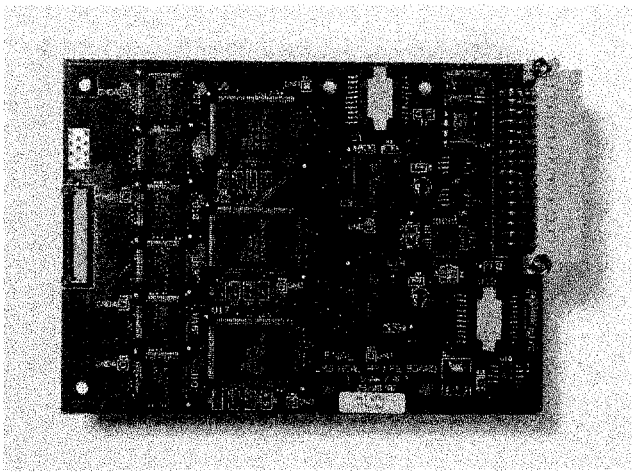

Figure 2: Front End Module circuit board

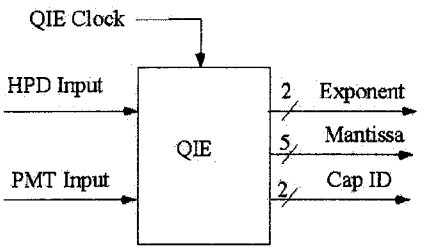

Figure 3: QIE signals

II. Operation of CCA

The CCA is a multi-function device whose design is intimately tied to the requirements of the QIEs. The CCA has two major functions:

- Send individually programmable delayed clocks to each of the QIEs, to correct for time differences within the hadron calorimeter (58 nsecs max).
- Accept exponent and mantissa information from 2 QIEs, align the data and send the data to a gigabit serializer that drives an optical link.

Other CCA functions include the following:

- Provide a serial interface similar to I^2C for programming the CCA.

- Check QIE CapIDs to see that QIEs are synchronized.
- For test purposes, force QIEs into fixed range mode instead of auto ranging mode.
- Adjust QIE pedestal level to correct for HPD leakage.
- Reset QIEs.
- Place QIE in calibration mode (special high sensitivity ADC range) for calibration with a radioactive source.
- Issue test pulse triggers of programmable polarity for either HPD or PMT operation to the QIEs.
- Flag bunch crossing counter check error.
- Provide test pattern registers to check operation of DAQ and check the optical data links.

As can be seen from the preceding list of functions, operation of the CCA is closely tied to that of the QIEs. Figure 4 shows the connections between 1/2 of a CCA, and a QIE. The common control signals for the full CCA are at the top of the figure. The specific CCA address is set by 6 lines called RBX_A that are programmed by hard wire connections on the printed circuit board.

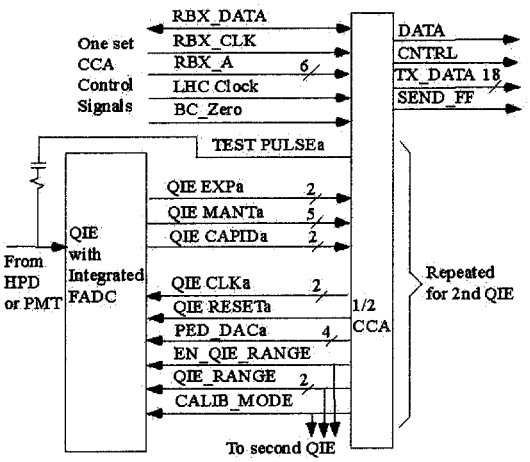

Figure 4: Signals to and from CCA

Operation of the CCA is examined by looking at four different sets of circuits.

A. *RBX interface and registers*

The RBX interface bus gets its name from the HCAL Readout Boxes. The RBX interface is a 2-wire communication interface that is similar to the well-known I^2C interface. All data is downloaded, 8 bits at a time, through the RBX_DATA line and clocked with the RBX_CLK line. Information is expected to be downloaded or read back at 100 Kbits/sec. RBX data is written to, or read from, a Pointer Register or a Data Register. The Pointer Register points to 1 of 28 eight bit internal registers as shown in Figure 5. The Data Register contains data to be written or read from the pointer address location. After each data transfer, the Pointer Register automatically points to the next internal register, to reduce chip communication overhead. For reliability, all registers are designed with SEU tolerant flip-flops [2].

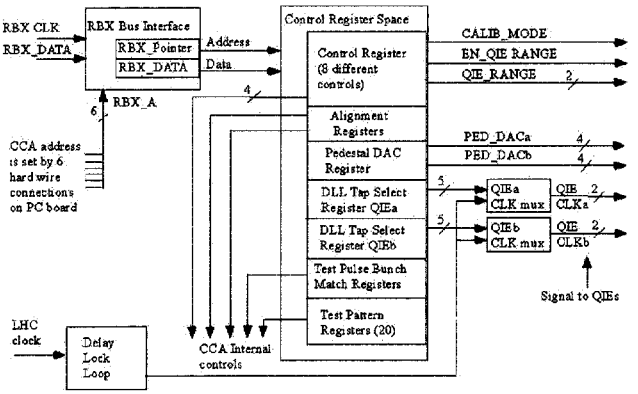

Figure 5: RBX and control register space

Figure 6 shows a typical set of instructions to download information to the CCA via the RBX bus. The first word contains the chip address, a bit (0) to choose the Pointer Register and a bit (0) to indicate a Write command. The second word uses 6 bits to indicate the internal CCA register address to be loaded in the Pointer Register. The third word again presents the chip address, sets a bit (1) to choose the Data Register, and a bit (0) to once again indicate a Write command. The next word is the data to be loaded into the internal register selected by the Pointer Register. Data can then be loaded into subsequent internal registers with each RBX bus cycle.

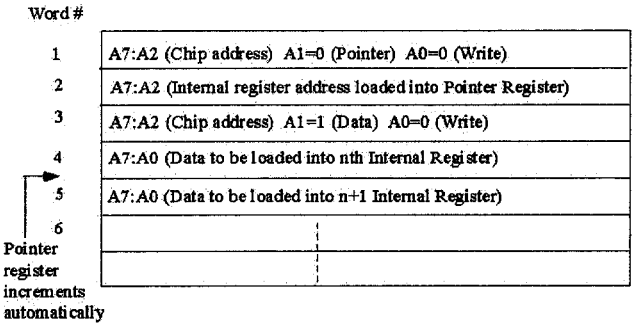

Figure 6: Typical data download to CCA via RBX bus

Figure 5 shows the 28 internal CCA control registers. The functions of the registers are as follows:

- **Control Register** - 1 register to set various internal CCA controls and control settings for QIEs.
- **Alignment Control Registers** - 2 registers, one for each of two QIEs for the purpose of selecting various timing options to permit channel operation with timing differences up to 58 nsec.
- **Pedestal DAC Register** - 1 register for two QIEs wherein 4 bits are used for each QIE to set a pedestal in the QIE to correct for HPD leakage currents.
- **QIEa DLL Tap Setting Register** - 1 register to program DLL delay for QIEa in 1 nsec increments from 0 to 25 nsec.

• **QIEb DLL Tap Setting Register** - 1 register to program DLL delay for QIEb in 1 nsec increments from 0 to 25 ns.

• **Test bunch Counter Match Register** - 2 registers that contain the Bunch Count at which a test pulse should be fired for each QIE, providing the Enable Test Pulse bit has been set in the Control Register.

• **Test Pattern Registers** - 20 registers that contain data or test patterns. The registers are used to verify proper DAQ communication and by loading data to a specific location, they are used to verify that the optical cable has been connected to the correct channel.

B. Delay Locked Loop

The basic Delay Locked Loop is comprised of 25 one nanosecond delay stages along with a Phase Detector, a Charge Pump, and a Loop Filter as shown in Figure 7.

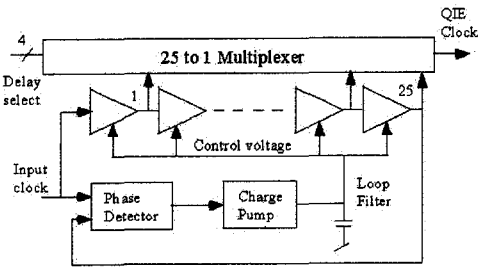

Figure 7: Delay Locked Loop

Each delay stage is comprised of two inverters. Control of the Locked Loop is accomplished by Control Voltages that are applied to the PMOS and NMOS devices in the inverters. A 25 to 1 multiplexer is used to provide fine control for the QIE clocks. The system requirement was to be able to move the clocks in 2 nsec increments. Program control for the DLL is shown in Figure 5. Each QIE has its own separate delay.

C. QIE data alignment and transmission

Seven bits from the Alignment Register are used to set 4 multiplexers in the Data Alignment block for proper data alignment of the QIE exponents, mantissas, and CapIDs from the QIEs. See Figure 8.

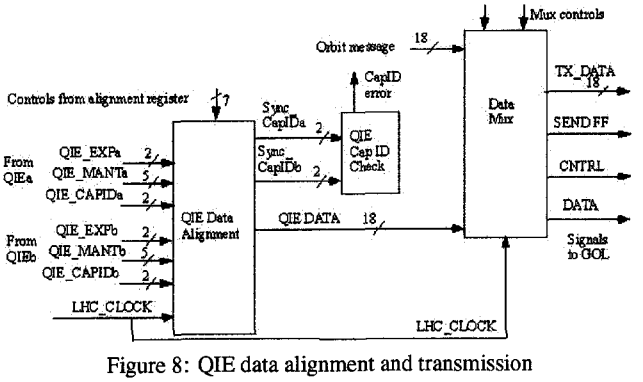

Figure 8: QIE data alignment and transmission

The CapIDs are checked for synchronization by comparing the CapID numbers (0, 1, 2, 3) from QIEa and QIEb. If the numbers do not match, a CapID error is flagged so that the data for the preceding interactions can be discarded if desired. The Data Multiplexer selects either QIE data or an Orbit Message to be sent to the GOL. The Orbit Message is transmitted when the Bunch Crossing Zero signal is received. At the same time the Orbit Message is being transmitted the QIEs are reset with CapID=0.

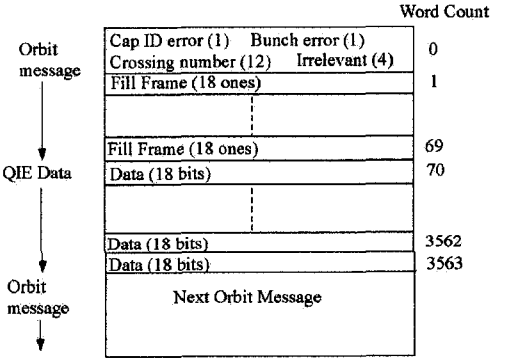

Figure 9: Typical data transmission

A typical data transmission is shown in Figure 9. After the BC0 is received, a 70 word Orbit Message is sent. The first word contains error flags and the Bunch Crossing Number that was counted by the CCA just before resetting the QIEs. Subsequent Orbit Message words contain Fill Frames for GOL synchronization or data from the Test Pattern Registers followed by Fill Frames. After the Orbit Message, QIE data is sent until BC0 is received, usually at word #3563, at which time the next Orbit Message is sent.

D. Other CCA Circuits

The remaining CCA circuits are seen in the center of the complete block diagram shown in Figure 10. The Bunch counter is a 12 bit counter that is reset by BC_Zero and then incremented by the LHC clock. When the next BC_Zero is received, the number in the Bunch Counter is compared to the pre-programmed value of 3563 in the Event Sync Check block and if the numbers do not match, a Sync error bit is sent to the Orbit Message block. The Orbit Message block takes the Sync error bit and the CapID error bit and formats them with the number from the Bunch Counter to form the first word in the Orbit Message. A separate bit from the Control Register is used to choose between the Orbit Message and QIE data to be transmitted via the Data Multiplexer.

The Test Pulse Trigger Comparator block produces a Send_Test_ Pulse signal when the programmed number in the Test Pulse Bunch Match Register equals the Bunch Counter number. The test pulse is one LHC clock cycle long. Polarity of the test pulse is programmed through a bit in the Control Register. Opposite polarity test pulses are used for HPDs and PMTs.

The Synchronizer block synchronizes test pulses for the two QIEs which may have different clock delays so that the test pulses occurs in the same time slice. This circuit also synchronizes the QIE reset pulses.

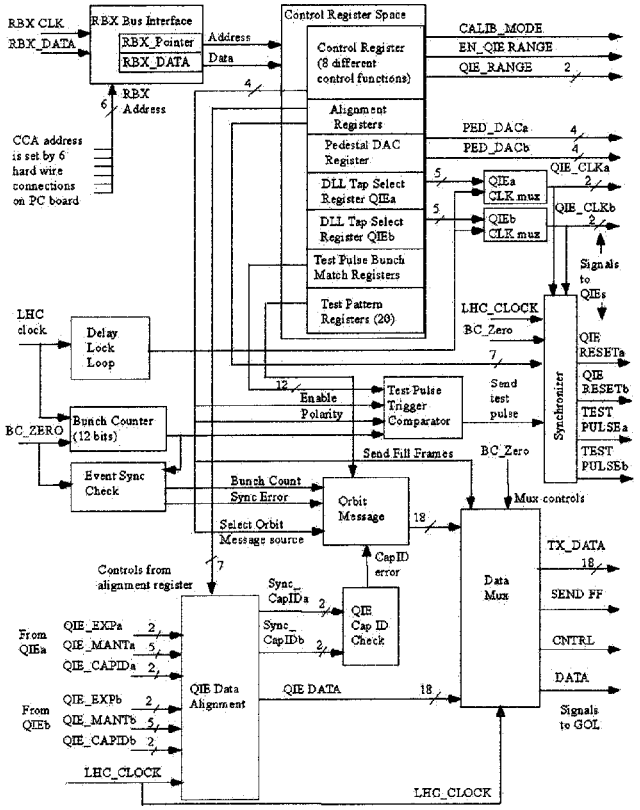

Figure 10: CCA complete block diagram

III. PRODUCTION PARTS

The CCA was produced in the Agilent 0.5 micron CMOS process. The die, which is shown in Figure 11, is 3.4 mm x 4.0 mm.

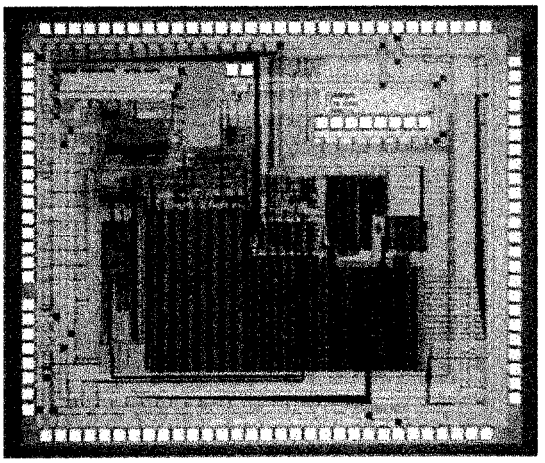

Figure 11: CCA die

A production run of 11,400 parts (22,800 channels) has been completed. The part is packaged in a 128 pin QFP that is 14 mm x 20 mm.

IV. TEST RESULTS

An initial lot of 500 CCA chips were packaged to check chip yield. An automated test set-up was developed to test the parts. Twenty-one separate measurements were made looking at such things current draw, writing and reading registers, functionality of all signals, and the programmed time delay for the QIE clocks. Initial measurements were made on 200 parts to establish cuts for the current draw (+/- 15%)and delay variations (+/- 2 nsec). After adding cuts to the test program, 227 chips were tested. Of those parts, 222 were found to be good for a yield of 97.8%. It is planned to package and test the remaining 10,900 parts in the near future.

V. CONCLUSION

The design of the Channel Control ASIC for the CMS hadron Calorimeter has been completed and a production quantity of devices has been fabricated. The CCA has been tested with QIEs and meets all of the requirements for the CMS application. Preliminary testing of the packaged parts indicates a very high yield.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

1) Theresa Shaw, et.al., "Specification for the CMS Hadron Calorimeter Front End Readout Module Channel Control ASIC", Revised March 8, 2002.

2) M. Liu, S. Whitaker, "Low Power SEU Immune CMOS Memory Circuits", IEEE Transactions on Nuclear Science, Vol. 39, No. 6, pp. 1679-1684, December 1992.