Radiation Tolerance of Prototype BTeV Pixel Detector Readout Chips

G. Chiodini, J.A. Appel, G. Cardoso, D.C. Christian, M.R. Coluccia, B. Hall, J. Hoff, S.W. Kwan, A. Mekkaoui, R. Yarema, S. Zimmerman, and L. Uplegger.

***Abstract*-- High energy and nuclear physics experiments need tracking devices with increasing spatial precision and readout speed in the face of ever-higher track densities and increased radiation environments. The new generation of hybrid pixel detectors (arrays of silicon diodes bump bonded to arrays of front-end electronic cells) is the state of the art technology able to meet these challenges.**

We report on irradiation studies performed on BTeV pixel readout chip prototypes exposed to a 200 MeV proton beam at Indiana University Cyclotron Facility. Prototype pixel readout chip preFPIX2 has been developed at Fermilab for collider experiments and implemented in standard 0.25 micron CMOS technology following radiation tolerant design rules. The tests confirmed the radiation tolerance of the chip design to proton total dose up to 87 MRad. In addition, non destructive radiation-induced single event upsets have been observed in on-chip static registers and the single bit upset cross section has been extensively measured.

I. Introduction

BTeV is planed to run at the Fermilab Tevatron collider. The experiment is designed to cover the "forward" region of proton-antiproton interactions and to study mainly particle-antiparticle mixing, CP violation, and rare decays of hadrons containing the beauty quark [1].

One of the key elements of BTeV is its vertex detector based on hybrid silicon pixel devices. It provides high precision space points for reconstruction of charged tracks in close proximity to the interaction region. The detector consists of thirty planar array of 10 by 10 cm^2 silicon pixel stations arranged perpendicular to the beam and sitting inside a dipole magnet (about 1.6T). Each station is realized with two L-shaped substrates staggered along the beam axis and covered by pixel sensors on both sides. The elementary block forming the pixel detector is an assembly (module) of one long sensor with several readout chips bump bonded to it and a flex circuit carrying power and signal traces. The pixel sensor and the read out chips are the only active electronics parts on the module. In fact, the chips are controlled and read out by FPGA's located outside the magnet. Due to the long interaction region along the beam direction (about 30 cm rms) most of the pixel detectors are crossed by particles coming from both directions.

At a nominal luminosity of $2 \cdot 10^{32}\ cm^{-2}s^{-1}$, the "hottest" chip, located at 6 mm from the beam, is going to be exposed to about 3.5 $Mrad \cdot y^{-1}$. The radiation field is mostly composed of charged hadrons, neutrons, electrons and gammas. The particle flux of these species decreases as an inverse power of the radial distance (the neutron flux reaches a plateau just outside the vertex detector) and they have a broad energy spectrum up to about 100 GeV. The pixel detector will experience a large total ionizing dose and neutron flux. Consequently, the front-end electronics, covering entirely the active area of the sensors, must be very radiation tolerant.

II. Radiation damage in CMOS devices

The front-end electronics for hybrid pixel detectors is realized in CMOS technology in order to keep the amount of power dissipation to a manageable level (about 0.5 $W \cdot cm^{-2}$). CMOS devices are sensitive to ionizing radiation due to the positive charge-up of the silicon oxide. The trapped charge causes a voltage threshold shift (charge-up of gate oxide), leakage current increases within NMOS devices (charge-up of the oxide surrounding the device) and between NMOS devices (charge-up of the oxide separating devices).

The radiation damage can be greatly reduced by using commercial deep-submicron technology for ASIC design instead of military hardened technologies. There are other major advantages in following the commercial trend such as: higher circuit density, higher yield, better reliability, and lower cost.

In this technology, the gate oxide thickness is so small (t_{ox} < 6 nm) that electron tunneling is extremely effective in removing trapped charge and stopping the formation of interface states. On the other hand, even in deep-submicron technology, the field oxide between devices is relatively thick. This means that radiation-induced leakage currents must be prevented by special layout rules. For example employing enclosed-gate devices and devices with guard rings, the leakage currents are prevented from flowing

Manuscript received July 15, 2002.

This work is supported by Fermilab National Accelerator Laboratory, which is operated by Universities Research Association under contract with the US Department of Energy.

Corresponding author G. Chiodini, Fermi National Accelerator Laboratory P.O. Box 500 Batavia, IL 60510, USA (telephone: 630-840-5151, e-mail: chiodini @fnal.gov).

The first eleven authors are with Fermi National Accelerator Laboratory P.O. Box 500 Batavia, IL 60510, USA.

The last author is with Istituto Nazionale di Fisica Nucleare Milano, via Celoria 16 – 20133, Italy.

respectively drain and source and between devices. Following these layout rules [2] the radiation hardness is found to increase enormously.

However, Total Ionizing Dose (TID) effects are not the only concern in a radiation enviroment. Nuclear recoil can deposit enough energy density to cause Single Event Effects (SEE). There are three important SEE's in CMOS technology to be considered: Single Event Latch-up (SEL), Single Event Gate Rupture (SEGR), and Single Event Upset (SEU).

In SEL, a device supposed to be off (or a parasitic device in parallel to the real one) is suddenly turned on, providing a path from the supply to ground. A single latch-up can result in a large current and destruction of the IC or melting of wire bonds supplying power. SEL sensitivity has been observed to decrease in deep submicron processes for a variety of reasons [3] (reduced thickness of the epitaxial layer, retrograde wells, and Shallow Trench Isolation). In addition, the use of guard rings around NMOS devices helps to prevent latch-up.

In SEGR, total or partial damage of the dielectric gate material occurs due to an avalanche discharge. In reference [4], studies of the dependence of SEGR on gate oxide thickness show that the phenomenon is likely not to be a concern in deep-submicron technology. The Critical Field E_c to rupture, for a given Linear Energy Transfer (LET), increases for decreasing gate oxide thickness. In particularly, for t_{ox}< 6 nm, the critical field is higher than 7 MV·cm^{-1} for LET < 80 MV·cm^{-1}, which is significantly larger than the electric field present in dielectric gate oxide in 0.25 micron CMOS devices.

In SEU, a soft error is introduced in logic circuits due to an electric glitch positively amplified by the circuit itself. The phenomenon is not a destructive one, but it can change the state of a flip-flop or induce other unwanted logic state transitions. SEU effects are possible if the local energy deposited, or equivalently the local charge deposited, is large enough. The critical energy depends strongly on the technology used. In particular, a technology with smaller feature size generally has smaller critical energy. This does not necessary mean that the deep-submicron technology is more prone to soft errors. In fact, to cause upset, the charge must be released near a sensitive node, (often the drain of a CMOS device). The sensitive volumes are smaller for small feature size technology than for larger feature size technology. There are circuit-hardening techniques to mitigate single event upset [5], but usually these require an increase of the circuit area, complexity, and power consumptions - all factors already constrained in a readout chip for pixel sensors.

In conclusion, modern deep-submicron CMOS processes are not expected to suffer from SEL and SEGR effects, but can be quite sensitive to SEU effects. For this reason, we did proton irradiation tests with BTeV readout chip prototypes in order to verify the robustness to Total Dose and Single Event Effects.

III. The FPIX readout chip

A. Introduction

In order to satisfy the needs of BTeV, the pixel detector must provide "very clean" track crossing information near the interaction region for every beam crossing; this is every 132 ns. This requires a low noise front-end, an unusually high output bandwidth, and radiation-hard technology. A pixel readout chip (FPIX) is being developed at Fermilab to meet the requirements of future Tevatron Collider experiments [6]. In Figure 1 the FPIX chip block diagram is shown.

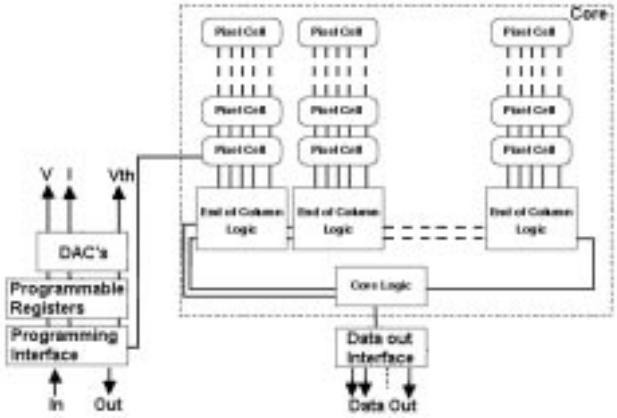

Fig. 1. Main functional blocks implemented in FPIX chips for pixel read-out.

BTeV readout chips consist of an array of 22 columns of 128 cells of 50 by 400 micron square. Each front-end cell implements a charge sensitive amplifier closed in feedback by a DC input leakage current compensation circuit. An AC-coupled amplifier further increases the analogue signal. Ultimately, a group of several discriminators form a flash ADC, providing over-threshold information and pulse-height digitization [7],[8].

The readout of a column is by end-of-column logic through token-pass signal arbitration. In the end of column, up to four timestamps can be stored and associated with the corresponding cells over threshold. Only cells over threshold are read out. The readout of the columns is arbitrated by the core logic through a column token-pass signal and the data are sent off chip by a fast data output serializer. The pixel kill and charge-injection mask registers, and digital-to-analog (DAC) registers are downloaded to the FPIX through a serial programming interface.

The mask and charge-injection registers consist of small size daisy-chained flip-flops (FF's) and are implemented in each pixel cell. A high logic level stored in one of the mask FF's disables the corresponding cell. This is meant to turn off noisy cells. Analogously, a high logic level stored in one of the charge-injection FF's enables the cell to receive in input an analogue pulse for calibration purposes. Thus, there are two independent long registers, which are serpentine through the chip. The DAC registers control features of the chip and minimize the number of connections between the chip and the outside world. In the DAC's, the stored digital value is

translated into an analogue voltage or analogue current to set bias voltages, bias currents, and discriminator thresholds.

B. The preFPIX2 chip prototypes

The preFPIX2 represents the most advanced member of a succession of pixel readout chip prototypes to date. It has been realized in standard 0.25 micron CMOS technology, following radiation tolerant design rules, from two vendors. Exposures of preFPIX2T chips to a Cobalt-60 source at Argonne National Laboratory [7] and preFPIX2I chips to protons at the Indiana University Cyclotron Facility verified the high tolerance to total dose and bulk damage [9]. In this paper, we present results of proton radiation tests performed with preFPIX2Tb chip including both total dose and single event effects. The proton irradiation tests were done exposing several chips to 200 MeV proton beam at the Indiana University Cyclotron Facility (IUCF). The preFPIX2Tb chips contain 16 columns with 32 rows of pixel cells, core readout architecture, a programming interface, and DAC's. It was manufactured by Taiwan Semiconductor Manufacturing Company. The comparison of the chip performance before and after exposure shows the radiation tolerance of the design up to about 87 Mrad total doses. In addition, we measured the SEU cross section of the static registers, in order to establish the sensitivity of our design to radiation induced digital soft errors during real operation.

IV. Experimental setup

A. Proton irradiation facility at IUCF

The proton irradiation tests took place at the Indiana University Cyclotron Facility where a proton beam line of 200 MeV kinetic energy is delivered to users. The beam profile was measured by exposing a photographic film. The beam spot, defined by the circular area where the flux is not less than 90% of the central value, had a diameter of about 15 mm, comfortably larger than the chip size (the preFPIX2Tb is 4.3 mm wide and 7.2 mm long). Before the exposure, the absolute fluence was measured by a Faraday cup; during the exposure by a secondary electron emission monitor. The cyclotron has a duty cycle factor of 0.7% with a repetition rate of about 17MHz and most of the tests were done with a flux of about $2 \cdot 10^{10}$ protons$\cdot$cm^{-2}s^{-1}. The irradiation was done with the chips powered on, in air at room temperature, and no low energy particle or neutron filters were used. The exposures were done in several steps with multiple boards about 2 cm behind each other and with the active surface of the chips facing the beam (except for one chip placed at 45 degrees and one placed at 180 degrees). Mechanically, the boards were kept in position by an open aluminum frame. The beam was centered on the chips. The physical position of the frame was monitored constantly by a video camera to ensure that no movements occurred during exposure. Due to the alignment precision and measurement technique employed, the systematic error on the integrated fluence is believed to be less than 10%.

In reference [10] the production of ions in bulk silicon by a 200 MeV proton beam is described by a Monte Carlo simulation as a two-stage process. In the first stage (internuclear cascade) the proton hits a silicon nucleus and produces light fragments, mainly forward. In the second stage, the resultant heavy ion nucleus (from nitrogen to silicon) recoils and evaporates isotropically producing further light fragments. In these inelastic collisions, the light fragments produced in the internuclear cascade, have a long range (up to more than 100 microns) and low linear energy transfer (less than 1.5 MeV$\cdot$cm^{2}mg^{-1}). The recoiling heavy ions have a shorter range (about 10 microns) and relatively high linear energy transfer (up to 14 MeV$\cdot$cm^{2}mg^{-1}) and can be very effective in causing SEU in electronics. In reference [11] the linear energy transfer threshold for SEU in a static register realized in 0.25 micron technology has been measured using ion beams of various species (i.e., various linear energy transfer values) to be 14.7 MeV$\cdot$cm^{2}mg^{-1}. This value is quite high for a 0.25 micron technology, but small enough to expect an SEU sensitivity to 200 MeV protons.

B. Hardware and software DAQ

Each chip under test was wire-bonded to a printed circuit board in such a way that it could be properly biased, controlled, and read out by a DAQ system. The DAQ system was based on a PCI card designed at Fermilab (PCI Test Adapter Card) plugged in a PCIbus extender and controlled by a laptop PC. The PTA card generated digital signals to control and read back the readout chips. The software to control the PCI card I/O busses was custom written in C. The PCI card busses were buffered by LVDS driver-receiver cards near the PCIbus extender located in the counting room. The differential card drove a 100 foot twisted-flat pair cable followed by another LVDS differential driver-receiver card which was connected with a 10 foot flat cable to the devices under test. All the DAQ electronics were well behind thick concrete walls, protecting the apparatus from being influenced by the radiation background from the cyclotron and from activated material.

V. Experimental results

A. Single Event Latch-Up

During the irradiation tests, the circuits were powered with an applied bias voltage of 2.5V. The analogue and digital currents were continuously monitored. The analogue current decreased slightly from 21 mA to 18 mA during the proton exposure and remained low also after exposure. This can be explained by a decrease of the power consumption in the flash ADC's. In fact, the bias current of the comparators diminishes slightly due to the P-MOS threshold voltage shift induced by the radiation [9]. The digital current increased slowly during irradiation and saturated at about 70 mA but returned quickly (in few minutes) to normal values when the exposure was over. No power supply trip-offs or large increases in the bias currents were observed during the irradiation. There is no

evidence of single event latch-up or of significant radiation induced leakage currents. This result is expected from reference [11] where no evidence of latch-up up to linear energy transfer of 89 MeV·cm^{2}mg^{-1} was reported.

B. Single Event Gate Rupture

The damage of a CMOS device due to Single Event Gate Rupture does not necessary mean a hard failure of the chip, but is likely to show up as performance degradation. In order to detect the occurrences of SEGR due to the proton exposure, we measured the noise and the discriminator threshold of each individual cell before and after irradiation. The presence after exposure of a pixel cell with a noise or threshold significantly different from the other ones is an indication of radiation damage localized only in those particular cells, possibly the occurrence of SEGR of individual transistors.

We made the above test for four preFPIX2I's, irradiated up to 26 Mrad [11], two preFPIX2Tb's, irradiated respectively up to 14 and 29, and one preFPIX2Tb, irradiated and measured at 14, 43, and 87 Mrad. We screened a total of about 4032 pixel front-end cells, each one containing about 550 transistors. All the cells were working before and after the irradiation, and none of them showed peculiar behavior. What has been observed after the irradiation was a slight increase of the average threshold that can be adjusted by changing an internal voltage reference (details about the FPIX2 front-end characterization after gamma and earlier proton irradiations can be found in references [7] and [11].)

Figures 2 and 3 show the noise and threshold distributions of preFPIXTb chips irradiated with proton doses of 14, 43, and 87 Mrad. The noise and threshold values reported are in electrons assuming an average calibration capacitance of 3 fF. The absolute calibration of the injection capacitance was done measuring the spectra of three different X-ray sources using a chip connected to a pixel sensor. This value is somewhat lower than the nominal 4 fF used in earlier publications by our group.

The absence of noisy cells and of large differences in individual thresholds due to irradiation, strongly suggests that single event gate rupture is not a concern in this design. For these measurements, the chips were downloaded with the same DAC values and a shift in the average threshold is clearly visible. The comparator threshold shift is not observed in gamma irradiation[7], which means it is likely to be a bulk effect. The shift is due to a change of the second stage baseline. This is believed to happen because of the combination of two effects. The first one is the threshold shift of the two P-MOS devices in series between the input and output of the second stage amplifier. The second one is the slight leakage current increase of the parasitic junction between the nwell of the two devices and the substrates. In Figure 4 the average threshold shift induced on the chip is shown as function of the total dose; and a saturation of the effect at about 40 Mrad is apparent. The digital circuitry of the chip didn't show any degraded functionality. In particularly, the digital speed remained unaltered, as inferred from the shift register download operations.

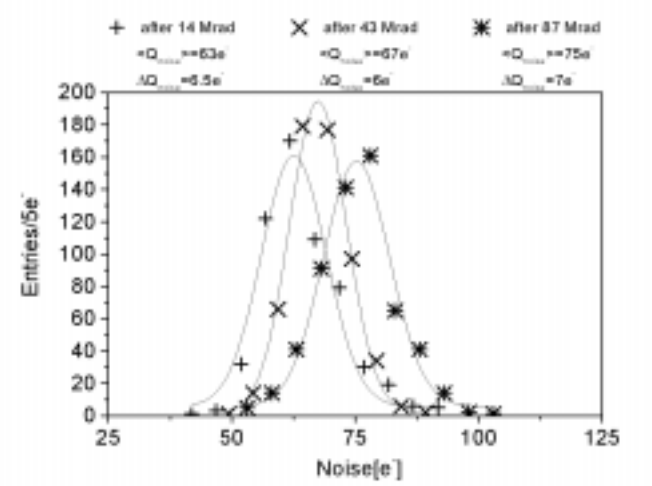

Fig. 2. Measured amplifier noise in the 576 cells of preFPIX2Tb after 14, 43, and 87 Mrad of 200 MeV proton irradiation.

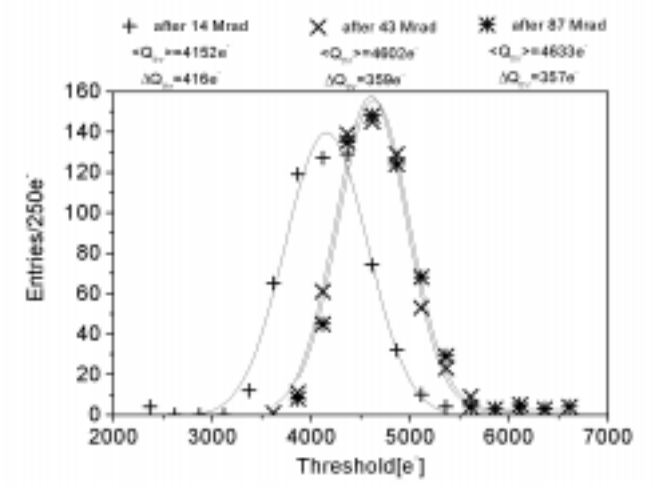

Fig. 3. Measured discriminator threshold in the 576 cells of preFPIX2Tb after 14, 43, and 87 Mrad of 200 MeV proton irradiation.

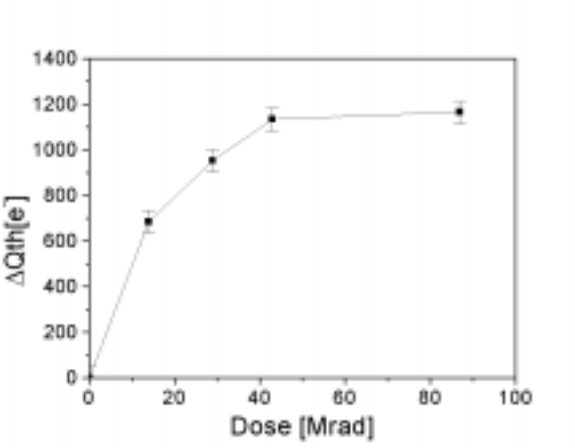

Fig. 4. Measured average threshold shift in preFPIX2Tb exposed to 200 MeV protons as a function of the total dose. The error bars represent a guessed systematic error of the measurement.

C. DAC analogue response

The analogue output of the DAC's implemented in preFPIX2Tb are available external to the chip. This means that change of the DAC behavior due to the proton irradiation can be measured. Figure 5 shows the response, before and after proton irradiation, of the DAC used to adjust the first discriminator threshold. Five curves are the deviation of the analogue response from the linear fit (also shown). The five curves are for before exposure and various total doses. The linearity and accuracy of the DAC output remain acceptable, even after 87 Mrad total doses. The highest deviation from the linear fit is seen when the most significant bit is set true. The spread can be quantified in terms of number of counts. At the extreme situation of 87 Mrad total dose, the digit inaccuracy is not more than 12 counts when the most significant bit is set to one, where 255 counts is full scale, and much less before and after.

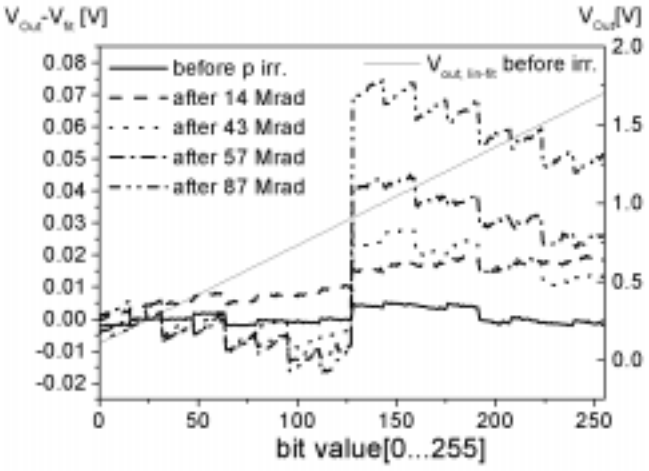

Fig. 5. The straight line corresponds to the linear fit of the DAC analog response before irradiation. The other curves are the deviations of DAC analog response with respect to this fit before and after several total dose exposures to 200 MeV protons.

D. Single Event Upset

In our tests, a great deal of attention was focused on measuring radiation-induced digital soft errors. We concentrated our effort on the preFPIX2Tb registers storing the initialization parameters, because they have a large number of bits and the testing procedure is easy to perform. The results obtained allow prediction of the performance of other parts of the chip potentially affected by the same phenomena.

VI. Testing procedure

The SEU measurements consisted of detecting single bit errors in the values stored in the registers. The testing procedure consisted of repeatedly downloading all the registers and reading back the stored values after one minute. The download and read-back phases took about 3 seconds. The download of the parameters was done with a pattern with half of the stored bits having a logical value 0 and the other half having a logical value 1. For the shift-registers, the patterns were randomly generated at every iteration loop. For the DAC registers, the patterns were kept constant. A mismatch between the read-back value and the downloaded value is interpreted as a single event upset due to the proton irradiation. No errors were observed in the system with the beam off and running for 10 hours. A summary of the total single bit errors detected in the preFPIX2Tb readout chips, together with other relevant quantities, is shown in Table 1. The rate of single bit upsets is statistically consistent among the various chips.

To explore a possible dependence of the error rate on the beam incident angle, we placed one chip at 45 degrees and another one facing the beam from the substrate side (fifth and eighth chip in Table 1). The data do not show any statistically significant difference in error rate among the three beam orientations, suggesting that SEU phenomena aren't affected by the proton incident angle in deep-submicron technology.

Moreover, we didn't see any increase of the upset rate for a chip indium bump bonded to a pixel sensor prototype (last board of table 1). This means that high Z secondary ions (bigger atomic number than silicon), produced by protons crossing the bumps of indium, stop before the reach of the readout chip.

In separate tests, the mask register of one board was operated in clocked mode with a clock frequencies of 380 kHz and 16 MHz. The corresponding results are reported in the next section but not in Table 1.

Board #	Int. flu. [10^{14} cm^{-2}]	Bit errors in Mask [2 · 576 = 1152 bit]	Bit errors in DAC [14·8 = 112 bit]
26	2.33	18↑+35↓	10
9	3.65	22↑+52↓	19
7	3.65	27↑+59↓	19
29	3.65	23↑+57↓	20
26 (45°)	3.65	14↑+63↓	31
11	2.6	10↑+38↓	20
26	5.0	28↑+85↓	32
12 (180°)	5.0	15↑+79↓	23
4 (with sensor)	4.0	24↑+53↓	23
Total	35.93	194↑+982↓	197

Table 1. Total single bit errors observed in mask and DAC registers of preFPIX2Tb exposed to 200 MeV proton beam (an upper arrow means a transition from 0 to 1 and a down arrow means a transition from 1 to 0). The horizontal table line separates boards irradiated in various tests.

VII. SEU cross section

It is common practice to express the error rate in a register as a single bit upset cross section σ_{SEU}, defined as the number of errors per bit per unit of integrated fluence:

$$N_{errors} = FN_{bit}\sigma_{SEU}$$

where N_{errors} is the number of upsets, F is the integrated fluence, and N_{bit} the number of bits exposed.

The single bit upset cross-sections have been computed for the shift-registers in unclocked and clocked mode, and for the DAC registers in un-clocked mode. The results are shown in Table 2. Only the statistical error on the cross section has

been considered. For the shift-registers, the cross section has been computed separately for the radiation induced transition from 0 to 1 and from 1 to 0 because the data have enough precision to show the existence of an asymmetry.

Register	Mode	SEU cross-section [10^{-15} cm^{2}bit^{-1}]
Mask : from 0 to 1	Un-clocked	0.94±0.07
Mask : from 0 to 1	Clocked at 16 MHz	1.6±0.5
Mask : from 1 to 0	Un-clocked	2.81±0.12
Mask : from 1 to 0	Clocked at 0.380 MHz	4.2±1.2
Mask : from 1 to 0	Clocked at 16 MHz	7.2±1.0
DAC	Un-clocked	4.9±0.35

Table 2. Single bit upset cross section for 200 MeV protons measured in mask and DAC registers of preFPIX2Tb under different clock modes.

The high beam fluence used during the irradiation was of some concern regarding saturation effects in the error rate. To study this, we collected some data at a fluence of about $4 \cdot 10^9$ protons$\cdot$cm^{-2}s^{-1}, about 5 times less than the nominal fluence. In this short test, only one board was irradiated and the single bit cross section was measured to be statistically compatible with the results at higher fluence.

VIII. Discussion

The prediction of the single bit upset cross-section is very difficult because a lot of parameters came into play [12]. Nevertheless, some gross features of the data can be understood simply. The disparity in the cross section between the shift registers and the DAC registers is likely caused by the different size of the active area of the NFET transistors, which are larger for the DAC register FF's. Besides that, the DAC register FF's have a more complicated design and an increase in complexity, as a rule of thumb, translates to a larger number of sensitive nodes that can be upset.

The SEU asymmetry for the transition from 0 to 1 with respect to 1 to 0 can be explained in terms of the FF design. The FF's of the shift-registers are D-FF's implemented as cross-coupled nor-not gates. Such a configuration has different sensitive nodes for 0 to 1 and 1 to 0 upsets. No such an asymmetry is expected for the DAC registers because the FF's are D-FF's implemented as cross-coupled nor-nor gates. This symmetric configuration has the distribution of sensitive nodes for low logical level the same as when a high logical level is stored.

The SEU data taken with a shift-register in clocked mode seem to show an increase of upset rate with respect to the un-clocked mode data. Nevertheless, in only one case does the cross-section differ significantly for the two modes; this corresponds to the shift-register clocked at 16 MHz and for the transition from 1 to 0. In this case the increase of SEU cross-section is about 2.6±0.4 .

In reference [10], a beam angular dependence is expected for devices with very thin sensitive volumes that have linear energy transfer threshold over 1 MeV$\cdot$cm^{2}mg^{-1} and tested with 200 MeV protons. We didn't observe any dependence of the upset rate on the beam incident angle. In fact, due to the smaller device size of the deep-submicron elements, the sensitive volumes are more cubic than slab shaped.

IX. Impact of SEU on BTeV vertex detector

The insensitivity of the upset rate observed in our test with respect to the beam incident angle gives some confidence that the upset cross section doesn't depend significantly on the direction of the incoming particle. Moreover, the recoiling ions causing upset in the electronics have a short range, so the material surrounding the readout chips is unlikely to generate secondary ions that can increase the upset rate. This is confirmed by our tests with beam incident at 45 degrees and on the backside of the chip, and with the chip bump bonded to a pixel sensor.

In the BTeV experiment environment the upset rate due to the electromagnetic component of the radiation field (gammas and electrons) can be neglected, because they produce few secondary ions in material. Table 3 shows the expected upset rate due to charged hadrons, high energy neutrons, and low energy neutrons for the different kinds of registers implemented in the FPIX2 chips.

The cross section values used for the registers are the one measured in our tests and should represent very conservative estimates. In fact, SEU upset cross-section for protons saturates at about 200 MeV kinetic energy and is higher than the cross-section for neutrons or pions for most of the energy spectrum involved. The data output serializer SEU cross-section is going to be measured this summer with a dedicate serializer prototype operated at nominal output speed of 140 Mbit$\cdot$s^{-1}. Therefore, in this calculation, we use the DAC register SEU cross section increased linearly up to 140 MHz frequency clock assuming a scale factor of 0.16$\cdot$MHz^{-1} as measured in our test for the mask registers. With such an assumption, the serializer SEU cross section is equal to about 10^{-14} cm^2. We have to keep in mind that an increase in upset rate in the serializer can be expected when clocked at high frequency, but we don't expect an intolerable rate of soft errors. The expected SEU bit error rate in the BTeV pixel vertex detector is small enough that it will not be necessary to design explicitly SEU tolerant registers. We believe that the SEU rate can be comfortably handled by a periodic read-back of the chip configurations during the data taking and a re-download of the chip configuration when an upset is detected.

	Charged Hadrons	Neutrons [E>1.4 MeV]	Neutrons [E>14 MeV]
Total Flux [plane^{-1}s^{-1}]	1.4×10^8	1.5×10^7	2.0×10^7
Kill or Inject [error$\cdot$h^{-1}]	14	1.5	2
DAC [error$\cdot$h^{-1}]	3	0.3	0.4
24 bit Serializer [error$\cdot$h^{-1}]	13	1.4	2

Table 3. Particle fluxes integrated on one pixel plane in BTeV experiment and the predicted single bit error rate for different registers at luminosity L = $2 \cdot 10^{32}$ cm^{-2}s^{-1}. The serializer SEU cross section is assumed to be 10^{-14} cm^{2}bit^{-1}.

X. Conclusions

Total dose and single event tests validate the deep submicron CMOS-process FPIX2 designs as radiation tolerant, particularly suitable for exposure to large integrated total dose. No evidence of catastrophic failure or deterioration of the readout chip functionality at full speed has been observed up to dose of 87 MRad (200 MeV protons). The single event upset cross sections of static registers are relatively small, but measurable (from 10^{-16} to $6 \cdot 10^{-16}$ cm^2). The expected SEU bit error rate in the BTeV vertex detector is manageable and does not require further SEU hardened registers to be implemented.

XI. Acknowledgements

We thank A. Deyer, G. Dychakowsky, and K. Knickerbocker for their help at Fermilab. We thank Chuck Foster and Ken Murray for the generous technical and scientific assistance they provided us during the irradiations at IUCF.

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