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Single Event Upset Rate of 140Mb/s Pixel-Data Serializer

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Abstract

We report on high-dose irradiation studies performed with a 200 MeV proton beam on a 140 Mbit/s pixel-data serializer prototype realized in standard 0.25 micron CMOS technology. The data serializer was implemented recently for the BTeV pixel readout chip developed at Fermilab.

Pixel, Readout Chip, Serializer, Single Event Upset, Proton Irradiation

1. Introduction

Hybrid pixel detectors are the state-of-the-art technology for vertex detectors required for high track density, fast readout, and high radiation tolerance. The necessity to minimize the number of output signals, without compromising the high readout bandwidth, requires the use of fast data output serial links. In the new generation of experiments at hadron colliders, an intense radiation field is present, which can induce Single Event Upsets (SEU) in the data transmission. These soft errors can result in data corruption, equivalent to digital noise, and loss of driver-receiver synchronization, introducing readout dead time.

2. BTeV Pixel-Data Serializer

The BTeV experiment covers a “forward” region of proton-antiproton interactions at Fermilab’s Tevatron Collider. [1]. It employs, near the interaction region, a vertex detector based on hybrid silicon pixel modules (each an assembly of one long sensor with several readout chips bump bonded to it). At the nominal luminosity of $2{\cdot}10^{32}\,cm^{-2}s^{-1}$, the “hottest” chip, located at 6 mm from the beam, will be exposed to about 3.5 Mrad per year.

We have prototyped a pixel-data serializer in standard 0.25μm CMOS technology, following radiation-tolerant layout rules. The serializer was

implemented recently on a full-size BTeV pixel readout chip (FPIX2) developed at Fermilab [2].

The on-chip pixel data will be sent to FPGA's, located 30 feet away in a low-radiation area. The transmission protocol is point-to-point, using Low Voltage Differential Signaling (LVDS) serial links. In order to maximize the data throughput, the FPGA's latch the signals on both the rising and falling edges of the clock. The 24-bit long hit data (5 column-number bits, 7 row-number bits, 3 pulse-height bits, 8 timestamp bits, and 1 "word mark" bit) are serialized onto 1, 2, 4, or 6 programmable serial links. The serializer-FPGA synchronization is established and maintained by sending a "Sync/Status" word when no data are to be sent and just before each time the "Token-Pass" signal is launched to the 1st pixel column. See reference [3] for more details of the BTeV pixel architecture.

3. Single Event Upset Testing Procedure

An SEU test was performed by exposing a pixel-data serializer prototype to a 200 MeV proton beam at the Indiana University Cyclotron Facility (IUCF). The average flux was about $2\cdot10^{10}cm^{-2}s^{-1}$. The prototype was properly biased and clocked at 70 MHz by means of an FPGA located on a custom made PCI card developed at FNAL. The computer with PCI card was 30 feet from the irradiation area, behind concrete walls. The testing procedure consisted of counting the number of wrong bits and wrong words, as latched and stored by the FPGA. When an error was detected, a global reset was asserted and the error counting cycle started again after the serializer-FPGA synchronization was re-established. The reset cycle takes at most the time needed to send two 24-bit long words. This procedure was automatically performed by the FPGA, but the error counter contents were saved and displayed asynchronously once each minute.

4. Results

In Table 1, the numbers of bit and word errors observed are reported for the one- and six-serial-line cases. Taking into account the integral fluence and the low statistics of the data, it is not possible to see small differences in Single Event Upset rates between the two configurations.

Table 1. Measured bit errors in pixel -data serializer prototype

Int. flu [$10^{14}cm^{-2}$]	# serial lines	Word errors	Bit errors
2	1	6	14
3	6	12	24

Defining a single bit upset cross section σ_{SEU}, by Nerrors = $FN_{bit}\sigma_{SEU}$, where Nerrors is the number of upsets, F is the integrated fluence, and Nbit the number of bits exposed, we get from Table 1 that $\sigma_{SEU}=31\cdot10^{-16}cm^2$. This cross section is about one order of magnitude bigger than the one reported in [4] for static registers implemented on BTeV pixel chip prototypes[1]. By the end of the test, the serializer prototype was exposed to an integral fluence of $5\cdot10^{14}cm^{-2}$ (10^{14}[200MeV p]cm^{-2}=5.8Mrad). After the irradiation, with the beam off, we left the system running for eleven hours and no errors were detected. These tests also show the high radiation tolerance of the serializer to a total dose of 29 Mrad.

5. Conclusions

We have reported the SEU cross section of a 140Mb/s pixel-data serializer realized in the 0.25μm CMOS process. The cross section is small, but larger than the one for static registers. This may be due to the dependence of the cross section on the clock frequency. The error rate in the BTeV vertex detector is expected to be so small that it can be handled without any further SEU-hardening techniques.

References

[1] BTeV collaboration, http://www.btev.fnal.gov/ public_documents/ btev_proposal/index.html. 2002.
[2] D.C. Christian at al., Nucl. Instrum. Meth. A 435, 144 ,1999.
[3] D.C. Christian, FERMILAB-CONF-02-319-E, Dec. 2002.
[4] G. Chiodini, et al., Nucl. Instrum. Meth. A 501, 183, 2003.

[1] As reported in [4], an increase of the SEU rate with frequency was already apparent for the static registers in clocked mode.