GaAs Junction Field Effect Transistors (JFETs) offer a higher gate turn-on voltage, resulting in a better noise margin and reduced power dissipation, than the more widely employed GaAs MESFET. The primary reason the JFET has not been more widely used is the speed penalty associated with the gate/channel junction and corresponding gate length broadening. We present the ion implantation processes used for a self-aligned, all ion-implanted, GaAs JFET that minimizes the speed penalty for the JFET while maintaining the advantageous higher gate turn-on voltage. Process characterization of the $p^+$-gate implant done with either Mg, Zn, or Cd along with the co-implantation of P is presented. In addition, a novel backside channel confinement technology employing ion-implanted carbon is discussed. Complete JFET device results are reported.

INTRODUCTION:

GaAs junction field effect transistors (JFETs) operate with a higher gate turn-on voltage (~1 V) than GaAs MESFETs (~0.6 V) as a result of the higher built-in potential of the p/n junction gate of the JFET over the Schottky barrier gate of the MESFET. This characteristic translates to lower gate leakage currents, larger possible logic voltage swings, and higher noise margins for circuits based on GaAs JFETs compared to MESFETs [1]. These attributes make GaAs JFETs attractive for low power microwave and digital applications [2]. However, the higher logic swing and noise margin can be offset by slower transistor switching due to higher gate capacitance if the gate length corresponding to the junction exceeds that of the gate metallization. This gate length broadening occurs for diffused and non-self-aligned implanted gate JFETs [1]. This speed penalty is minimized by employing a refractory gate contact, self-aligned, ion implantation structure where the gate junction length more closely coincides with the gate metal contact [3]. The benefit of this self-aligned approach is evident in Fig. 1 where a non-self-aligned structure is drawn next to a self-aligned, implanted, JFET. The non-self-aligned JFET of Fig 1.a suffers from gate length broadening and gate metal overlap that increase the gate capacitance while the self-aligned, implanted, JFET of Fig. 1.b minimizes these contributions to gate capacitance. We discuss the ion implantation process steps required to realize a self-aligned GaAs JFET. Our approach achieves the enhanced-gate turn-on voltage attributed to the high built-in gate potential of the JFET while minimizing gate junction broadening and gate capacitance.
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Several authors have reported GaAs JFETs based on diffused, implanted, or epitaxial gate junctions; however, our approach is unique in using a self-aligned refractory metal gate contact with all doping done by ion implantation. R. Zuleeg et al. [4], fabricated enhancement mode n-channel GaAs JFETs using zinc diffusion to form the p+ gate region where the threshold voltage was adjusted by varying the Zn diffusion time and thereby varying the gate/channel junction depth. M. Wada et al. [1] advanced the diffused gate approach by using a vapor diffusion source to realize shallow junction depths (30 nm or less) and therefore faster transistor switching. All-implanted GaAs JFETs were first reported by G. L. Troeger et al. [5], using a non-self-aligned process with gold based gate metallization. M. R. Wilson and co-workers [6], reported an improved all-implanted GaAs JFET with Ti/Au gate metallization where gate junction capacitance was reduced with a shallow p+ gate Zn implantation. Moreover, the approaches of Troeger and Wilson do not allow self-aligning source and drain implants to be employed since the Au based gate contact is incompatible with the required implant activation anneal of 750 to 850 °C performed with the gate metal in-place. To our knowledge, there has been only one report of a GaAs JFET using implantation to self-align the gate contact. In this case, J. K. Abrokwah et al. [7], reported n-channel GaAs JFETs with a tungsten silicide gate contact and a self-aligned source and drain implant applied to an epitaxial p+ gate and n-channel structure. Abrokwah’s epitaxial approach achieved a high peak transconductance of 554 mS/mm for a 0.6 µm x 10 µm device. However, our self-aligned process, where all impurity doping is done by ion implantation, will have advantages for flexibility of device integration and cost reduction.

Our approach incorporates the advantages of a thermally stable, refractory metal gate contact that allows self-aligned source and drain implants to minimize gate length broadening while maintaining the high gate built-in potential of the p/n junction. In this paper we will focus on the issues related to the ion implantation doping of the JFET. Complete DC and microwave device results for submicron JFETs are also presented.
The key steps in fabricating the self-aligned GaAs JFET fully by ion implantation are depicted in Fig 2. A minimum of four distinct device regions must be formed via implantation. These regions are: 1) the p+-gate, 2) the n-channel, 3) the p-backside confinement layer, and 4) the n+ source and drain regions. For advanced device structures, and in particular for deep submicron gate length JFETs, the n-type doping profile is further modified under sidewall spacer regions and at lightly doped drain (LDD) regions. In the following sections the optimization of the first four regions is discussed.

**n-channel implant:**

The n-type channel region is formed by the direct implantation of a donor species. Although S, Se, and Si are all candidate n-type dopants, as with GaAs MESFETs, Si-implantation is almost exclusively employed. The implant parameters (dose and energy) are significantly different than those used for GaAs MESFETs due to the overlapping profiles of the gate, channel, and backside implants. As represented in Fig. 3, the p+-gate region and p-backside implant will compensate part of the n-channel implant profile thus requiring an increased dose compared to a GaAs MESFET channel implant. For enhancement operation ($V_{th} = 0.2$ V) the channel implant dose is $\sim 1 \times 10^{13}$ cm$^{-2}$ depending on the specifics of the activation process while a similar threshold MESFET dose is closer to $5 \times 10^{12}$ cm$^{-2}$. As with implanted MESFETs, the channel dose can be varied to adjust the threshold voltage to realize enhancement or depletion mode devices. The channel implant energy is selected so that the donor peak is intersected by the falling tail of the p+-gate implant. This channel position attempts to maximize the peak electron...
concentration in the channel for optimum transconductance while minimizing the overlap of the p⁺-gate and the channel.

**p⁺-gate implants:**

The p⁺-gate implant is the key to optimizing the JFET performance. There are several competing requirements for the p⁺-profile that must be considered. First, the surface acceptor concentration must be on the order of 3-5x10¹⁹ cm⁻³ to form an ohmic gate contact. If the gate contact is not ohmic, the surface depletion will reduce the gate turn-on potential as seen in Fig. 4 and allow excess gate leakage [3]. As the primary advantage of the JFET is the higher gate turn-on voltage, the full p/n junction barrier should be maintained by forming an ohmic gate contact. Second, the p⁺-region should have a steep profile after the implant activation anneal. This second requirement can be further separated into two conditions: a) the p-type implant species must have limited channeling to produce a sharp as-implanted profile and b) the acceptor species must not diffuse into the channel region during the implant activation anneal. Requirement 2.a can be met by either using very low implant energies or by employing relatively heavy implant species. Our approach has been to employ heavier implant species that will produce less of a channeling tail for the same implant energy due to more nuclear stopping near the surface. Figure 5 shows as-implanted SIMS profile for 45 keV, 3x10¹⁴ cm⁻² implants of three candidate ion species: Mg, Zn, and Cd. To maximize the surface concentration of the Mg-implant at 45 keV, it was implanted through a 60 nm silicon nitride cap layer to shift the peak to the surface.

![Fig 3: Calculated (with TRIM92 [8]) ion profiles for a fully implanted JFET with Zn p⁺-gate (45 keV, 3x10¹⁴ cm⁻²), Si n-channel (70 keV, 1x10¹³ cm⁻²) and C p-backside (95 keV, 3x10¹² cm⁻²) implants.](image_url)

![Fig 4: Calculated band diagram from the one-dimensional Poisson equation for an n-channel GaAs JFET with either a Schottky (assumed barrier height of 0.5 eV) or an ohmic gate contact. The Schottky gate contact reduces the gate p/n junction barrier and will reduce the gate turn-on voltage.](image_url)
The SIMS profiles of Fig. 5 clearly demonstrate the advantage of using a heavier ion to achieve a sharper as-implanted profile, however, the final device profile may be modified during the implant activation anneal. Therefore, to satisfy condition 2.b, in-diffusion of the acceptor species must be minimized. Extensive studies of acceptor implantation and annealing have shown that capless rapid thermal annealing [9, 10] and co-implantation of a column V species [11, 12, 13] can minimize acceptor redistribution. We have applied both of these techniques to maintain sharp acceptor profiles. First, the activation anneal of all the implanted dopant is performed in one RTA step between 800 and 850 °C for 15 sec. During the anneal the source and drain regions are uncapped, however, the refractory gate contact is in-place and acts as a cap for the p⁺-region. Figure 6.a shows the SIMS ion profile for a Zn-gate implant co-implanted with P as-implanted and anneal with and without the W cap. The sample annealed with the W cap had the W removed with a SF₆/O₂ RIE plasma etch prior to SIMS analysis with 5-10 nm of GaAs removed during the W overetch. Accounting for the GaAs material removal, both the capless and W-capped samples show negligible diffusion for the 850 °C RTA and therefore maintain the desirable p⁺-gate profile. P co-implantation coincident with the acceptor profile is also used to reduce the As-vacancy concentration, enhance the Ga-vacancy concentration, and thereby improve the acceptor activation on a Ga-site. By enhancing acceptor activation, interstitial diffusion is reduced [14]. Figure 6.b compares as-implanted profiles for 45 keV, 3x10¹⁴ cm⁻² Cd with and with P co-implantation. The sample with P shows a dramatic reduction of in-diffusion.

**p-backside carbon implant**

P-backside implants (a.k.a. buried p-implants) are typically employed in GaAs MESFETs and JFETs to improve channel confinement and thereby reduce output conductance and sub-threshold currents. There has been an inherent trade-off between optimizing the DC and the AC (high-frequency) performance of GaAs MESFETs or JFETs that incorporate a p-type implant below the n-type channel region. This trade-off relates to the need for a high implant dose to realize good carrier confinement, and thus low DC output conductance and sub-threshold slope, and a low dose implant to minimize the gate-to-source capacitance (Cgs) from the resulting channel/p-layer junction. Any increase in Cgs will degrade the high-frequency performance by reducing both the unity gain cutoff frequency (f₁) and the maximum oscillation frequency (fmax). This problem becomes more severe as the gate length of the transistor is reduced since carrier...
confinement is more difficult to realize, thus requiring an increased dose for the buried p-implant that in turn will degrade the high-frequency performance.

![Graph](image)

Fig. 6: SIMS profiles of (a) Zn (45 keV, 3x10\(^{14}\) cm\(^{-2}\)) co-implanted with P (62P\(_2\): 45 keV, 3x10\(^{14}\) cm\(^{-2}\)) as implanted and annealed (850 °C, 15 sec) with and without a W cap and (b) Cd (45 keV, 3x10\(^{14}\) cm\(^{-2}\)) as implanted and annealed (830 °C, 15 sec) with and without a P co-implantation (62P\(_2\): 45 keV, 3x10\(^{14}\) cm\(^{-2}\)).

Typically the p-backside implant has been formed using Be or Mg implantation; however, C has unique acceptor activation properties in GaAs that make it ideal for this application. In general, Be and Mg, the two lightest column II acceptors, achieve nearly 100% activation in GaAs after annealing at ~800 °C while implanted C typically activates at less than 50%. On the other hand, the acceptor activation of implanted C can be significantly enhanced by the co-implantation of a column III species such as Al or Ga [15]. Similarly, if C is co-implanted with Si a high donor/acceptor compensation ratio is achieved [16]. It is the realization of effective donor compensation in regions where the Si-channel implant and C-backside implant overlap that produces sharpening of the channel implant profile. The effective compensation coupled with the lower activation of the singly implanted C below the Si-channel implant makes C-implantation ideal for backside implantation.

To demonstrate the utility of C-backside implants self-aligned GaAs JFETs were fabricated using either C or Mg as the backside implant species [17]. Two backside implant doses (1.5 or 3x10\(^{12}\) cm\(^{-2}\)) were studied with the implant energy adjusted to achieve a constant projected range for both ions. The DC and microwave performance of devices with nominally the same threshold voltage were compared. The DC performance for devices with the same p-backside dose was comparable independent of ion species as summarized in Table I. As expected, the higher dose samples have better output conductance (lower g\(_{DS}\)) with lower sub-threshold leakage at the price of a drop in transconductance. However, for 0.5 μm self-aligned GaAs JFETs a 28% improvement
in $f_1$ to 28 GHz and a 46% improvement in $f_{\text{max}}$ to 43 GHz was realized for the C-backside JFET over the Mg-backside JFET over a range of gate bias conditions as seen in Fig. 7. The enhanced high-frequency performance is explained in terms of the extracted device capacitances summarized in Table II. The C-implanted devices have lower $C_{\text{gs}}$ and $C_{\text{ds}}$, particularly at the higher dose, arising from the lower acceptor concentration below the channel as a result of the lower C activation. This translates to less junction capacitance at the backside of the channel and therefore improved high-frequency performance for the C-implanted over the Mg-implanted JFET.

Table I
Summary of DC performance of 0.5 $\mu$m x 50 $\mu$m self-aligned Zn-gate JFETs for two doses of Mg or C backside implants. The channel dose has been adjusted to maintain nominally the same threshold for all devices. $I_{\text{sat}}$ and $g_m$ were measured with $V_{DS} = 1.5$ V and $(V_{GS} - V_{TH}) = 0.8$ V. $g_{DS}$ was measured at $V_{DS} = 1.5$ V and $V_{GS} = 1.0$ V.

<table>
<thead>
<tr>
<th>buried-p implant (Mg @ 210 keV, C @ 95 keV)</th>
<th>channel implant dose ($\times 10^{13}$ cm$^{-2}$)</th>
<th>$V_{TH}$ (V)</th>
<th>$I_{\text{sat}}$ (mA/mm)</th>
<th>$g_m$ (mS/mm)</th>
<th>$g_{DS}$ (mS/mm)</th>
<th>sub-threshold slope (mV/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mg: 1.5$\times 10^{12}$</td>
<td>1.2</td>
<td>0.18</td>
<td>94</td>
<td>242</td>
<td>26</td>
<td>200</td>
</tr>
<tr>
<td>C: 1.5$\times 10^{12}$</td>
<td>1.2</td>
<td>0.30</td>
<td>99</td>
<td>248</td>
<td>15.5</td>
<td>110</td>
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<tr>
<td>Mg: 3.0$\times 10^{12}$</td>
<td>1.6</td>
<td>0.23</td>
<td>100</td>
<td>201</td>
<td>6.2</td>
<td>80</td>
</tr>
<tr>
<td>C: 3.0$\times 10^{12}$</td>
<td>1.3</td>
<td>0.20</td>
<td>98</td>
<td>209</td>
<td>9.0</td>
<td>90</td>
</tr>
</tbody>
</table>

Table II
Summary of extracted capacitances (fF/mm) for 0.5 $\mu$m x 100 $\mu$m Zn-gate JFETs with Mg or C backside implants at the dose listed. Values are for $V_{DS} = 1.5$ V and $V_{GS} = 1.0$ V.

<table>
<thead>
<tr>
<th>buried-p implant (Mg @ 210 keV, C @ 95 keV)</th>
<th>$C_{\text{gd}}$</th>
<th>$C_{\text{ds}}$</th>
<th>$C_{\text{gs}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mg: 1.5$\times 10^{12}$</td>
<td>247</td>
<td>386</td>
<td>750</td>
</tr>
<tr>
<td>C: 1.5$\times 10^{12}$</td>
<td>262</td>
<td>375</td>
<td>786</td>
</tr>
<tr>
<td>Mg: 3.0$\times 10^{12}$</td>
<td>236</td>
<td>450</td>
<td>984</td>
</tr>
<tr>
<td>C: 3.0$\times 10^{12}$</td>
<td>226</td>
<td>345</td>
<td>829</td>
</tr>
</tbody>
</table>
Fig. 7: $f_t$ and $f_{\text{max}}$ versus gate bias with VDS = 1.5 V for 0.5 μm x 100 μm self-aligned JFETs with low (1.5×10^{12} cm^{-2}) or high (3×10^{12} cm^{-2}) Mg or C p-backside implants. The DC performance of these devices is summarized in Table I and the extracted capacitances are listed in Table II.

self-aligned n$^+$ source/drain implants

The final implant step for the self-aligned GaAs JFET is the source and drain n$^+$-implant. Since the p$^+$-material is removed from these regions with an isotropic wet chemical etch, the refractory gate contact is slightly under cut as can be seen in Fig. 8. This under cut serves to space the n$^+$-implant away from the gate contact to act as a sidewall spacer. The n$^+$-implant is then performed using $^{29}$Si at a dose between 2 to 3×10^{13} cm^{-2} and is activated, along with all the other implants, in one RTA step. The RTA temperature has to be optimized to account for the conflicting requirement of a lower temperature to minimize diffusion of the p$^+$-gate region and the need for some what higher temperatures to achieve full donor activation as compared to acceptors (typically optimum activation temperatures are ~850 °C for Si donors and ~750 °C for most acceptors).

Fig. 8: SEM micrograph of a cross-section of a nominally 0.7 μm gate length JFET. The source and drain region have been etched down ~700 Å with an isotropic wet etch that also undercuts the tungsten gate contact and forms a T-shaped gate.
Self-aligned JFETs have been fabricated with implanted Mg, Zn, and Cd p⁺-gate regions. The effect of optimizing the p⁺-gate profile was first demonstrated by comparing Mg-gate to Zn-gate JFETs [3, 14, 18]. Figure 9 shows IDS and gm versus gate bias for nominally 0.7 μm x 50 μm Mg and Zn-gate JFETs. Although the threshold voltages of these devices are not identical, the Zn device is clearly superior. For a given voltage above threshold the Zn-JFET has higher current drive and higher transconductance. The enhanced performance is a result of the sharper p⁺-profile in the Zn device with less of the p-implant extending into the channel region. The high-frequency results discussed earlier along with the C-backside implant were also for a Zn-gate device with a 0.5 μm gate length. The high-frequency metrics of that device (f₁ = 28 GHz and fₘₐₓ = 43 GHz) are comparable to a GaAs MESFET of the same gate length while still achieving the higher gate turn-on voltage of the JFET (0.95 V for 1 mA/mm of gate current).

Figure 10 shows the DC performance of a 0.7 μm gate length Cd-gate JFET with a C-backside implant. The DC performance is comparable to a similar size Zn-gate JFET, however, a 26% increase in f₁ to 26 GHz and 11% increase in fₘₐₓ to 40 GHz over the Zn-gate JFET was measured. The high-frequency enhancement is not completely understood but may relate to the overall shallower doping profile in the Cd-JFET over the Zn-JFET.
Fig 10: DC performance of 0.7 μm x 50 μm Cd-gate JFET. (a) $I_D$ vs $V_D$ with $V_G$ starting at 1.0 V and stepping at -0.25 V. (b) $I_D$ and $g_m$ vs $V_G$ with $V_D = 1.5$ V. This device had a $f_t$ of 26 GHz and $f_{max}$ of 40 GHz.

CONCLUSION

Self-aligned GaAs JFETs have been developed that realize the higher gate turn-on voltage inherent to a JFET while still achieving excellent high-frequency performance comparable to a GaAs MESFET. The JFET structure employs extensive ion implantation process steps to produce a p+-gate, n-channel, p-backside, and n+ source and drain. The source and drain implant is self-aligned to the refractory gate contact to minimize excess gate capacitance typically associated with a JFET. The all implanted, self-aligned, JFET should find application in high-speed, low-power, circuit applications.

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