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Initial Experience with the CDF Layer 00 Silicon Detector

Christopher S. Hill *

University of California, Department of Physics, Santa Barbara CA 93106

Abstract

We report on initial experience with the CDF Layer 00 Detector. Layer 00 is an innovative, low-mass, silicon detector installed in CDF during the upgrade for Run 2A of the Tevatron. Noise pickup present during operation at CDF is discussed. An event-by-event pedestal correction implemented by CDF is presented. This off-line solution prevents L00 from being used in the current incarnation of the on-line displaced track trigger. Preliminary performance of Layer 00 is described.

Key words: Layer00, L00, CDF silicon

The Collider Detector at Fermilab (CDF) completed a major detector upgrade for the start of Run 2A of the Tevatron in March, 2001. The upgraded detector (CDFII) is described in detail elsewhere[1]. The baseline CDFII silicon system consists of 7 layers of double-sided silicon divided into two sub-systems, SVXII and ISL. In 1999, an innovative detector consisting of an additional single-sided layer of silicon built onto the beam-pipe was added to the upgrade. Since this detector is located radially inside layer 0 of SVXII, the sub-system is called layer 00 (L00).

L00 was added to the Run2A upgrade for two reasons. Firstly, to improve the impact resolution of the CDFII detector. SVXII readout electronics and associated cooling tubes are inside the tracking volume. Multiple scattering in this material degrades impact parameter resolution, especially for low-momentum particles. Placement of a minimal material silicon layer at a smaller radius provides a precise measurement which recovers this lost resolution. Secondly, L00 was installed to extend the useful lifetime of the silicon system. The inner layers of SVXII will have a limited lifetime due to radiation damage. Eventually, their double-sided sensors will no longer be depleted at the maximum

* For the CDF Collaboration.
Email address: chill@fnal.gov (Christopher S. Hill).

applicable bias voltage. L00 using single-sided radiation hard silicon can have significantly higher bias voltage applied and thus can compensate for radiation damaged layers of SVXII.

L00 is a single castellated layer providing full azimuthal coverage. The inner (128 strip) and outer (256 strip) sensors are located at radii of 1.35 cm and 1.62 cm respectively. The implant(readout) pitch is 25(50) μm. The sensors are mounted on a carbon-fiber support structure with integrated cooling. There are 12 sensors along the beam-line for a total length of 94 cm. Adjacent sensors are ganged together and readout over low-mass, fine-pitched cables. These cables allow the readout electronics to be located outside the tracking volume minimizing multiple-scattering from inactive material. The total number of channels readout in L00 is 13,824. The motivation, design, and construction of L00 are described in greater detail elsewhere[2].

Although Run2A of the Tevatron began March 2001, L00 commissioning did not begin until February 2002 due to a problem with its power supplies [1] . High voltage regulating MOSFETs were suffering single-event-burnout caused by proton losses from the Tevatron. When this transistor fails the detector sees the full 500V, and it cannot be shutoff through the normal interlock system. This problem was addressed by replacing these MOSFET transistors with a more radiation tolerant BJT type. In addition, a crowbar protection circuit was installed. Commissioning was completed May 2002. Greater then 95% of L00 has been consistently yielding physics quality data since that date.

Upon initial operation of L00 in CDF, significant noise was observed. This noise is characterized by a non-uniform pedestal shape across the 128(256) strips of a narrow(wide) sensor. The magnitude of the effect varies from event to event, and from module to module. The noise is determined to be pickup on the fine-pitched cables because effects are most pronounced at the edges of these cables as can be seen in Figure 1. Bench studies have been carried out to confirm these findings. A L00 module was placed in a well grounded Faraday cage. No pickup is seen in this environment. A wire carrying signals from a waveform generator was inserted as a noise source. Experiments were performed varying the amplitude, frequency, location, and shielding of the noise source. These tests confirmed that the cables are the antennae that pickup the noise. The tests also showed that the cables, which are stacked on top of each other, shield one another. Furthermore, these experiments demonstrated that a well grounded shield placed between the noise source and the analog signal cables eliminates the problem.

Examination of CDF data supports the conclusions drawn from the bench studies. It is confirmed that the location within the cable stack is important

[1] These power supplies are custom made for CDF by CAEN.

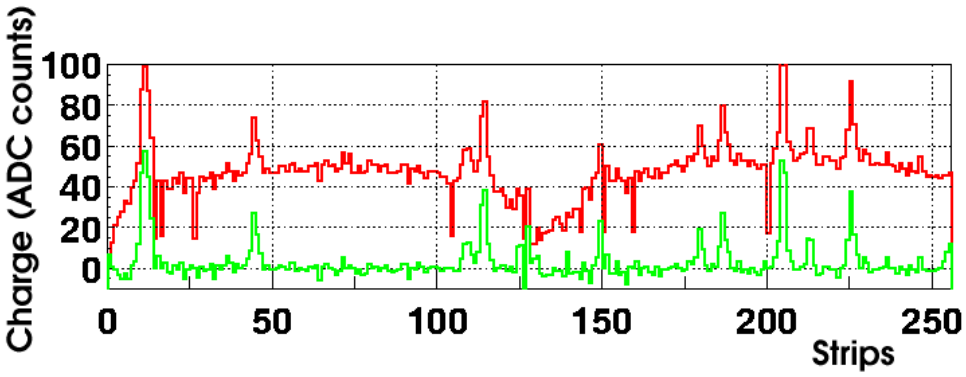

Fig. 1. This figures displays a sample physics event in a 256 strip L00 sensor. The raw charge as a function of strip number is plotted in red. Note the severe pickup near the edge of the cable (strip 128). Overlaid in green is the pedestal subtracted charge. The pedestal is determined by a χ^2 fit to Chebyshev polynomials.

due to the relative shielding that they provide. In the wide modules, the cables in the middle of the cable stack have the least pickup implying that there are noise sources above and below these cables. In the narrow modules, the innermost cable in the cable stack has the least pickup which indicates that the noise is coming from above these cables. Notably, this exonerates the beam-pipe and carbon-fiber support structure as the source of the noise. It is also observed that there is less pickup on the west than on the east. This is interesting since the L00 EMI shield's ground connection was made on the west.

The SVX3D readout chip has an internal circuit which dynamically subtracts the pedestal on an event-by-event basis[3]. This circuit assumes a flat pedestal, however, making it ineffective for the L00 noise problem. Instead, CDF employs an off-line event-by-event pedestal correction. The small channel count of the L00 detector allows all strips to be readout for every event. The charge on each strip is used to perform a χ^2 fit to Chebyshev polynomials for an event pedestal. The fit is performed first over all channels and then repeated excluding strips with charge above threshold. A sample physics event before and after fitted pedestal subtraction is displayed in Figure 1. This procedure was tested by embedding Monte-Carlo clusters in $p\bar{p}$ collision data and found to have a 95% efficiency with a 95% purity. It was also checked that no impact on cluster size or centroid resolution was introduced by the fitting procedure. CDF successfully introduced this operational solution prior to the completion of L00 commissioning. This solution has the consequence of preventing L00 from being used in the current incarnation of the on-line displaced track trigger (SVT). This conflict must be resolved for L00 to extend the useful lifetime of CDFII silicon as a triggering device. Additionally, the time to readout all channels of L00 limits the L1 trigger rate to $\sim 30\ kHz$, which will become an

issue as Tevatron luminosity increases [2] .

After the event pedestal described above is subtracted an average signal-to-noise ratio of 10:1 is obtained for hits in L00. This was the design goal and is sufficient for operation. Nevertheless, the signal charge is less than that expected because the clustering algorithm has not yet been optimized for L00. The data collected so far have been used to perform a global alignment of the L00 detector. Offsets of 200 μm in x,y and a rotation of 1 degree were found and corrected. These mis-alignments are consistent with the expected installation precision. After global alignment a hit efficiency of 85% is measured. Analysis of tracks through L00 have revealed mis-alignments of the drift chamber (COT) and the other silicon sub-systems (SVXII+ISL). A precsion alignment of L00 awaits the re-alignement of the COT+ISL+SVXII. Without a precision alignment, the effect of L00 on IP resolution is obscured. Nonetheless, analysis of low p_T tracks whose resolution is dominantly determined by multiple-scattering effects can show the impact of L00. Indeed, a correlation between the unbiased residual to the L00 intersection point and measured IP is found. This correlation shows these tracks are not truly displaced from the interatcion point and attachment of L00 hits will correct this mis-measurement.

Layer 00 is an innovative silicon detector that has been successfully built, installed, and commissioned in CDF with 95% of the detector producing physics quality data since May 2002. Noise on the analog signal cables is present during operation at CDF. The problem is solved operationally with an event-by-event pedestal fit peformed off-line. First results obtained with L00 data are encouraging. A signal-to-noise of 10:1 with an efficiency of 85% is acheived. A preliminary alignment of L00 has been performed. Evidence that L00 will improve IP resolution in CDF when the precision alignment is complete was presented. It is expected that the physics impact of L00 will soon be demonstrated.

References

[1] CDFII Collaboration "Technical Design Report," *FERMILAB-PUB-96/390-E.*

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[3] M. Garcia-Sciveres et al, "The SVX3D Integrated Circuit for Dead-timeless Silicon Strip Readout," Nucl.Instrum.Meth.A435:58-64,1999.

[2] The design goal of CDFII is a L1 trigger rate of 50 kHz.