DOE/ER/82953-1

Project Title:

**Wire-Shaped Semiconductor Light-Emitting Diodes
for General-Purpose Lighting**

**US Department of Energy
Phase I SBIR Award**

DE-FG02-00ER82953

Phase I Contract Period: 02 Sep 2000 to 01 March 2001

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Executive Summary

The proposed SBIR Phase II program seeks to continue development and optimization of a new type of light-emitting diode (LED) with a wire-shaped, cylindrical geometry. The intended application is for low-cost, high-efficiency general-purpose lighting, and the ultimate objective is the long-anticipated realization of a solid-state lighting replacement for fluorescent bulbs and incandescent lamps. A generic design and fabrication process is under development that will be applicable to a number of compound semiconductors; including AlGaAs, InGaP, AlGaInP, ZnSe, and GaN and its related alloys; and therefore, emission wavelengths (colors) over the entire visible spectrum can be achieved. Combinations of diodes; or alternatively, a blue-emitting diode with a phosphor, can produce "white" light needed for interior and exterior lighting of commercial and residential buildings.

The wire-shaped LED is made by forming semiconductor cladding layers on a wire or filamentary substrate. As a specific example, a 10- to 20-micron thick cladding layer of GaN is grown on an electrically-conducting graphite or SiC fiber. The "wire substrate" serves as one lead of the diode. A p - n junction is formed over the surface of the cladding layer and is contacted by selectively-applied metallization to form the other lead of the diode. Refractory metals or coated silica or silicon nitride fibers are also feasible as wire substrates. The wire-shaped LEDs can be made by a several liquid- and vapor-phase deposition and crystal growth methods. Further, GaAs, AlGaAs, InGaP, and GaN-related alloys can also be deposited as cladding layers. GaN is of particular interest, however, because of its potential as a general-purpose high-performance LED and due to its remarkable insensitivity to defects and grain boundaries. Thus, this fortuitous situation makes GaN one of the most promising candidates for application to wire-shaped LEDs.

There are several motivations for this approach: The external optical coupling efficiency in a cylindrical geometry can be very high. This may be contrasted with conventional die-based LEDs where the optical coupling losses and parasitic absorption limit the external efficiency of the LED to around 5 to 20%. We believe the wire-shaped configuration can lead to a three- or four-fold improvement in LED performance due to better optical coupling of the electroluminescence. Secondly, the wire-shaped geometry eliminates the need for expensive semiconductor wafers. We also contend that higher throughput deposition processes are possible with fiber coating due to more favorable heat and mass transfer and amelioration of stress effects in fiber geometries compared to thin film deposition on wafer substrates.

The Phase I work surveyed and experimentally assessed a number of techniques for producing these wire-shaped LEDs, including melt coating, chemical vapor deposition, recrystallization by traveling infrared zone melting or in-situ resistive heating, diffusion, and in-situ oxidation. In some cases, a recrystallized seeding layer of silicon or germanium (with grain sizes up to 500 microns) is first formed on the wire substrate prior to CVD or solution growth of the compound semiconductor cladding layers. These were used to seed the subsequent epitaxial growth of GaAs in a separate CVD step. The feasibility of the proposed approach was demonstrated by the realization of a GaAs LED on a graphite fiber. Obviously, much work remains in order to improve the efficiency of this new generation of light-emitting diodes. This Phase II proposal outlines a path for the continued research, development, demonstration, and optimization of wire-shaped light-emitting diodes for general-purpose lighting.

I. SIGNIFICANCE, BACKGROUND INFORMATION, AND TECHNICAL APPROACH

1. Identification and Significance of the Opportunity and Technical Approach

Improvements in the efficiency of general-purpose lighting can lead to significant reductions in electricity usage for the United States. It is estimated that about 20% of all electrical power is used for lighting. Therefore, a doubling in lighting efficiency—defined as lumens output per watt of electrical power supplied—would lower electricity consumption by roughly 10%. In addition, the worldwide economic benefits could amount to a savings of \$100 billion per year with an approximate 200-million ton reduction in annual carbon emissions [HAITZ *et al.*, 1999]. There is a wide consensus that lighting efficiency improvements of a factor of two to four over conventional lighting are now feasible. A more in-depth discussion of the potential benefits of efficient general-purpose lighting is presented in section x.x.

Semiconductor electroluminescent devices, and most prominently the *light-emitting diode* (LED), have long held promise as successors for fluorescent lights and incandescent lamps. In the last decade, developments in semiconductor materials technology, especially with regard to the III-V compound nitrides and phosphides, have spurred renewed efforts in LEDs. The proposed SBIR program seeks to explore, assess, and develop a new generation of light-emitting diodes (LEDs) based on a cylindrical geometry (see FIGURE 1) such that the luminescent semiconductor components are formed as cladding layers around a filamentous or wire substrate. These wire-based LEDs are designed for dramatic increases in efficiency, as well as improved compatibility with low-cost, high-throughput manufacturing. In addition, their wire shape is conducive to retrofitting exterior and interior lighting fixtures in residential, commercial and industrial buildings and facilities, and also for street lighting, outdoor advertisement displays, and greenhouses. This is an important consideration if LEDs are to make significant and timely inroads into these applications.

FIGURE 1: Simplified schematic of a wire-based light-emitting diode (external reflector not shown).

We are developing a generic materials technology that will be applicable to a wide-range of semiconductors such as GaAs, AlGaAs, GaN, and AlGaInP, and thus span the entire visible region of the spectrum. The main focus on the experimental effort has been to demonstrate methods of forming semiconductor coatings of sufficiently large grain size on a variety of wires or filaments using both liquid-phase and vapor-phase methods of crystallization. The main motivation of the cylindrical geometry is due to its inherent high light extraction efficiency compared to wafer-based LEDs, thus providing much enhanced performance. The cylindrical geometry also has advantages related material yield, recrystallization, and stress reduction.

1.1 Introduction and Overview

The purpose of this work is to develop a completely new technology for solid-state lighting based on a cylindrical geometry, wire-substrate LED design applied to a number of well developed semiconductors materials. We believe such an approach is warranted if drastic cost reductions are to be realized for large-scale applications such as general-purpose lighting. Further, these new designs offer features for much improved performance since light coupling can be greatly enhanced in this geometry. Contemporary LED designs using a wafer-based die suffer from severe optical coupling losses that can be overcome with the cylindrical geometry design proposed here. We intend to assess the feasibility of this approach by experimentally demonstrating and fully characterizing device prototypes in several semiconductors with characteristic emission wavelengths in the red, yellow/green, and blue regions of the visible spectrum.

Presently, almost all semiconductor devices are made in a planar topology using wafers cut from bulk crystals, or in epitaxial structures formed on wafer substrates. We are proposing a new paradigm where semiconductor structures are manufactured in a cylindrical configuration with a filament or "wire substrate" form (see FIGURE 2). This approach has some unique and significant advantages which will be discussed shortly. Details of the connections, i.e., ohmic contact metallizations—which are not indicated in FIGURE 2—will also be described. The choice between a filament or wire substrate approach depends on the semiconductor material and the device application. More sophisticated multilayer structures are also feasible.

FIGURE 2: LED device topologies (Contacts not shown).

The structure shown in FIGURE 2a is typical of conventional LEDs. A multilayer device is formed by several diffusions, ion implantations, or epitaxial growth steps on a single-crystal (or sometimes polycrystalline) substrate wafer. There are several methods of fabricating the structures shown in FIGURES 2b and 2c. For the filament structures (FIGURE 2b), semiconductor rods can be grown from the melt or vapor phase. For instance, RIEMANN [1996] reported the die-free growth of monocrystalline silicon rods with diameters of 300 microns at pull rates of 2.5 cm/min. Alternatively, FRANZOSI *et al.* [1977] described the growth of single-crystal silicon rods with a CVD (chemical vapor deposition) process. The junction shown in FIGURE 2b can be formed by post-growth diffusion.

The wire-substrate embodiment of an LED (FIGURE 2c) can be realized in several ways. The wire has the advantage of serving as one ohmic contact to the device. The wire must be metallurgical compatible with the process used to coat it with semiconductor layers. Several promising wire materials include carbon fibers, SiC fibers, refractory metals, or metals coated with SiC. The fiber is coated with a ten- to several hundred-micron thick cladding layer of semiconductor material using either a chemical vapor deposition or solution growth process. The wire can also be coated with a sheathing layer of germanium and silicon, by solidification after the fiber is coated with the molten semiconductor. Silicon and germanium are not in themselves useful for light-emitting diodes, since they both have poor luminescence properties, but silicon and germanium sheaths can be utilized as seeding layers for subsequent deposition of compound semiconductor layer(s) such as GaN and AlGaInP. The logic of a Ge or Si "seeding layer" approach will be explained shortly.

A major part of the Phase I effort has been to experimentally determine the best of several approaches to accomplish this. We anticipate that the best approach will be specific to the particular semiconductor and fiber. Ideally, the semiconductor layers will have large-grain crystalline material with grains oriented along the length of the fiber. In the case of silicon and germanium, a recrystallization step to increase grain size will likely prove advantageous. A Ge-coated fiber can be used as a "substrate" for epitaxial growth of an AlGaAs/ GaAs device. Similarly, a wire coated with a large-grain sheathing layer of silicon can be used as a substrate for GaN epitaxy. Junctions can be formed by multiple growth steps or diffusion. The fabrication technology is discussed in more detail in subsequent sections. Schemes for contacting the outer layer of the p - n junction will also be described. Some new developments in transparent conductive oxides may be useful in this regard.

A specific implementation of the wire substrate LED, which indicates the increased light coupling expected in a cylindrical geometry, is shown in FIGURE 3. The wire serves as one lead to the device. A second lead to the outer layer of the p - n junction can be made by a wire bond, or a more elegant technique. The LED rod is placed in a reflective package as is commonly done with many commercial LEDs. A critical advantage of the cylindrical LED is its potential for high coupling efficiency. Typically, in planar LEDs such as shown in FIGURE 2a, only about 5% of the luminescence is externally coupled out of the device. The rest is parasitically absorbed (mostly in the substrate) through internal reflections. This is because the radiative emission is isotropic, and the escape cone solid angle to avoid totally internal reflection in materials with high refractive indexes, such as semiconductors, is less than 20° . As can be seen in FIGURE 3b, the cylindrical geometry will give very high optical output coupling efficiencies. Well over 50% should be possible at minimum, but if the wire-substrate / semiconductor interface is reflective, even higher coupling efficiencies will be achievable.

FIGURE 3: Wire-substrate LED in a reflective mirror housing : a. perspective view, b. cross-section with a few representative ray tracings for injection luminescence escaping the LED. Much higher coupling efficiencies ($> 50\%$) will be possible compared to planar LEDs (FIGURE 2a) where coupling efficiencies are typically about 5%. The cylindrical wire LED will potentially be much brighter than commercial LEDs.

FIGURE 3 shows an array of LEDs mounted in a reflective backing receptacle intended for large-area illumination. In this case, each wire-shaped LED can be connected in series to utilize a higher drive voltage and lower drive current. This will lower resistive losses and can simplify the rectifier electronics needed to interface LED lighting with utility supplied alternating current. FIGURE 4 shows a scheme where the LED filaments are placed on a reflective sheet such as a metal foil and covered with a textured, transparent encapsulant. The optical coupling due to diffuse scattering and internal reflection is suggested in some representative ray tracings. This device is discussed in more detail in section 2. In such a case, the backing sheet is flexible and the LED array can be rolled up for shipping and deployed as a ceiling or wall covering in a variety of architectural uses.

Figure 3: Wire-substrate LED array. The LED filaments have an exterior contact and are connected in series to use a higher supply voltage and lower current.

FIGURE 4: Light trapping in cylindrical solar cells with back reflector and textured encapsulant.

Much of the technology developed here could be applied with appropriate modifications to wire-shaped solar cells. Conversely, many of the techniques used to manufacture solar cell modules can be used for the wire-shaped LEDs proposed here. This is an important consideration, since until now, solar cells are the only semiconductor device that is produced in areas comparable to that which will be needed for general-purpose lighting. Thus, there is much incentive to develop an LED technology that can exploit the established infrastructure of the solar cell industry. As the largest US-owned manufacturer of solar cells, AstroPower produces $4 \times 10^4 \text{ m}^2$ of solar cells per month and is well positioned to apply the know-how in solar cell and module fabrication to the wire-shaped LEDs described in this proposal.

1.2 Background

The motivation for and potential impact of low-cost, high-efficiency solid-state lighting are no doubt familiar to a wide technical audience. A brief introduction to the current status of light-emitting diodes appears in the February 2001 issue of *Scientific American* (CRAFORD *et al.*, 2001, "In Pursuit of the Ultimate Lamp"). An informal survey of commercially available LEDs can be found at <http://ledmuseum.home.att.net>. More detailed technical discussions of specific devices are compiled in volume 48 of *Semiconductors and Semimetals*, R.K. WILLARDSON and E.R. WEBER [1996], eds., "High Brightness Light Emitting Diodes". Current news and industry trends about LEDs appear regularly in *Compound Semiconductor* magazine and the March 2000 issue features main articles on light-emitting diodes. As support for the relevance and motivation of the work proposed in this SBIR application, we could do little to improve upon the discussion by R. HAITZ, F. KISH, J. TSAO, and J. NELSON "The Case for a National Research Program on Semiconductor Lighting" (available by e-mail request from bikazmi@sandia.gov or can be forwarded by sending e-mail to mauk@astropower.com). WHITTAKER [2001] emphasizes several challenges facing LED developers in response to the needs of the lighting industry and these include: 1. enhanced efficiency, 2. larger, shaped dies, 3. improved thermal management, 4. a factor of ten reduction in cost, and 5. reduced packaging requirements. We believe we can make a strong case that the proposed wire-shaped LED design and the methods we have developed to fabricate such devices will successfully address these issues.

As already mentioned, almost all semiconductor electronic and optical devices including LEDs are based on the use of a substrate wafer and "planar process" technology where the starting point of device fabrication is a thin disc of semiconductor material (called the *wafer* or *substrate*) sliced from a single-crystal boule. (In the case of solar cells, the wafers are often cut from a polycrystalline ingot.) The device structure is then built up by some combination of thin-film epitaxial growth processes, impurity diffusions, ion implantations, oxidations, metallizations, photolithographic patterning, and etching steps. Organic LEDs and thin-film display technologies generally forego the semiconductor substrate, but much of the fabrication technology is similar to that used in the integrated circuit industry.

In optoelectronics, there have been few deviations from the planar wafer topology approach which has typified the 50-year history of semiconductor technology. There is, of course, the burgeoning field of nanotechnology (quantum dots, quantum wires, porous silicon, nanocrystals, and nanotubes) and MEMS; but their practical applications for lighting and energy conversion are generally not expected in the near term.

To provide some perspective and background to the proposed work, FIGURE 5 shows some of the novel device geometries that have been proposed over the years for various applications including solar cells, microelectronic circuits, and light-emitting diodes. FIGURE 5a represents the wafer-based semiconductor topology that serves as the basis of the microelectronics, solar cell, and optoelectronics industries. FIGURE 5b shows a solid rod of semiconductor. A 1961 patent by HENKER describes the use of such rods for photodetectors. Some work was reported in the 1970s [JOHNSON *et al.*, 1977] on using 2- to 4-mm diameter silicon rods (with wrap-around diffused junctions) as solar cells with trough-type reflectors in solar concentrator systems. FIGURE 5c is the wire-shaped LED which is the subject of this proposal. FIGURE 5d is a hollow tube of silicon which can be grown by die-shaped crystal pulling. MLAVSKY patented a tubular solar cell based on such structures in 1976. FIGURE 5e is a 1-mm silicon sphere. A company called Ball Semiconductor, Inc. (Allen, Texas;

www.ballsemi.com) is developing working transistors and small-scale integrated circuits defined on the surfaces of 1-mm diameter single-crystal silicon spheres [LINEBACK, 1999]. This spherical geometry has a long pedigree at Texas Instruments. Spherical silicon was proposed by Jack Kilby (the Nobel Prize winner and co-inventor of the integrated circuit) as a photoelectrochemical device for solar generation of power in the early 1970s—for a review, see for example, A.J. BARD, "Photoelectrochemistry and Solar Energy: Progress, Promise and Problems" *J. Analytical Chemistry* 168, (1984) 5. Subsequently, Texas Instruments developed a Spherical Solar™ solar cell which consisted of an array of diffused silicon balls mounted in a perforated aluminum sheet [LEVINE *et al.*, 1991]. Texas Instruments has abandoned this process. It was sold to Ontario Hydro who are presently trying to sell or license the process, but doubts to its commercialization remain (*Photovoltaic Insider's Report*, June 1997). In formulating the approach proposed in this Phase I program, we addressed the limitations of the Spherical Solar™ solar cell—such as problems associated with sizing, handling, and processing small (~400 micron diameter) spheres, interconnecting spheres, and avoiding shunts—while still retaining its favorable features—elimination of wafer sawing, amenable to impurity gettering, and favorable light trapping.

Discrete crystals formed on a substrate (as suggested in FIGURES 5d and 5e) have some potentially interesting features, although the electrical contacting and interconnections is problematic. Figure 5d is the result of heterogeneous nucleation and unimpinging growth on a substrate. The type of structures shown in FIGURE 5e can be made by a fluidics self-assembly process: small crystals are separated from a silicon wafer by patterning and etch undercutting, they are then suspended in a liquid that is flowed over the surface of a plastic substrate whereupon they are sited in indentations embossed into a plastic substrate. To round out the survey, Figure 5i shows a device configuration comprised of small semiconductor spheres imbedded in a dielectric matrix. Such structures have interesting optical properties but have been difficult to utilize in electrical devices. Finally, FIGURE 5j shows an "epi-lift" structure proposed as a solar cell by BLAKERS [1996] of the Australian National University and made by selective liquid-phase epitaxy on a grid-patterned substrate. The epitaxially-grown part is separated from the substrate to yield a free-standing, wire-frame or mesh semiconductor structure.

A recent development in cylindrical-geometry solar cells is a CuInSe₂ "filament" solar cell proposed by the Daystar Company (Denver, CO) that may have some similarities to the wire LEDs proposed here. Not much has been reported on this cell and we do not know enough details to comment or compare, although there are some indications Daystar uses a rectangular metal ribbon substrate to deposit CuInSe₂ solar cells in the form of narrow strips.

As the foregoing suggests, there has certainly been some thoughts and efforts devoted to semiconductor device topologies which fall outside the wafer paradigm. Nevertheless, it is striking that practically none of this work has been yet applied to light-emitting diodes. Many of the features touted in this approaches can be profitably applied to light-emitting diodes. We believe that while several of the device geometries shown in FIGURE 5 are interesting for light-emitting diodes, the wire-substrate geometry (FIGURE 5c) has the most compelling advantages for high performance and low-cost manufacturing.

a. wafer-based devices

b. semiconductor rod

c. wire-substrate LED

d. silicon tubes

e. silicon sphere (1-mm diameter)

f. Spherical silicon™ solar cell array

g. discrete crystals formed on a substrate

h. fluidic self-assembly of discrete crystals

i. semiconductor spheres embedded in a dielectric matrix

j. epilift structure From BLAKERS [1996].

Figure 5: A pictorial survey of some novel device topologies (see text for more discussion).

2. Technical Approach

Overview

Fortunately, there is a wide range of options for fabricating the wire-substrate cylindrical light-emitting diodes described above. Our basic concept is to coat an electrically conducting fiber, such as made of SiC, carbon (graphite), or a refractory metal such as tungsten or tantalum. A non-conducting fiber, such as made of silica (SiO_2) or silicon nitride (Si_3N_4) is also workable but is not the first choice since the device design is simplified if the wire substrate is conducting and can function as a contact and lead of the diode. One option is to deposit the light-emitting diode compound semiconductor layer(s) directly on the fiber using chemical vapor deposition. This is feasible, but the average grain size of the deposited semiconductor cladding layer is generally small (~ 10 microns) which in some materials may preclude efficient operation due to excessive non-radiative minority carrier recombination and high shunting paths at the grain boundaries. Instead, we first deposit a seeding layer of silicon or germanium directly on the fiber. Neither of these materials are suitable for light-emitting diodes since they exhibit relatively low room-temperature luminescence. However, they can be deposited on the fiber by a number of techniques including melt coating, CVD, or metallic solution growth (similar to liquid-phase epitaxy). And they can function as seeding layers for the subsequent epitaxial growth of the luminescent structure of the LED. Ge has a close lattice match to GaAs, $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$, $\text{Al}_x\text{Ga}_{1-x}\text{As}$, ZnSe, and a range of AlGaInP alloys. Silicon has a good lattice match to GaP, ZnS, and AlGaP. Although far from lattice matched, silicon can also be used to seed the epitaxial growth of GaN and related ternary alloys. Perhaps the most important attribute of silicon and germanium is that they can be readily recrystallized. The as-deposited, small-grain (10 to 20 micron) silicon and germanium cladding layers are annealed or melted on the fiber by passing the fiber through a heated zone of an infrared furnace. Multiple passes produces very elongated grains with their largest dimension oriented along the axis of the fiber. The silicon cladding layer can be encapsulated with a (~ 200 -nm thick) thermal oxide to maintain good wetting and adhesion of silicon to the fiber and prevent coalescence or "balling up" when in the molten state. Large grains, in the millimeter size range, can be achieved by such recrystallization. The literature reports practically single-crystal cladding layers for such recrystallization or annealing processes when applied to refractory metals and metal silicides and carbides [SCHAEFER, 1964]. (We should mention that similar recrystallization of compound semiconductors is generally unworkable due to the incongruent melting and high volatility of components.) After a large-grain silicon or germanium cladding layer is attained on the wire substrate, the structure is used in a CVD or solution growth process to grow several more cladding layers of a compound semiconductor such as GaAs or GaN. These compound semiconductor layers comprise the active, i.e., light-emitting, components of the device. A p - n junction is formed either between two compound semiconductor layers of opposite conductivity type, or by a post-growth impurity diffusion process. With this outline of the technical approach, implementations with specific materials can now be discussed.

AlGaAs and GaAs Wire-Substrate LEDs

A schematic cross-section (not to scale) of the wire-substrate double heterostructure AlGaAs/GaAs LED is shown in FIGURE 6. This particular design is meant to suggest one possible implementation; other variations are possible. The thick wide-bandgap AlGaAs outer cladding layer is contacted by wire bonding (not shown), or indirectly by coating with a conductive transparent oxide. This layer is thick (> 10 microns) in order to avoid punch through

or shunting during the metallization. A heterojunction is formed between the outer cladding layer and an oppositely doped base or luminescent layer. An optional inner cladding layer provides carrier confinement as is typically done in planar heterojunction LEDs. The AlGaAs layers are formed on a germanium seeding layer, the purpose of which is described shortly. The wire is also a back contact.

Figure 6: Schematic cross-section of AlGaAs wire substrate LED (not to scale).

The structure of FIGURE 6 can be made in several ways. We briefly describe one approach, but this is suggestive and should not be misconstrued as the definitive technique. We start with a narrow gauge wire of a refractory metal (tungsten, molybdenum), or a carbon (graphite) or SiC fiber. The wire is coated with a germanium layer. This can be done by CVD or by pulling the wire through molten germanium (melting point = 937 °C). The Ge coating can be recrystallized by slowly heating one end of the wire and passing a molten zone along the length of the wire. For CVD, the coating of wires with polycrystalline layers is, in fact, a very old technique: the analogous van Arkel / Boer process, developed for zirconium and other metals, dates from the early years of this century. Based on experience with other materials, and in addition to germanium and silicon [SCHÄFER, 1964], quite large (~1 mm or greater) grain sizes can be achieved. With a zone pass technique, even single crystal layers are possible. Evidently, surface energy effects with this geometry are very favorable for achieving long oriented grains along the length of the wire. The recrystallized Ge coating serves as a seeding layer for multiple layer growth of AlGaAs. This can be done by CVD or by passing the wires through arsenic-supersaturated Al-Ga metallic solutions similar to those used in conventional liquid-phase epitaxy. Many fibers can be coated simultaneously.

GaN Wire-Shaped LEDs

GaN can be deposited directly on fibers. In this case, a recrystallized silicon or germanium seeding layer may not be necessary because GaN light-emitting diodes may be able to tolerate relatively small-grains (~10 microns) and still exhibit good luminescence. A surprising feature of GaN is the demonstration of high performance LEDs in material with defect densities exceeding 10^8 cm^{-2} and which shows a mosaic structure indicative of many low-angle grain boundaries. GaN is a hexagonal crystal structure, in contrast to the other semiconductors cited here which are cubic (diamond and zinc blende). Consequently, we observe a tendency for GaN to grow on a fiber with its *c* axis oriented along the axis of the fiber (FIGURE 7). Thus, in the case of GaN there appears to be an oriented texturing effect for the crystal growth process. Thus, for wire-shaped LEDs GaN must be considered the prime candidate on several counts: 1. its high radiative efficiency at blue wavelengths, 2. its tendency for oriented growth along the fiber, and 3., its tolerance of high defects and grain boundaries.

FIGURE 7: a. crystallographic facets of hexagonal GaN, and b. oriented growth and fibrous texture along the axis of the wire substrate.

Two methods of depositing the GaN are utilized in this work. In the first, the GaN is deposited by a chemical vapor-transport technique using GaN powder as the source material and ammonia as the transport agent. In the second method, GaN is formed by coating the fiber with a thin layer of molten gallium, which is converted to GaN by prolonged annealing in ammonia.

Silicon-Coated Wire-Substrates for GaN and Other III-V Compound LEDs

The silicon-coated wire substrate is similar to the germanium-coated substrate described above. A schematic cross-section is shown in FIGURE 8. In this case, a graphite or silicon carbide fiber is coated with a thin layer of molten silicon. This coating can be recrystallized to achieve larger grain sizes. The fiber is then used to seed the epitaxial growth of a compound semiconductor: GaN, InGaN, GaP, or ZnS. A thick wide-bandgap emitter/cladding layer is then grown to form a *p-n* junction. The fiber is then placed on an aluminum sheet and alloyed to make ohmic contact to the emitter. The emitter layer can be thinned if necessary using wet etches, plasma etches, or anodizations. This may be necessary, as initially a thick emitter is preferred to avoid punch through when alloying to the aluminum sheet. Helpful recent developments are low-temperature surface passivation techniques, such as plasma-enhanced chemical vapor deposition of silicon oxynitride, to reduce minority carrier surface recombination velocities.

Figure 8: Schematic cross-section of silicon-coated wire substrate with a compound semiconductor LED (not to scale). The contacts are through the wire substrate and aluminum sheet.

Figure 9: Schematic cross-section of LED array. The structure of each LED component is the same shown in Figure 8.

FIGURE 9 shows multiple wire-substrate LEDs assembled in a parallel array. We anticipate some improved optical coupling due to the reflectivity of the aluminum sheet. The array of wire-substrate cells could be encapsulated with a silica glass. The textured (i.e., wavy) front surface is also good for optical coupling. Better yet would be a conducting oxide encapsulant. We show an optional anodically grown oxide on the aluminum sheet to prevent shorting. This design should show very low series resistance since the emitter is contacted by the aluminum along the length of the wire. When finished, it may be possible to roll the sheet up (with the axis of the roll parallel to the wires). This would greatly facilitate shipping and storage of the modules. During the course of the Phase II work, other design improvements will be investigated.

The wire substrate is one contact. The wires will protrude from the ends of the array. Normally, the wires can be tied together to connect cells in parallel. By scribing or cutting grooves as shown in FIGURE 9, groups of cells can be electrically isolated. At this point, the wires can be connected to the aluminum sheet of adjacent cells for a series interconnection. In this way, a high-voltage module could be realized. Other series interconnection schemes are undoubtedly possible.

A natural question is whether the wire material (carbon, SiC, or a refractory metal) will contaminate the semiconductor coating layers. In the case of carbon and silicon carbide fibers we mention previous work where molten silicon was solidified on carbon or SiC substrates, such as in the S-web or carbon net process [FALKEBERG *et al.*, 1987]. Solar cells of about 15% efficiency have been made from silicon solidified in contact with graphite. In many of these cases an interfacial layer of SiC is formed between the graphite and silicon. This SiC layer is thought to be beneficial. At any rate, clearly, there are good candidate materials for the wire substrate. Metal wire substrates could be made workable by first coating them with carbon or silicon carbide.

3. Anticipated Benefits

The primary performance benefit of the proposed approach is related to its potential for high efficiencies through much enhanced optical coupling efficiencies. The total overall efficiency η_{tot} of an LED is determined as the product of three factors

$$\eta_{tot} = \eta_{inj} \cdot \eta_{rad} \cdot \eta_{coup}$$

where η_{inj} is the injection efficiency which is the fraction of current comprised of injected minority carriers into the quasi-neutral region(s) of the luminescent layer(s) of the LED; η_{rad} is the radiative efficiency which is a measure of the fraction of injected minority carriers that recombine radiatively (as opposed to non-radiatively through defect-, surface-, or impurity-mediated recombination), and η_{coup} is the coupling efficiency which indicates the fraction of luminescent photons generated by radiative recombination that escape through the external surfaces of the LED. In many compound semiconductor heterojunctions, the injection and radiative efficiencies are quite high, often approaching 100%. The coupling efficiency, on the other hand, normally limits the total efficiency. Coupling efficiencies of 2 to 10% are not uncommon in commercial LEDs. The low coupling efficiency is a consequence of the anisotropic nature of luminescence, the high refractive index of the semiconductors, and the geometry of the LED (FIGURE 10a). In a planar LED, only a small fraction of the luminescence falls within the escape cone for transmission through the front surface, i.e., light which is internally incident upon the surface at an angle greater than about 15° is internally reflected, where it is lost in multiple internal reflections and parasitic absorption in the substrates and contacts. Transparent (wide bandgap) substrates, reflecting layers between the substrate and epitaxial layers, surface texturing and structuring, and shaping of the die have all served to improve coupling efficiency but have been either limited in effect or too costly to justify.

FIGURE 10: Comparison of conventional light emission in conventional LED die (a); in wire-shaped LED (b), and direct geometric comparisons of acceptance angle and loss cones in planar front surface LED and cylindrical LED (c).

Provided the thickness of the cladding layer and substrate wire are optimized, the coupling efficiency of the wire-shaped LED can be much higher than in an LED die. The wire-shaped LED has a much wider acceptance cone for transmission through the front surface. The use of a wire made of reflecting material or of a reflective coating between the cladding layer and wire, such as by a quarter-wavelength stack of oxides formed by anodic oxidation, can improve the coupling efficiency. Also, the inclusion of wide bandgap transparent cladding layers permits more latitude in spacing the layers and thicknesses for optical coupling. Our ray tracing computer modeling program indicates coupling efficiencies of 50 to 78% (depending on reflectance of the wire substrate) are possible with optimized layer thicknesses and core diameters.

Other Potential Technical and Manufacturing Advantages of Wire-Shaped LEDs

We anticipate the following advantages using this approach:

1. The wire or filament topology eliminates the need for crystal pulling of large boules, wafer sawing and kerf loss, and wafer polishing. There is no material loss in the wire process.
2. Wires can be coated with semiconductor layers in high-throughput, continuous deposition processes. Many wires can be pulled through in parallel and simultaneously coated. There is a well established technology base for growing and processing oxide, metal, and ceramic fibers.
3. Thermal stress effects are less pronounced in fibers than sheets, therefore faster cooling rates can be tolerated which will permit high throughput processes without excessive generation of stress-induced defects.
4. High-temperature processing could be achieved by simply passing an electric current through the wire for Joule heating. This could be used in crystallization, deposition, and annealing steps to save energy. It also suggests a van Arkel-Boer "hot wire" CVD process.
5. Unlike the Spheral Solar™ approach, sizing of the fibers is not critical.
6. The process is fault tolerant. Wire devices can be easily tested in-situ or before moduling. Filaments in an array which are dead or shorted can be left unwired. Selective anodization of shorted regions of fibers can also be used to correct shunts. This technique was used successfully in the Spheral Silicon™ process.
7. The filaments are compatible with most standard semiconductor processes (diffusion, oxidation, rapid thermal annealing, anodization, hydrogenation and grain boundary passivation, or plasma and wet etching).
8. Parallel and series connection is facilitated to achieve high-voltage arrays. The wire substrates can be interconnected according to performance to achieve better current matching than is possible with wafer-based cells.
9. The high surface-to-volume ratio should make the filaments more amenable to impurity gettering steps. Further, growth could be effected in stages with intermittent gettering steps, thus permitting removal of deep lying or slow diffusing impurities. Thus, lower purity starting materials could be tolerated.
10. Flexible or roll-up arrays should be possible.
11. The wire-substrate devices lend themselves to highly automated assembly into modules. The packaging LED arrays is actually one of the biggest cost components of these technologies. We believe wires will be easier to assemble and package than either die or wafers. Presently much of this labor intensive work is done overseas to take advantage of low labor costs. The cost advantage of our approach will be due to engineering and automation, which should give U.S. producers an advantage over the low-wage countries which presently dominate the LED assembly business.
12. Much of the technology developed here for LEDs could be adapted for low-cost solar cells.

Economic and Social Benefits

The economic and social benefits of more-energy-efficient lighting are clear and substantial. At the time the Phase I proposal was submitted, electricity was not a topic of high concern for the average American. In the last year, the California electric power crisis and its impending spread throughout the rest of the country has brought the issue of conservation and more efficient utilization of the electricity to the forefront. It was reported in late March that California electricity rates will increase by about 46% in the next several months. Economic growth and the maintenance and improvement of living standards will depend on the success of innovations of energy conversion and utilization. The potential impact of light-emitting diodes is shown in TABLE 1 from HAITZ *et al.*, "The Case for a National Research Program on Semiconductor Lighting"

Table 1: Projected Global Savings in Energy, Energy Cost, and Energy Generating Capacity as a function of LED penetration with LED efficiencies of 50 lm/W.

	Year	2005	2010	2015	2020	2025
LED penetration	%	0.05	0.5	4	9	10
Energy Savings per Year	TWh/yr	1	18	150	370	440
Energy Cost Savings per Year	M\$/yr	100	1,800	15,000	37,000	44,000
Energy Generating Capacity Saved	GW	0.1	2	17	42	50

As one of the world's largest suppliers of solar cells and photovoltaic systems, AstroPower would be in a truly unique position with the introduction of high-performance light-emitting diodes developed under this SBIR. Currently, the company is involved in manufacturing, distributing, and implementing complete residential photovoltaic power systems in California, both in retrofitting existing homes and in new housing starts. The company is directly involved in components manufacture, installation, construction, compliance with local and national codes, interfacing with the electrical utility, customer education, and consumer financing. This broadbased expertise may be critical in transitioning residential and commercial buildings from fluorescent and incandescent lighting to semiconductor lighting.

Strategies Unlimited (<http://www.strategies-u.com>) estimates the market for visible LEDs will grow to \$3.2 billion by the year 2003, with high-brightness LEDs comprising about one-third of this total. Annual market growth has exceeded 50% recent years. Significantly, a large fraction of the LED market is being captured by Taiwan and East Asia. The proposed Phase II SBIR work can provide an American company with a highly proprietary, patented LED technology to regain market share for the US.

4. Summary of Phase I Work

In this section, we review the Phase I experimental work and summarize the significant findings. The proposed approach is a considerable departure from conventional semiconductor technology, and there is a range of options for producing wire-shaped LEDs (none of which were obviously superior to the others nor sufficiently generic to include all materials and device designs). For these reasons, we opted for a broadbased experimental survey of crystal growth methods with applications to several semiconductors, and then focused on demonstrating the critical step in producing wire-shaped LEDs: the feasibility of producing device-quality cladding layers and p - n junctions in several types of compound semiconductors formed on a wire substrate. We were substantially successful in this. A p - n junction GaAs / Si light-emitting diode was formed on a 150-micron diameter carbon fiber. Further, we have found a number of highly promising crystal growth and processing steps to build a formidable technology based for wire-shaped light-emitting diodes.

4.1 Survey of Fibers and Fiber Selection

We identified and procured a number of candidate fibers for use as substrates for melt growth and CVD. These are summarized in TABLE 2 below. In fact, this was considered an important component of the Phase I work, namely to down select available fibers that were compatible with the crystallization processes. Varying amounts of data were provided by the supplier.

TABLE 2: Fibers Used as Substrates for Wire-Shaped LEDs

Fiber	Manufacturer	Other specifications
Hi-NiCalon™ SiCO fiber	Nippon Carbon Co.	Filament diameter = 14 microns Resin: PVA500 filaments per yarn density = 210 g / 1000 m
Sylramatic™ SiC Fiber	Dow Corning	0.150 mm diameter
Nextel™ Ceramic Fiber	3M	1000 Denier Roving
Tungsten	Johnson Matthey	0.025 mm diameter
Carbon fiber	Mitsubishi	0.010 mm diameter
SCS-6 SiC Filament	Textron	0.015 mm diameter
Boron filament	Textron	0.010 mm diameter
Tungsten silicide coated W wire	Prepared by IEC Univ. Delaware	0.120 mm diameter
Molybdenum	Alfa Aesar	0.025 mm diameter

4.2 Melt Coating of Si and Ge on Carbon or Refractory Metal Wires

Wire substrates can be pulled through crucibles containing molten silicon or molten germanium. Surface tension effects and pull velocities should permit control of coating thickness. These layers can be recrystallized to enhance grain size if necessary, as discussed in a late section. The process of melt coating is straightforward. The fiber is pulled through a pool of molten silicon or germanium contained in a graphite or silica crucible. The fiber pull speeds are 0.5 to 4 cm/min. Several systems at AstroPower were adapted to coat silicon and germanium on various fibers. FIGURES 11 and 12 show layers of silicon and germanium on 150-micron diameter carbon fibers by melt coating.

Figure 11: Scanning electron micrograph of Si-coated carbon fiber. Carbon fiber is 150 microns in diameter. Silicon coating is 20 microns thick. Average grain size is approximately 10 microns.

FIGURE 12: Ge/Si/carbon fiber composite. (similar to Figure 11 for silicon).

4.3 Silicon Chemical Vapor Deposition on Wires

We developed an iodine-based CVD process for coating various fibers with silicon cladding layers. In principle, this process can be applied to germanium and several III-V semiconductors. Silicon chemical vapor deposition is normally implemented with silane or chlorosilane precursors. Other silicon compounds are also feasible as precursors for Si CVD and may have definite advantages related to cost, deposition rates and efficiency, silicon utilization, process control, safety, toxicity, and waste disposal. In the 1960s, silicon transport based on reversible disproportionation reactions with iodine was demonstrated by several groups [GLANG *et al.*, WAJDA *et al.*, MAY]. For reasons specific to integrated circuit technology, halide transport using iodine or bromine was abandoned in favor of pyrolysis of chlorosilanes or silanes. However, CVD criteria for photovoltaic applications are markedly different than for integrated circuits and it is worth revisiting the early work with an eye towards low-cost silicon deposition. Recently, WANG and CISZEK of NREL have described the use of an iodine transport reaction for eventual application to thin polycrystalline silicon solar cells, the most recently reported results are summarized by the authors:

Grains as large as 20 μm are easily obtained. Higher temperatures favor larger grains. The typical growth rate is 3 $\mu\text{m}/\text{min}$ and strongly depends on the substrate and source temperatures. A minimum substrate temperature of about 800 $^{\circ}\text{C}$ is needed to start the deposition. An effective minority carrier lifetime of about 5 μs was measured, implying a diffusion length far exceeding the layer thickness.

SCHUMAKER has made an interesting argument that the larger size of precursor SiBr_4 and SiI_4 molecules relative to SiH_4 or SiHCl_3 imply a higher critical nuclei size and will thus raise the threshold for nucleation, resulting in sparser nucleation and silicon films with larger grain sizes, and also avoiding the spurious formation of silicon dust due to homogeneous nucleation in the gas phase that plagues Si CVD using silane or chlorosilanes.

AstroPower developed an iodine transport using a closed system wherein a silicon source and substrate fiber are heated as shown schematically in FIGURE 13. The appeal of this approach is its simplicity, high deposition rates, potential high utilization (i.e., near-100% deposition efficiency) of silicon, atmospheric-pressure operation, and its non-use and non-generation of highly toxic or dangerous materials. We easily achieved growth rates well in excess of 1 micron per minute. It should be emphasized that in this process the iodine transport agent is continually recycled, effectively avoiding the usual CVD costs associated with chlorosilane precursors. As a perspective, FALLER *et al.* determined that 60% of the total operating cost (chlorosilane, hydrogen, electric power) of depositing a 30-micron thick silicon film by chlorosilane CVD can be attributed to the cost of SiHCl_3 .

FIGURE 13. Schematic of Iodine Transport Process for Silicon CVD.

FIGURE 14 shows the vertical tube silicon CVD system. FIGURE 15 shows the graphite fixture used to hold the silicon source and fiber. FIGURE 16 the system in operation.

FIGURE 14: Vertical system for iodine transport silicon CVD.

FIGURE 15: Silicon CVD fixture to hold fiber and source.

Figure 16: Iodine-transport system for Si CVD on fibers.

4.4 Recrystallization of Silicon and Germanium on Wire Substrates

After depositing a Si or Ge layer by melt coating or CVD, the layer can be melted and recrystallized numerous times to enhance the grain size. FIGURES 20a through 20b show scanning electron micrographs of CVD silicon films that were recrystallized by creating a moving molten zone (about 0.5 cm in length) along the fiber by using a traveling (0.5 to 2 cm/min) infrared heater. The ambient was argon, but prior to growth, the silicon layer is encapsulated with a thin coating of silica formed by adding a small amount of oxygen to the ambient at 1000 °C. As can be seen the silicon cladding layers become much smoother and uniform upon recrystallization. It also appears that the grain size is invariably enhanced, but we defer any quantitative claims to future experiments planned for the Phase II program where a systematic study (using fiber x-ray diffraction, crystallographic etching, and electron or x-ray microdiffraction) of grain growth as a function of recrystallization conditions shall be performed.

FIGURE 20a: Recrystallized CVD silicon on carbon fiber (sample REX0328015-p1)

FIGURE 20b: close view of sample in 20a.

FIGURE 20c: Striations observed in silicon recrystallized on carbon

FIGURE 20d: Closer view of grain boundaries in recrystallized silicon on carbon fiber.

FIGURE 21: sampleX206-11 p1
Recrystallized CVD silicon on carbon fiber.

FIGURE 22: Recrystallized CVD silicon on carbon fiber.

The regularly spaced striations of FIGURE 20c may indicate excessively fast solidification and consequent constitutional supercooling. FIGURE 21 shows terracing (perhaps indicating a step flow mechanism of grain growth) on closer view of the recrystallized silicon. FIGURE 22 is interesting and important because the grains appear to be highly elongated and oriented very uniformly along the axis of the fiber. Such low angle grain boundaries might have less deleterious electrical properties. FIGURES 22a and 22b are views of sections of the silicon-on-carbon-fiber composite that were sheared to observe the cross-section after recrystallization.

FIGURES 22a and 22b: Cross-sections of recrystallized silicon on carbon fibers.:

FIGURES 23a and 23b show the results of a few experiments on multistranded NiCaLon fibers (see Table 2). This may be an option to improve wetting or alter the texture of cladding layer crystals for melt coating, CVD, or recrystallization.

Wetting of the fiber by silicon and germanium is a critical factor in this type of coating. As mentioned, the ambient and encapsulant coatings such as silicon dioxide or silicon nitride, possibly formed in-situ at high temperatures by control of the ambient, can drastically improve wetting and adhesion of the fiber.

A second issue in melt coating and recrystallization steps is related to contamination of the silicon or germanium with fiber components. This issue needs more attention in the Phase II program, but we do not believe contamination problems are severe since as will be presented later, we were able to fabricate *p-n* junction diodes in silicon formed on carbon and SiC fibers. At any rate, so long as contamination is confined to the silicon or germanium seeding layers and does not migrate into the compound semiconductor layers formed on the silicon or germanium, the purity of the silicon or germanium should not limit LED performance. Nevertheless, consideration of impurity redistribution should be considered in the global optimization of the LED design and fabrication process.

FIGURE 23 a and b: Recrystallized melt-coated silicon on multi-stranded fibers.

4.5 GaAs CVD on Wire-Substrates

The wire substrate is coated with a cladding layer of GaAs using a conventional GaAs chemical-vapor deposition (CVD) process modified with a fixture to hold the wire substrate horizontally in a heated zone. The system is shown in FIGURES 24a and 24b. Several transport agents (iodine, water vapor, or HCl) can be used for the growth. GaAs deposition directly on a carbon or silicon carbide fiber or on a carbon fiber or SiC fiber with a recrystallized silicon or germanium seeding layer was studied. Most studies used water vapor (2000 ppm_v) or iodine as the transport agent.

FIGURE 24a: Schematic of GaAs CVD system.

Figure 24b GaAs CVD system.

FIGURE 25 is a scanning electron micrograph of a GaAs cladding layer deposited directly on a 150-micron diameter carbon fiber using water-vapor transport CVD. The GaAs layer is 12 microns thick and the average grain size is 6 to 10 microns. FIGURE 26 is the energy-dispersive x-ray analysis (EDAX) spectrum which indicated the cladding layer was stoichiometric GaAs.

FIGURE 25: CVD-grown GaAs on 150-micron diameter carbon fiber (sample X206-12b-p1).

FIGURE 26: EDAX spectrum of GaAs deposited on carbon fiber. (sample X206-12b-p1.sp)

FIGURES 27a to 27h are side views of samples of GaAs grown on carbon fibers. Again, there is a strong dependence of grain size along the length of the non-uniformly heated fiber. FIGURE 27h shows a sheared sample of a carbon fiber which had a silicon seeding layer first deposited by CVD followed by a GaAs layer grown by CVD. The two layers are distinct in the micrograph and closer examination of such samples confirmed the not-surprising result that the epitaxial GaAs layer replicates the grain structure of the polycrystalline layer on which it is seeded. Therefore, if the grain size of the silicon seeding layer is enhanced by recrystallization, then larger-grain GaAs cladding layers should be achievable.

FIGURE 27e: (see text) sample V209-42.

FIGURE 27f: (see text):

FIGURE 27g: (see text) sample: X206-12a-p1.imx

FIGURE 27h: X206-12a-p2.imx cleaved section showing GaAs, underlying silicon seeding layer, and carbon fiber.

4.6 GaN CVD for Wire-Shaped LEDs

As mentioned, GaN is the prime candidate for wire-shaped LEDs due to its blue emission wavelength, high performance potential, tendency for oriented growth along the axis of the fiber, and tolerance of high defect densities, including grain boundaries. Unfortunately, the time frame and resources of the Phase I program did not permit an extensive development of a GaN wire-shaped light-emitting diode. We were, however, able to perform experiments showing the compatibility of a simple GaN CVD technique for producing the fibrous GaN crystals compatible with the wire-shaped LED geometry. We adapted a CVD system for the growth of GaN on silicon since we had obtained silicon-coated fibers as described previously.

FIGURE 28 shows a schematic of the GaN CVD system (photo in FIGURE 29) that uses infrared lights for heating. GaN chemical vapor deposition is based on a GaN powder source and atmospheric-pressure ammonia as the transport agent. The GaN powder is heated to 1100 °C and the silicon substrate is heated to 1050°C. FIGURES 30a and 30b are scanning electron micrographs of oriented GaN growth on single-crystal silicon substrates.

FIGURE 28: GaN CVD schematic.

FIGURE 29: GaN CVD system.

FIGURE 30a: GaN-on-silicon by CVD.

FIGURE 30b: (top-view of sample in 30a.

FIGURE 31: GaN whiskers

FIGURE 32 GaN fibrous growth.

FIGURES 31 and 32 shows whisker or fibrous growth of GaN produced by the CVD reaction. There is a marked tendency for GaN to grow in the filamentary morphology that is desired for wire-shaped LEDs. More controlled columnar growth is shown in two perspectives of FIGURE 33. The hexagonal crystal form of GaN is bound by its slowest growing facets which are planes in the zone axis oriented along the c-axis.

FIGURE 33: GaN column growing on a single-crystal silicon substrate.

4.7 Device Characterization

The samples comprised of silicon cladding layers on carbon fibers were fabricated into photodiodes in order to assess the quality of the silicon layer. A wrap-around junction was formed by phosphorus diffusion at 950 °C for 30 minutes. The samples were then selectively etched to partly expose the silicon under the diffused junction and contacted with a strip of aluminum deposited by thermal evaporation through a shadow mask. FIGURE 34 shows the current-voltage characteristics the wire-shaped silicon diode. The diode showed light sensitivity but this was difficult to quantify precisely due to the uncertainty in delineating the illuminated area of the diode. We estimated that the photocurrent density generated under one-sun AM1.5 simulated illumination was approximately 10 mA/cm². We presume that recrystallization to achieve larger along with more optimized device fabrication would produce higher photogenerated currents.

FIGURE 34: *p-n* junction formed by phosphorus diffusion of an emitter in a silicon cladding layer (25 microns thick) deposited by CVD on a 150-micron diameter carbon fiber. Hor scale: 1 V/div; Vert. Scale: 2 microA/div.

FIGURE 35: *p-n* junction formed in CVD-grown GaAs layer on a silicon cladding layer deposited by CVD on a 150-micron diameter carbon fiber. Hor scale: 1 V/div; Vert. Scale: 2 microA/div.

We then used carbon and silicon fibers (150 microns in diameter) coated with silicon cladding layers (both as-grown and recrystallized) as substrates for GaAs CVD. The GaAs overlayer was approximately 5 microns thick. The samples were Zn-diffused and fabricated diode by similar techniques to those described above for silicon diodes. A current-voltage characteristic for one of these GaAs / Si / carbon fiber diodes is shown in FIGURE 35. The sample generated an open-circuit voltage of 245 mV under AM1.5 illumination when operated as a solar cell. An infrared viewer showed room-temperature electroluminescence when driven with a current of 10 mA. More detailed analysis by way of low-temperature photoluminescence was made of the GaAs / silicon / fiber diodes. Several representative PL spectra for GaAs layers grown on silicon cladding layers are shown in FIGURE 36.

FIGURE 36: Low-temperature photoluminescence spectra of GaAs CVD layers grown on silicon cladding layers. PL measurement temperature is 9 K.

4.8 Summary and Important Findings of Phase I Work

To summarize, several techniques appear feasible for forming polycrystalline cladding layers of silicon, germanium, GaAs, and GaN on a wide variety of wire or fiber materials including carbon, SiC, and various refractory metals. The as-deposited grain sizes of these cladding layers are about 10 microns, but in some case, larger grains are observed. Recrystallization can enhance grain sizes up to 500 microns, and we believe with more effort even larger grain sizes are possible. Some preliminary experiments suggested and assessed techniques for making GaN wire-shaped light-emitting diodes. Simple diffused *p-n* junction devices were made in silicon and GaAs / silicon cladding layers deposited on carbon and SiC single-strand fibers. The samples so made showed good current-voltage characteristics and were light-sensitive when operated as photodiodes and solar cells. The GaAs / silicon wire-shaped diodes exhibited electroluminescence at room temperature when driven with a forward-bias current of 10 mA. It was concluded from the Phase I work that there are no insurmountable obstacles to making wire-shaped light-emitting diodes in the most important compound semiconductors currently used to make LEDs. Moreover, for most materials there are several highly promising methods for fabricating such devices. Finally, the characterization has suggested collateral solar cell applications for this technology that may be of commercial importance.

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Appendix: Analysis and Device Modeling

A fairly generic device model can be formulated which with some modification can be used to simulate performance of a number of devices such as LEDs, solar cells, detectors, and TPV cells made in a wide range of materials including silicon, germanium, GaAs, and other III-V compounds.

A model for filament or wire-based devices was developed in order to: 1. assess the potential of this approach for LEDs; 2. optimize device structures; 3. interpret device characterization, and 5. provide a sensitivity analysis of device performance to shunts, grain boundary effects, defects,

Obviously, the geometry of these devices lend themselves to cylindrical co-ordinates:

The steady-state combined minority carrier transport /continuity equation in cylindrical co-ordinates is given by

$$\frac{\partial^2 u}{\partial r^2} + \frac{1}{r} \cdot \frac{\partial u}{\partial r} + \frac{1}{r^2} \cdot \frac{\partial^2 u}{\partial \phi^2} + \frac{G(r, \phi)}{D} - \frac{u}{D \cdot \tau} = 0$$

where u is the excess minority carrier concentration, D is the minority carrier diffusion coefficient, and τ is the minority carrier recombination lifetime.

For the dark current of a solar cell or the injection current of an LED when $G(r, \phi)$ is 0, this equation reduces to

$$\frac{\partial^2 u}{\partial r^2} + \frac{1}{r} \cdot \frac{\partial u}{\partial r} - \frac{u}{L^2} = 0$$

where L is the minority carrier diffusion length.

The above equation is solved in terms of Bessel functions.

$$u(r) = J_0(k \cdot r) + B \cdot Y_0(k \cdot r)$$

where B is a constant and $k = 1/L^2$. The optics modeling to determine $G(r, \phi)$ can be complicated. Various ray-tracing software is available to handle this. Similarly, the extraction of light from wire-substrate LEDs can be modeled using ray tracing software. We purposely did not specify wire dimensions (wire and layer radii) in the preceding discussion. One aim of the modeling is to determine best device structures within constraints imposed by the fabrication processes.

The following analysis is for a semiconductor structure with an annular geometry (i.e., bounded by two concentric rings)

Using the technique of separation of variables, we assume $u(r, \theta)$ is of the form $u(r, \theta) = R(r) \cdot \Phi(\theta)$

and substitute into

$$\frac{r^2 R'' + rR' + \lambda r^2 R}{R} + \frac{\Phi''}{\Phi} = 0$$

where $\lambda = 1/L^2$
which implies that

$$\frac{\Phi''}{\Phi} = \text{const} = -n^2$$

for $n = 0, 1, 2, 3, \dots$

$$\Phi_n = \begin{cases} \cos n\theta \\ \sin n\theta \end{cases}$$

$$R = C \cdot J_n(\sqrt{\lambda} \cdot r) + E \cdot N_n(\sqrt{\lambda} \cdot r)$$

J_n is the modified Bessel function and N_n is Neumann's function. The constants C and E are determined by the boundary conditions. At the edge of the space-charge region the excess minority carrier concentration is 0. If the front surface is perfectly passivated, the derivative

$$\left. \frac{\partial u}{\partial r} \right|_{r=\text{surface}} = 0$$

If a wide bandgap emitter layer is used, then the front surface recombination losses are negligible. For the wire-shaped cells, we can assume the back surface is sufficiently far from the junction so as not to affect the minority carrier current.

Next, the minority carrier radiative recombination rate distribution is found as

$$\mathfrak{R} = \frac{\tau_{\text{rad}}}{\tau_{\text{rad}} + \tau_{\text{nr}}} \cdot u(r, \theta)$$

This expression can be numerically integrated over the quasi-neutral to determine the total amount of luminescence. Using such a model, the layer thicknesses of the wire-shaped LED can be optimized.