The CDF-II Silicon Tracking System

T.K. Nelson

M.S. 318, Fermilab, P.O. Box 500, Batavia, IL 60510-0500

on behalf of the CDF Collaboration

Abstract

The CDF silicon tracking system for Run II of the Fermilab Tevatron consists of eight layers arranged in cylinders spanning radii from 1.35cm to 28cm, and lengths from 90cm to nearly two meters for a total of six square meters of silicon and 722,000 readout channels. With an innermost layer (Layer 00) utilizing radiation tolerant p^+ -in- n silicon and low-mass readout cables between the sensors and readout electronics, double-sided vertexing layers (SVXII) designed for use with a deadtimeless secondary-vertex trigger, and outermost layers (ISL) utilizing mass-producible modules attached to a carbon fiber spaceframe, this system is a starting point for the next generation of silicon trackers for the LHC and Tevatron.

1 Introduction

A new silicon tracking system is a critical element in the upgrades to the CDF experiment for Run II of the Fermilab Tevatron. The new main injector and antiproton recycler result in a hundred-fold increase in luminosity for Run IIa with an additional factor of 2-3 for RunIIb slated to begin in 2005. This increase in luminosity and the accompanying change in bunch timing results in higher occupancies and collision rates, necessitating much faster detector systems. The choice of a novel drift chamber design (COT [1]) for the main tracking system necessitates a large silicon tracker or a third technology, since the inner radius of the COT is limited by aging and occupancy to 40cm.

* Based upon talk presented at the Fifth International Conference on the Large Scale Applications and Radiation Hardness of Semiconductor Detectors (Florence, July 2001).

Initially, the solitary silicon system proposed for CDF-II was SVXII [2], a vertexing and tracking detector consisting of five cylindrical layers of double-sided silicon. This design improves upon the previous SVX' by enlarging coverage and eliminating gaps, while providing the assembly precision to allow online triggering of 2-d displaced tracks. However, with an 10.6cm outer radius, this compact detector must be surrounded by another fast tracking device in order to robustly link to tracks found in the COT.

This intermediate tracker was first envisioned as a scintillating fiber device, but was changed to another silicon-based device, the Intermediate Silicon Layers (ISL [3]) in 1996. The ISL consists of one(two) cylinders of double-sided silicon in the central(forward) region. Along with linking tracks in the COT to SVXII, the ISL enables silicon-only forward tracking, and at nearly 2m in length extends the coverage for vertexing and b -tagging to $\eta = 2$.

Layer 00 [4] was added to the design in 1999 to enhance the performance of SVXII. Layer 00 consists of cooled single-sided radiation-tolerant silicon mounted on the beampipe using lightweight construction techniques. In addition to improving the impact parameter resolution and longevity of the tracker, Layer 00 provides valuable operational experience with the radiation tolerant sensors that will be important for RunIIb and the LHC experiments.

The combination of these three detector systems result in superior impact parameter resolution and tracking over a wide kinematic range, complimenting the capabilities of the COT to provide excellent tracking for CDF-II. Table 1 summarizes the properties of the silicon system. As the design of SVXII and ISL have been described extensively elsewhere, more emphasis will be placed upon Layer 00 here.

2 CDF-II Silicon DAQ

The three silicon systems of CDF-II vary widely in design, but are united as one by common readout electronics and data acquisition initially developed for the SVXII project [2]. These components include the SVX3 chip, the optoelectronic port cards, the silicon DAQ and the online silicon trigger for displaced tracks.

The SVX3D silicon readout chip [5] is fabricated by Honeywell in rad-hard $0.8\mu\text{m}$ CMOS. The front-end includes 128 channels, each with a charge-to-voltage preamplifier and 42 cell pipeline with 4 buffer cells. The back end includes a comparator, ADC and sparsification. The chip can be run in a deadtimeless mode: the front and back ends are capable of simultaneous, independent operation, facilitating timely use of silicon information in the trigger.

Table 1
The layout of the CDF-II silicon tracking system

Layer(Device)	z coverage(cm)	Radii(cm)	Axial Pitch(μm)	Stereo Angle	Stereo Pitch(μm)
1 (Layer 00)	$ z < 96$	1.35/1.62	25	—	—
2 (SVXII)	$ z < 94$	2.5/3.0	60	90°	141
3 (SVXII)	$ z < 94$	4.1/4.6	62	$+1.2^\circ$	125.5
4 (SVXII)	$ z < 94$	6.5/7.0	60	90°	60
5 (SVXII)	$ z < 94$	8.2/8.7	60	90°	141
6 (SVXII)	$ z < 94$	10.1/10.6	65	-1.2°	65
7 (ISL forward)	$20 < z < 64$	19.7/20.2	112	$\pm 1.2^\circ$	112
7 (ISL central)	$ z < 22$	22.6/23.1	112	$\pm 1.2^\circ$	112
8 (ISL forward)	$42 < z < 87$	28.6/29.0	112	$\mp 1.2^\circ$	112

Another key feature is the ability to subtract chip-wide pedestals on an event-by-event basis, allowing the real-time subtraction of common mode noise.

The beryllia portcards [6] mounted within $\approx 1\text{m}$ of the readout electronics regulate voltages, fan out power and control signals to entire “wedges” of the detector, and convert the digital output of the SVX3-based hybrids to optical signals for the DAQ, located $\approx 30\text{m}$ away. The Fiber Interface Boards (FIBs) that receive the data from the portcards along with all of the related timing and control modules comprise the DAQ.

The online Silicon Vertex Tracker (SVT [7]) capitalizes on the wealth of b -physics not captured by other triggers, allowing deadtimeless triggers on 2-d displaced tracks. Custom VLSI chips and an associative memory recognize hit patterns corresponding to displaced tracks. The SVT implementation requires exacting assembly tolerances for included layers (Layer 00 and SVXII): alignment of axial strips to $100\mu\text{m}$ over the entire length of the devices.

3 The SVXII Detector

The five double-sided layers of SVXII are assembled in three cylindrical barrels with beryllium “bulkheads” at each end for support and cooling of the modules, commonly called ladders. The ladders consist of two readout units of silicon with a hybrid at each end mounted directly atop the silicon to avoid gaps. The design is highly optimized, primarily in order to achieve the segmentation and assembly precision required for the SVT.

The cost of this optimization is complexity. There are separate silicon and hybrid designs for each of the five layers, and the ladders are quite complicated, resulting in difficult assembly procedures. A beryllia positioning plate and two hybrids are sandwiched around a sensor with a jumper to connect the ϕ and z hybrids to create a “quarter ladder”. After wirebonding, a second sensor is aligned and wirebonded with only fixturing for support to create a “half ladder”. Finally, two half ladders are aligned and support rails are glued to the face of the silicon. This configuration makes safe handling difficult. Roughly twenty hours of work and a six day pipeline are needed to build one ladder: assembly of all 180 ladders occupied four technicians for nine months.

The bulkheads were held in position on a rotational fixture and the ladders were installed from the inside out to assemble the barrels. Removal of a single ladder requires removal of a significant fraction of the ladders outside, so extensive testing was performed during ladder installation. Roughly five weeks were needed to install the 60 ladders in each barrel. Once the barrels were completed, a carbon fiber cover was added, the portcards and associated cooling that surround the barrels were installed and the barrels were mounted in the split-cylindrical carbon fiber/hexcel space tube.

4 The ISL Detector

The ISL takes a very different approach to overall design. A carbon fiber spaceframe with beryllium cooling ledges support 148 ladders of double-sided silicon. The ladders consist of two readout modules, each with three sensors and a double-sided hybrid all mounted to a common carbon fiber frame.

In contrast to SVXII, the single-minded focus of the ISL ladder design was simplicity [8]. There are two, nearly identical, double-sided silicon designs and only one hybrid design (AlN ceramic), resulting in all ladders being essentially identical. Three sensors and a hybrid are glued to a carbon-fiber frame and wirebonded to make a half-ladder. Two half-ladders are aligned and attached mechanically to create a full ladder. The frames allow very easy handling of the ladders, which can even be broken up into their component half-ladders if required. In contrast to SVXII, only five work hours and a two day pipeline were needed to fully assemble an ISL ladder. Ladder assembly took one technician seven months, along with a similar effort at INFN Pisa: a fraction of the SVXII ladder construction effort.

Ladder installation was similarly simple. Cooling and cabling were first installed in the spaceframe. Ladders were then installed, with removal of problematic ladders a relatively easy task. Despite the fact that many of the ISL modules were installed two or three times, the time required was still shorter

than for SVXII. The portcards for ISL and Layer 00 were then mounted together on cooling rings beyond the ends of the ISL.

5 The Layer 00 Detector

Layer 00 was conceived to enhance the performance and longevity of SVXII. SVXII has degraded performance for low-momentum tracks due to the silicon-mounted electronics and the resulting cooling requirements. With conventional double-sided silicon and readout chips mounted at small radius, there was also concern that the innermost layers of SVXII might not survive an extended RunII, with replacement of SVXII ladders a costly and time-consuming option. Placing a low-mass layer of radiation-tolerant silicon inside of SVXII recovers the lost resolution and enhances the longevity of the vertexing. Supported by the beampipe, such a device could also be replaced relatively easily.

The constraints on Layer 00 design are severe. It must fit between the beampipe ($r=1.25\text{cm}$) and the inner bore of SVXII ($r=2.1\text{cm}$). To meet the goal of lasting $5\text{-}10\text{fb}^{-1}$, it must withstand $5\text{-}10\text{MRad}$, requiring radiation-tolerant silicon which must be cooled to remove heat due to the ambient environment ($\approx 15\text{W}$) as well as that due to leakage currents after irradiation ($\approx 15\text{W}$). Material must be minimized to best benefit low-momentum tracking and with limited time and resources available, readily available components must be used wherever possible. Inclusion of Layer 00 in the (SVT) allows only certain geometries and requires stringent alignment. The design has six narrow (128 channel) and six wide (256 channel) groups in ϕ and six readout modules in z , with two sensors bonded together in each module for a total length of 95.5cm . The sensors are mounted on a carbon-fiber support structure with integrated cooling. To save space, eliminate material and protect the readout chips from radiation, the front-end electronics are mounted at larger radius on separate cooling structures beyond the ends of the silicon. The sensors are connected to the readout chips via long fine-pitch signal cables.

The sensors are single-sided $p^+n^-n^+$, $\langle 100 \rangle$ silicon with a $25\text{ (}50\text{)}\mu\text{m}$ implant (readout) pitch. These were produced by Hamamatsu Photonics (HPK), SGS-Thompson (ST) and Micron Semiconductor. Micron also produced oxygenated sensors. These sensors typically hold $700\text{-}1000$ Volts before breakdown, and have a low rate ($< 0.5\%$) of bad strips. The wide groups use only HPK sensors, while the narrow groups are comprised of five ϕ -wedges of ST sensors and one ϕ -wedge of oxygenated Micron sensors. The carbon fiber supports are fabricated using high-conductivity unidirectional material. The multi-layer construction is a complicated mix of 0° and 90° layers to achieve both the high thermal conductivity and the sharp corners required by the tight geometry. Four integrated cooling passages containing 2mm thin-walled aluminum tub-

ing remove heat from the silicon. Tests indicate that the warmest sensors operate at roughly -2°C before irradiation and 4°C after 5fb^{-1} . Even at a constant 5°C , Layer 00 should be operable for at least 7.4fb^{-1} . The readout cables are fabricated on $50\mu\text{m}$ thick polyimide film [9]. The traces are $1\text{-}1.5\mu\text{m}$ of gold atop $5\mu\text{m}$ of copper, and are $10\text{-}12\mu\text{m}$ wide. The $50\mu\text{m}$ pitch ($0.47\text{pf}/\text{cm}$) at the silicon and hybrid ends fans out to $100\mu\text{m}$ ($0.33\text{pf}/\text{cm}$) over most of the length to reduce capacitance: the longest is 47cm with a capacitance of $\approx 17\text{pf}$. The hybrids mount on conical carbon-fiber cooling structures beyond the ends of the silicon, placing the chips at large radius to reduce radiation exposure. All other DAQ is standard SVXII with the exception of HV supplies: all Layer 00 components are tested to 500V . Despite higher physics occupancy, readout time is less than that for SVXII due to the small number of channels, allowing the use of Layer 00 in the SVT.

To achieve the necessary alignment for the SVT, all six modules in each ϕ segment were simultaneously aligned and mounted to the carbon fiber structure. The completed detector was then transferred to the beampipe. The hybrids on one end were mounted to the support and cooling structures while those at the other end were tightly dressed to the beampipe for insertion into SVXII: insertion clearance was $300\text{-}450\mu\text{m}$ over the 1m length. Finally, the beampipe was supported from the SVXII spacetube and ISL extension cylinders via a system of carbon fiber legs to allow precise and stable alignment to SVXII.

6 Current Status

The detectors were completed between October and December of 2000, integrated and moved to the assembly hall for installation in January 2001. During accesses in February and April 2001, the testing and connection of the detectors to the power supplies and DAQ took place. This testing revealed some internal problems: 1 (of 108) dead chip in Layer 00, 3 (of 72) half-wedges and 3 (of 360) half-ladders in SVXII with problems, and 10 (of 296) half-ladders in ISL with problems. Some of these may be recoverable. It also appears that there is a solid blockage in the cooling lines for the central portion of the ISL which prevents operation of those ladders. While this may have resulted from excess glue in the assembly of some cooling lines, that hypothesis has not yet been confirmed and efforts to understand and remedy the problem continue. Meanwhile, commissioning commenced in March 2001 with the start of RunII.

Efficiency and occupancy are as expected: some poor Micron silicon in parts of SVXII and ISL reduces efficiency/occupancy in those layers, as shown in figure 1. Common mode pickup in the long cables of Layer 00 necessitates the use of the dynamic pedestal subtraction feature, but is otherwise as expected. DAQ tuning, timing relative to the Tevatron and other optimization are on-

Fig. 1. ISL ladder quality was judged by the relationship between efficiency and noise occupancy, which varies with the sparsification threshold. To keep readout time low, occupancy must be limited, so ladders were required to have better than 94% efficiency with less than 2% noise occupancy. Micron ladders have slightly fewer bad strips, but significantly more noisy strips than their Hamamatsu counterparts.

going. Tracking is now operational in SVXII and ISL, with more conservative operation of Layer 00 until machine conditions are better understood. Based upon early tracking results from SVXII, it appears that the required assembly tolerances for the SVT have been achieved [7].

7 Conclusions and Run IIb

The CDF-II silicon tracker should be ready for normal operation in the fall of 2001. Meanwhile, there is much to be learned from this project, which bridges the gap between the highly optimized but difficult to assemble silicon detectors

of the past (SVXII) and the mass produced (ISL) and more robust (Layer 00) systems of the future. The success of ISL production is an encouraging step towards the large LHC detectors, while Layer 00 will provide valuable operational experience with the radiation tolerant sensors that will be critical for those efforts. Furthermore, the lightweight techniques used in Layer 00 will benefit future detectors where increased occupancy forces the use of silicon where lighter drift chambers were previously preferred.

One such device is the CDF RunIIb silicon. The current design uses all single-sided radiation tolerant silicon: outer layers are simple small-angle-stereo modules similar to ISL and innermost layers are 0° - 90° layers much like Layer 00. All layers use fine-pitch cables between the sensors and the readout electronics to be built around the SVX4 chip: an improved SVX3 fabricated in $0.25\mu\text{m}$ CMOS.

References

- [1] K. Burkett, *Nucl. Instr. and Meth.* A 461 (2001), pp. 62-64.
- [2] J. Antos *et al.*, *Nucl. Instr. and Meth.* A 383 (1996), pp. 13-20.
- [3] A. Affolder *et al.*, *Nucl. Instr. and Meth.* A 461 (2001), pp. 216-218.
- [4] Pub. Proc. 2000 Meeting of Division of Particles and Fields, American Physical Society, Columbus, OH, August 9-12, 2000.
- [5] M. Garcia-Sciveres *et al.*, *Nucl. Instr. and Meth.* A 435 (1999), pp. 58-64.
- [6] J. Andresen *et al.*, IEEE Nuclear Science and Medical Imaging Including Nuclear Power Systems, 2000 Symposium, CD-ROM (2000), ISBN 0-7803-6506-2.
- [7] S. Donati, contribution to these proceedings.
- [8] M. D'Onofrio, contribution to these proceedings.
- [9] A. Gandi, CERN Microcable group.