An Implementation
of the LHCb Level 0 Muon Trigger
Using the 3D-Flow ASIC

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Abstract

The implementation of the LHCb Level 0 muon trigger using the 3D-Flow technique is discussed. The connection of the LHCb Muon Detector front end electronics to the L0 3D-Flow processor is also discussed.

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1 Introduction

We have investigated the possibility of implementing the L0 trigger using 3D-Flow asics currently under development [1, 2]. Several nice features of the 3D-Flow technique lend themselves to the L0 muon trigger. Among these features are

- the ability to gather information (in the case of the muon detector, binary hit information from pads) from a relatively large volume of the detector in an organized way, routing quickly to *one* cpu all the necessary information to identify a muon and to calculate its θ_x, θ_y, x intercept at the position of $\mu 1$ stations and y intercept at the interaction region in less than $3.2\mu s$.

- the ability to naturally buffer events so as to allow the requisite time for individual events to be calculated, respecting the limit that the average time per event must be $\leq 3.2\ \mu s$.

Figure 1: Muon System Components

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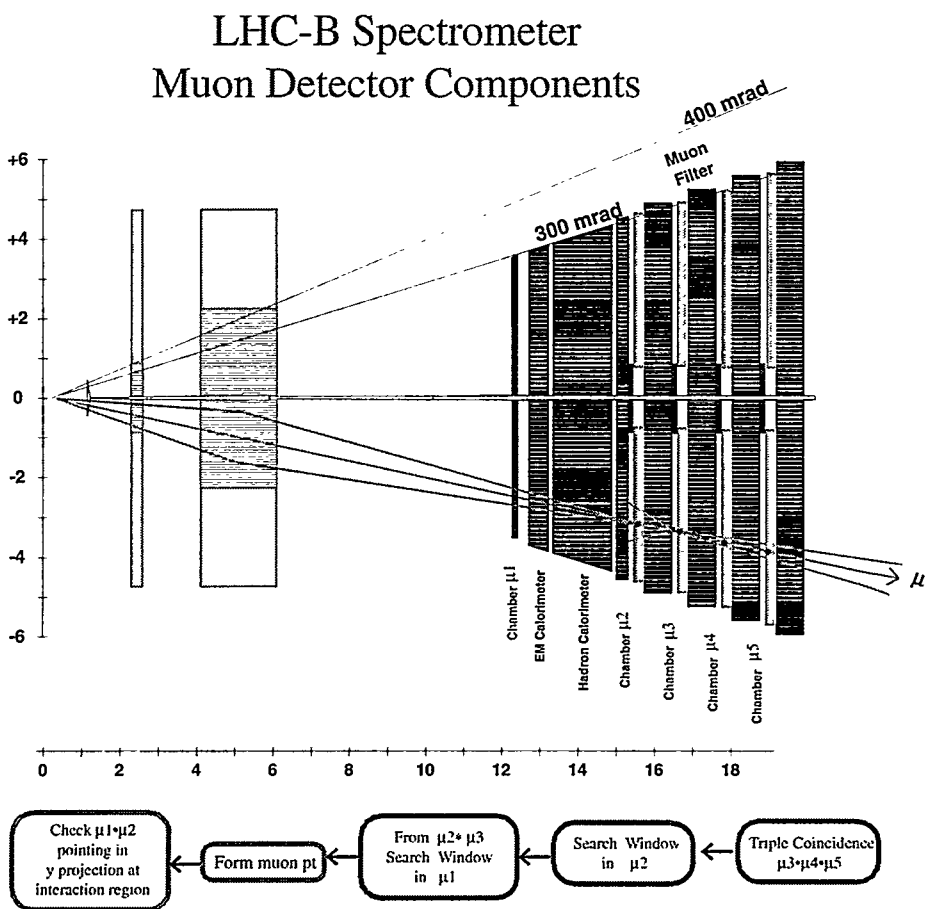
The LHCb Muon Detector components necessary for the LHCb L0 muon trigger are schematically shown in Fig. 1. The parameters of the LHCb Muon detector are given elsewhere in more detail [3]. Briefly, the muon detector consists of a shield whose components include the EM and hadron calorimeters and four layers of steel representing a dE/dx of ≈ 6 GeV and 20 interaction lengths and five muon stations for measurement of the muon trajectory.

1.1 The Muon Stations

Five stations μ1-5 composed of a mosaic of either Cathode Pad Chambers (CPC's) or Multigap Resistive Plate Chambers (MRPC's) serve to measure the trajectory of the penetrating muons using a pad structure which is projective in both x (bend plane) and y to the interaction region. The stations are positioned as shown in Fig. 1. The μ1 station is positioned immediately upstream of shield at 12.15 meters from the interaction region and the μ2-5 stations are embedded in the shield at average positions of 15.50, 16.60, 17.70 and 18.80 meters. The muon stations embedded in the shield must fit in the ≈ 40 cm available between the shielding walls. According to present plans, the μ1 station will be composed of four layers of CPC's. The μ2-5 stations are a combination of four layers of CPC's in the small angle region and two layers of MRPC's for the bulk of the coverage in the large angle region. Each layer of MRPC's is an independent 4 × 0.8 mm gap MRPC. The stations inside the steel are protected from the beam by shielding between the steel walls which extends from 10-15 mrad and 10-12 mrad in the x and y projections respectively.

1.2 The Muon Chamber Pad Structure

The necessity of forming the Level 0 muon trigger in 3.2 μs mandates a 2D pad structure in μ1 − 5 so that muon 3D hit information is available at the earliest possible time for the Level 0 muon trigger. A variety of studies have defined the μ1-5 pad configurations [4].

In order to minimize the number of pads required, each of the five muon stations shown in Fig. 1 has four regions with different pad sizes. The pad sizes in each muon layer of the various muon stations increase by a factor of two as we proceed from the region nearest the beam to the outermost region, thereby approximately preserving the average solid angle subtended by a pad in the different regions. The pad sizes in a given station are scaled relative to the upstream most muon station μ1 by the position of the stations relative to the interaction region in order to produce a pad configuration projective in both x and y to the interaction region.

The x sizes of the pads in μ stations 1 and 2 are dictated by the precision which the trajectory of the muon in the x must be measured in order to obtain good p_t resolution in the Level 0 trigger. The y sizes are chosen to allow good pattern recognition and reject spurious machine associated backgrounds [5] by pointing at the interaction region in the y projection. Since more precision is required in the x projection for determination of the muon p_t, a y/x aspect ratio of two to one has been adopted for the μ1-2 pads. After studies of pad sizes based on the effect on pattern recognition and Level 0 trigger performance,

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μ1 Pad Configuration

Region I and II
magnified by a
factor of 2
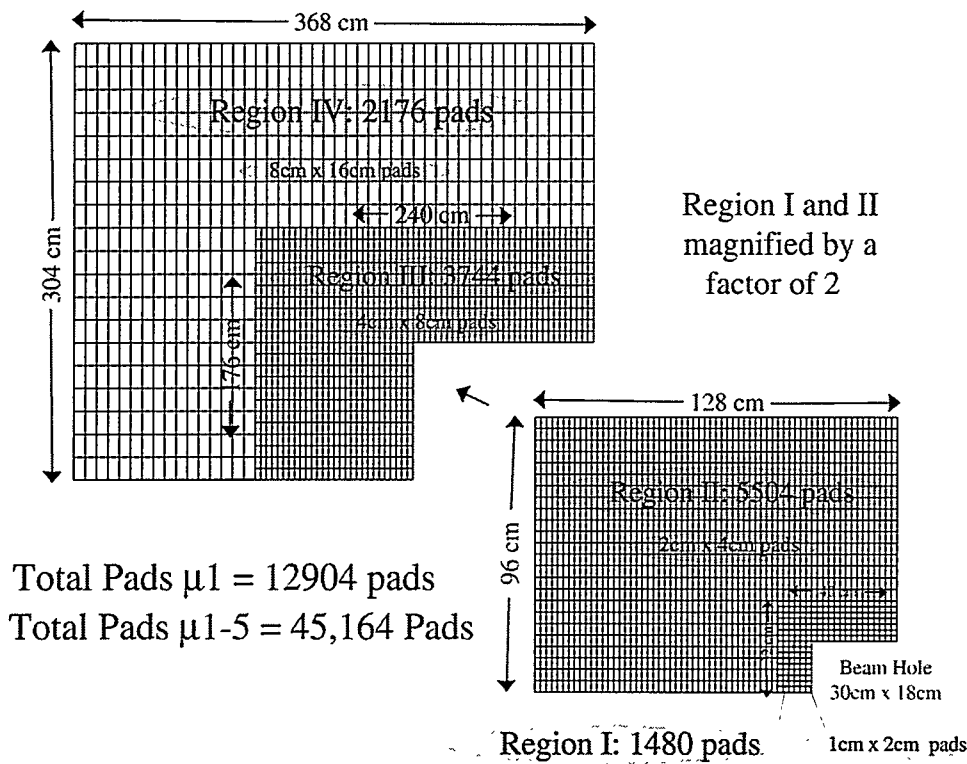
Total Pads μ1 = 12904 pads
Total Pads μ1-5 = 45,164 Pads

Figure 2: μ1 pad configuration

the pad structure given in Table 1 and shown in Fig. 2 below has been adopted for μ1. As mentioned above, the μ2 pad sizes are simply scaled relative to those of μ1 by the relative distance of the two stations from the interaction region.

The sizes in μ 3-5 are set by the requirements of clean pattern recognition of penetrating muons and formation of triple coincidences. The pad configuration for μ 3, 4 and 5 is similar to that of μ1,2 except that the x pad size in μ3-5 has been doubled relative to the x pad sizes of μ1 and 2, reflecting the lesser need for spatial resolution to find the triple coincidences. Hence, μ3, 4 and 5 pads have y/x aspect ratios of 1/1 but are still scaled by distance to the interaction region so as to be projective to the interaction region.

Region	x (cm)	y (cm)	θ_x (mrad)	θ_y (mrad)	Pad Size (cm)	# of pads
Beam Hole	$\mid x \mid \leq 30$	$\mid y \mid \leq 18$	$\mid \theta_x \mid \leq 24.7$	$\mid \theta_y \mid \leq 14.8$	-	-
I	$\mid x \mid \leq 40$	$\mid y \mid \leq 32$	$\mid \theta_x \mid \leq 34.6$	$\mid \theta_y \mid \leq 26.3$	1.0x2.0	1480
II	$\mid x \mid \leq 128$	$\mid y \mid \leq 96$	$\mid \theta_x \mid \leq 105.3$	$\mid \theta_y \mid \leq 79.0$	2.0x4.0	5504
III	$\mid x \mid \leq 240$	$\mid y \mid \leq 176$	$\mid \theta_x \mid \leq 197.5$	$\mid \theta_y \mid \leq 144.9$	4.0x8.0	3744
IV	$\mid x \mid \leq 368$	$\mid y \mid \leq 304$	$\mid \theta_x \mid \leq 302.9$	$\mid \theta_y \mid \leq 250.2$	8.0x16.0	2176

Table 1: μ1 plane pad configuration

The large capacitances of some of the pads in the large angle regions dictate that they be divided into smaller "physical" pads (a total of 232K for the μ1-5) which will then be ORed to form the "logical" pad structure (45K for μ1-5) of Fig. 2. The 3D-Flow processor will only have to deal with the "logical" pads.

2 The L0 Muon Trigger

The Level 0 muon trigger has the fundamental design goal of reducing the muon trigger rate due to $\pi/K \to \mu + x$ decays from minimum bias events while maintaining good efficiency for $B \to \mu + x$.

2.1 The L0 Muon Trigger Algorithm

The present L0 muon trigger algorithm is composed of the following steps executed in chronological sequence in less than 3.2 μs to be consistent with the length of the Level 0 pipeline:

- form triple coincidences of pad hits in specific search regions in μ4 and 5 based on "seed" hits in the μ3 plane.

- open search region in μ2 based on μ3 "seed" hits and form all μ2-μ3 combinations for all triple coincidences, .

- calculate x intercepts at μ1 of μ2-μ3 combinations.

- take closest hit pad in μ1 to x intercept of μ2-μ3 projection into μ1.

- calculate the μ1-μ2 combination x and y slopes and y intercept at the interaction region.

- calculate the p_t of the muon candidate from the x slope of the μ1-μ2 combination assuming that the track originated in the target.

- require that the y intercept pass within a certain y distance of the center of the interaction region.

Fig. 3 shows the expected resolution of the muon trigger p_t achieved with this algorithm and the pad structure discussed above.

3 3D-Flow Implementation of the Level 0 μ Trigger

The following section gives details of the implementation of the LHCb L0 muon trigger algorithm using the 3D-Flow asics. The parameters that affect the configuration of the 3D-Flow system include channel occupancy, required bandwidth at different L0 algorithm

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stages, and required channel reduction at different stages of the L0 trigger. Monte Carlo's of $B \to \mu$ and minimum bias $\pi/K \to \mu$ decays have been used to evaluate the performance of the 3D-Flow system with respect to these parameters as well as to minimize the number of asics required consistent with minimizing trigger rates and maintaining $B \to \mu$ efficiencies at different stages of the L0 muon trigger algorithm.

3.1   General Environment/Configuration for the 3D-Flow System

The pad configuration of the LHCb muon detector planes, μ1-5, generates 45,164 "logical" pad signals every 25 ns, a small subset of which is required by each individual 3D-Flow processor for execution of the Level 0 trigger algorithm. In spite of the fact that only a small percentage of these pads have signals for any interaction, all 45,164 pads will be transported in parallel to the 3D-Flow processor for each beam crossing. This is to avoid using part of the 3.2 μs available for execution of the Level 0 trigger for sparcification and encoding. At the LHCb average luminosity of $2.0 \times 10^{32} cm^{-2} s^{-1}$ only 31% of the "real" bunch crossings will have one interaction (note that only three of four beam bunches will actually cross, hence the qualification of a beam crossing as "real"). The 3D-Flow processors operate at 80 MHz, and is capable of fetching two 32 bit words of data every beam crossing.

The signals from the pads are binary $(0,1 \equiv$ no hit, hit respectively). Since the signals from the μ planes are slightly out of time with one another because of lead lengths and time slewing due to differing capacitances of the various pad sizes, they must be synchronized with trimable or programmable delays before reaching the 3D-Flow processor which assumes the 45K bits from a given beam crossing are in time.

Monte Carlo studies of the hit coordinates of $B \to \mu$ in each μ station have been used to determine search windows which result in good efficiency. The search windows in the y
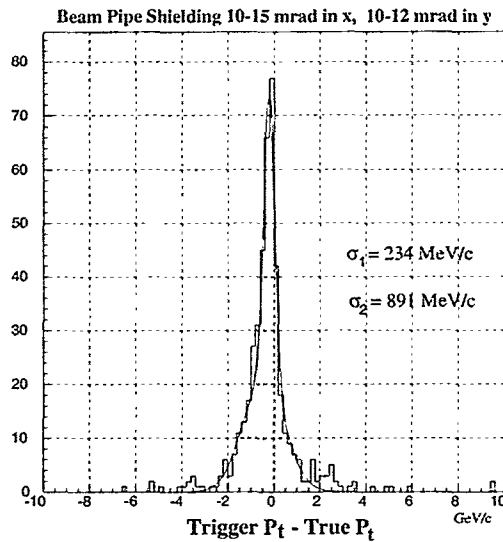

Figure 3: Muon trigger p_t - true p_t for $B \to \mu$

projection $\mu 4$ and $\mu 5$ has been determined to be ± 1 pads (relative to the index of the seed pad of $\mu 3$). The extent of the search region in x is ± 1 and ± 2 for $\mu 4$ and $\mu 5$ respectively. In $\mu 1$ and $\mu 2$ the y search window is ± 0 (only the row with the seed pad index needs to be interrogated). In the x projection, the search window extent is ± 8 pad for $\mu 1$ and ± 2 for $\mu 2$. Thus a total 47 pads in a reasonably small transverse region of $\mu 1$-5 relative to the $\mu 3$ seed pad must be collected in order to insure good efficiency for a muon that passes through that seed pad. These pads must be routed quickly to a single 3D-Flow processor in order to execute the Level 0 algorithm. Because of the design of the 3D-Flow system where an individual processor can communicate with processors on all sides of itself, this set of signals can easily be assembled in an individual processor. Therefore, the 3D-Flow processors, which can input 32 bits of information and share it with their neighboring processors every beam crossing, are well suited for this application.

The number of pad hits per station per interaction is very modest (of order 1% of the total pads on average for $\mu 1$ which is the busiest of the stations). However, the Monte Carlo simulations show that the mean occupancy of the $\mu 3$ seed station is ≈ 16 per interaction (based on full showering in the muon shield as predicted by MARS). The 3D-Flow Level 0 trigger will then have to handle approximately this number of "seed" hits every interaction and no reduction of rate is achieved by finding seed hits in $\mu 3$ other than rejection of crossings that have no interaction (40 MHz to 12.4 MHz). On the other hand, requiring hits in areas of μ 4 and 5 that form muon triples does reduce the rate by a factor of 4 (from 12.4 MHz to 3.1 MHz). Moreover, the number of pad signals that could be associated with a given $\mu 3$ seed hit that must be routed to a given processor to perform the algorith is modest (47 per seed pad)

Therefore, it is logical to design a two "stack" 3D-Flow Level 0 trigger, the first stage of which will be a large array of 3D-Flow processors to be connected to the 45,164 detector pads and which will distribute information to the nearest eight neighbor processors, and accept information from the eight neighbors in order to collect in one processor the 47 pad signals necessary for execution of the algorithm. In addition the first "stack" will execute only the first part of the Level 0 algorithm, i.e. finding the $\mu 3$ "seed" hits and the associated triple coincidences. This will produce a reduction of trigger rate to 4 MHz and greatly reduce the amount of data to that must be passed on to a second smaller "stack" (a maximum of 16 processors required in the second set of 3D-Flow processors based on the 2-3 triple coincidences expected at maximum per interaction) which will execute the remaining, more time consuming part of the algorithm.

Designating the initial array of 3D-Flow processors as a "layer", a "stack" of such layers would provide for the buffering that may be necessary to accommodate the handling of subsequent events which may arrive before the processing is finished in the first "layer" of 3D-Flow processors. Additional, more complicated steps of the algorithm would be deferred to a second (or even a third) "stack' of 3D-Flow asics which could be smaller and have more time for processing, reflecting the fact that only a few $\mu 3$ "seed" hits are expected per interaction and each step of the algorithm reduces the rate and volume of data for subsequent steps. These considerations lead to a 3D-Flow system as schematically represented in Fig. 4.

Pads Required from Muon Detector Planes for L0

Pad Region Sizes

5x3=15 pads

3x3=9 pads

Seed Pad

5x1=5 pads

17x1=17 pads

μ5   μ4   μ3   μ2   μ1

• the time required to execute the algorithm mandates
significant buffering via stack layers

• multiple stacks are desirable to
allow splitting of the algorithmin to slower and faster parts

• 47 pads are associated with
one μ3 "seed pad" and

• must be collected in one proceesor in order
to execute the Level 0 algorithm

• pads are to be shared with other seed pads

Stack I
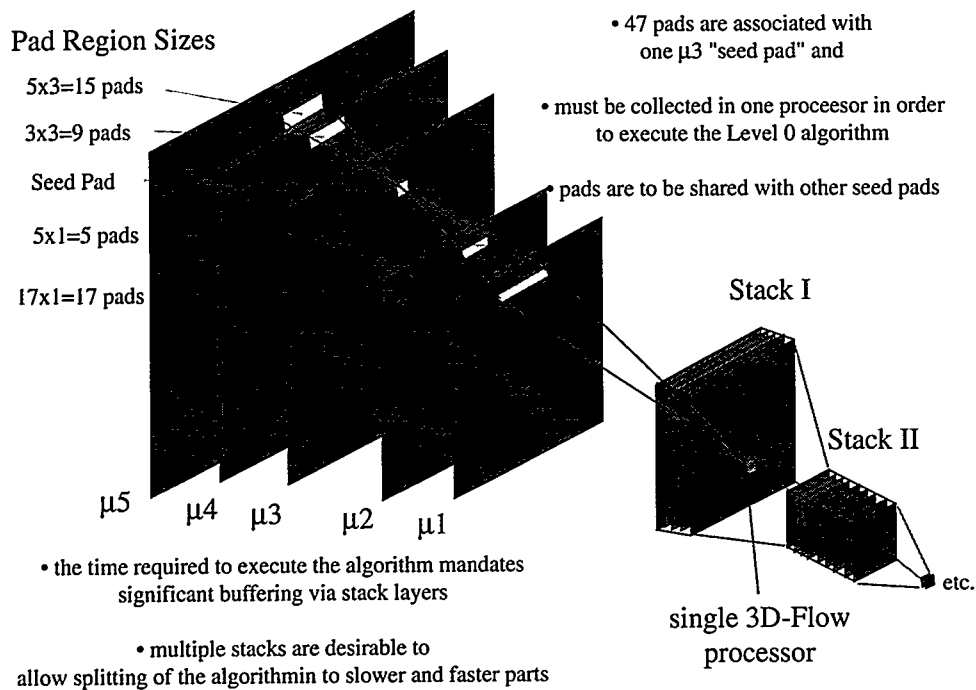
Stack II

single 3D-Flow
processor

etc.

Figure 4: Schematic of the 3D-Flow system

Using Monte Carlo simulations of this strategy, 3D-flow asics have been designed and an optimum 3D-Flow topology has been configured that fulfills the requirements, providing a large degree of flexibility for future changes, and optimizing cost by balancing the computer power with the routing necessary in the overall system. The bandwidth at different stages of the system has been checked in worst-case conditions.

3.2 Interface of Muon Detector to the 3D-Flow Processor

As stated above, all pad signals from the Muon Detector are assumed to be in time and are received in parallel by the 3D-Flow processors. Fig. 5 shows the flow of pad signals into a typical 3D-Flow processor in the first "stack" of 3D-Flow processors. These pads are hardwired to a given processor. The central dotted rectangle, which represents a typical 3D-Flow processor, shows the number of pads and from which plane they are received by a given processor. Each processor receives from the detector 31 bits of information (in two 16 bit words) from 31 pads in μ1-5. Five pad signals are received directly via the top port of the 3D-Flow from each of μ2-5 stations. Eleven pad signals are received from μ1. This collection of signals comprise the 31 bits of the 32 bit data word that is read in directly
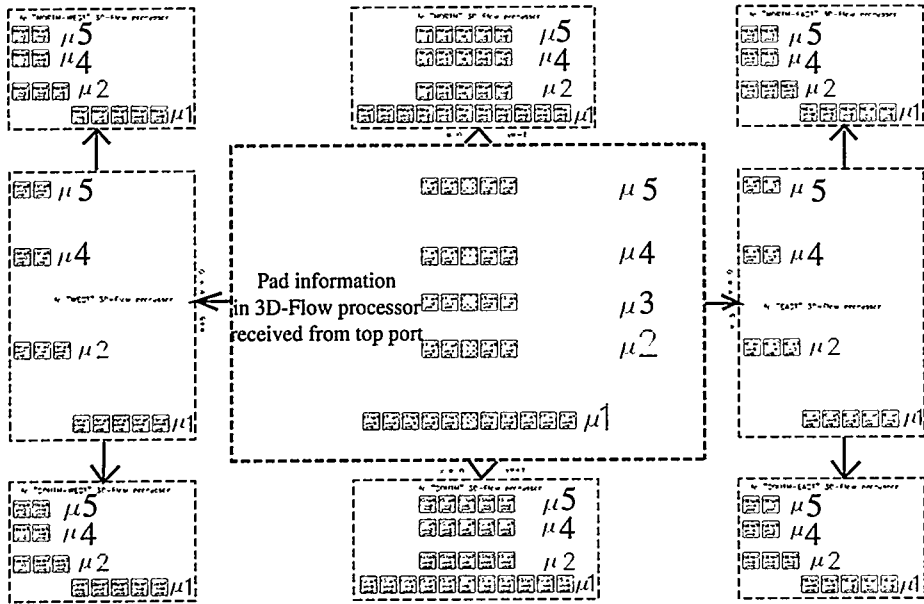
Figure 5: Pad hit collection by individual 3D Flow processors; flow of pad information shared with adjacent processors

from the Muon Detector per beam crossing.

3.3 Data Sharing with Adjacent Processors

Some of the data directly read in by a 3D-Flow processor are sent to the neighboring processors, which are shown in dotted rectangles surrounding the central processor in Fig. 5. In addition, the central 3D-Flow processor receives pad information from adjacent processors as shown in Fig. 6. The entire ensemble of pad signals required for execution of the Level 0 algorithm is also shown in the central rectangle of Fig. 6. The pads shown within the central dashed rectangle include both those that are directly read in and those that are received from its neighbor processors. The neighboring processors are shown in dashed rectangles together with the information that they transmit to the central processor.

The data and strobe lines in the interconnections between the processors are relatively simple. The same data lines and strobe lines are connected from a processor in an outer region to two processors in the inner region. The handshake return signal of FIFO FULL from the inner region processors needs an OR function. An OR function has to be inserted for the data that are transmitted from two processors of an inner region to one processor of an outer region. The same FIFO FULL handshake signal is sent from the outer region processor to the two inner region processors. Only one strobe from one of the inner region processors will be used to store the data into the outer region processor. All steps in the first part of the program routing the data are idenical, thus assuring synchronization.

As represented in Fig. 5 and Fig. 6, the sequence of events that takes place to collecting all hits associated with a valid muon with the required minimum p_t is as follows:

- Each processor is hardwired to receive information from five pads with the same x
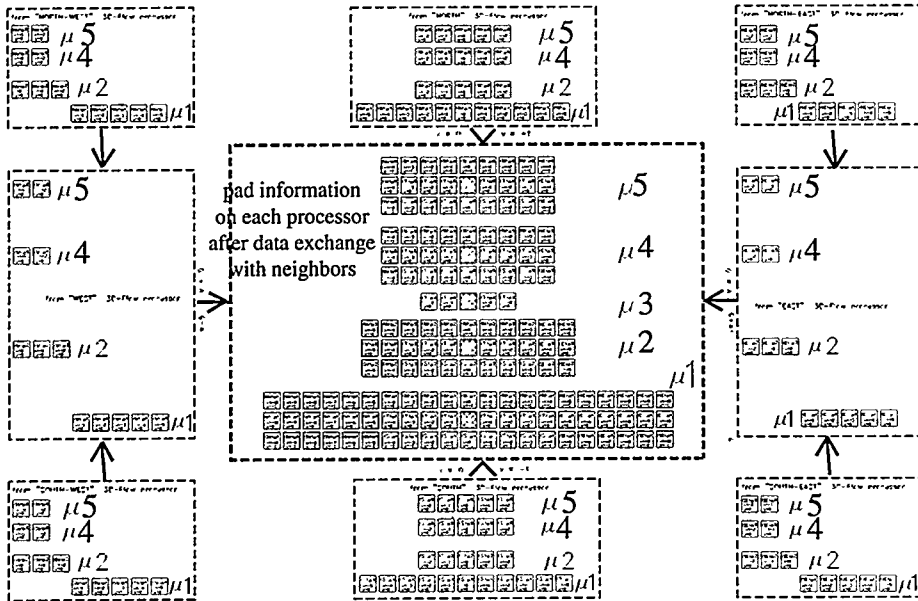
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Figure 6: Collection of pad information required for L0 by the 3D-Flow asic

and y indices in each plane μ2-5 including five "seed" pads from μ3.

- Each processor is hardwired to receive eleven pads from plane μ1. The additional pads are required because of the larger search window in μ1. This requires a two fold fan-out for the μ1 pads since they are used by more than one processor.

- After acquisition of the these pads from the detector, each processor sends pad information to the eight neighboring processors according to the scheme of Fig. 5.

- Simultaneously, each processor receives the information from the eight neighboring processors according to the scheme in Fig. 6.

- Each processor checks for μ3 "seed" hits. They also check for hits in the search windows of μ4 and μ5 which indicate a triple coincidence if time permits.

- If a "seed" hit (or, more ambitiously, a triple coincidence) is found, all pad information associated with the μ3 "seed" necessary to perform the L0 algorithm is sent to the second stack which can operate at a more leisurely rate in calculating the remaining part of the algorithm.

4 Summary

This brief note has outlined the strategy of the 3D-Flow system. As has been shown, the collection of pad information from a volume of the muon detector is gracefully and speedily

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handled by the 3D-Flow. In addition, the 3D-Flow system allows one to tailor the system to economically handle the 40 MHz input rate by executing different algorithm steps in different stacks, performing the simpler and more effective cuts early on and deferring the more complex calculations to later stacks. In addition, the "layering" of the system makes the buffering of incoming events quite natural, allowing operation at an input data rate of 40 MHz and a clock rate of 80 MHz. It is estimated at present that $\approx$ 2000 3D-Flow asics are required for the Level 0 muon trigger.

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