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Characterization of Indium and Solder Bump Bonding for Pixel Detectors[#]

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Abstract

A review of different bump-bonding processes used for pixel detectors is given. A large scale test on daisy-chained components from two vendors has been carried out at Fermilab to characterize the yield of these processes. The vendors are Advanced Interconnect Technology Ltd. (AIT) of Hong Kong and MCNC in North Carolina, USA. The results from this test are presented and technical challenges encountered are discussed.

1. Introduction

The BTeV pixel detector, like most pixel systems being developed for high energy physics experiments, is based on a design relying on a hybrid approach. With this approach, the readout chip and the sensor array are developed separately and the detector is constructed by flip-chip mating of the two together. This method offers maximum flexibility in the development process, choice of fabrication technologies, and the choice of sensor material. However, it requires the availability of highly reliable, reasonably low cost fine-pitch flip-chip attachment technology.

We have tested three bump bonding technologies, indium, fluxed solder, and fluxless solder. Table 1 summarizes the main characteristics of the indium and the solder bumps that we used for the results reported here.

From a practical point of view, the cost and the availability of a given technology are driving considerations. The multi-chip modules, which are the basic building blocks in pixel detector systems used in high energy physics experiments, have readout chips closely abutted to one another. This is very different from what is commonly done in industry. Our fine pitch and the requirement for small bumps also pose technical challenges to the vendors. Furthermore, our production quantities (number of wafers), while large by our own standard, are minuscule for industry. Our task is then to find industrial partners willing to work with us to adapt their technologies to our needs.

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2. Bump Bonding Process

The basic process flow used in the bump bonding is rather well established. This includes substrate preparation, bump growth, and finally a flip-chip mating step.

Substrate preparation is necessary to remove the insulating layer of aluminum-oxide that is formed on the Al pads. This step is critical for ensuring good electrical conductivity. Typically, this is done by sputtering an under-bump metal (UBM) onto the Al pads. Two or three layers (each of the order of 1-3 micron thick) of metal are sputtered. They also serve as a diffusion barrier and improve the adhesion of the bumps to the pads. The bumps are then put on by electroplating (solder) or evaporation (indium) to one (solder) or both (indium) of the substrates to be mated. The final step is to attach the substrates together. This requires a special flip-chip bonder with an alignment precision of 1-2 microns. Heat (solder) or pressure (indium) is then applied to form the mechanical bond[1].

3. Tested Components

We have conducted tests on dummy detectors produced by two companies to evaluate efficiency of bump-bonding with indium and eutectic Pb/Sn solder. The vendors are Advanced Interconnect Technology Ltd. (AIT) of Hong Kong and MCNC in North Carolina, USA. Table 2 shows the parameters of the dummy detectors we tested.

The detectors are composed of channels which are a number of daisy-chained bumps at a certain pitch connected to probe pads at an edge of the dummy detector. Fig. 1 shows a schematic layout of a portion (8 channels) of an AIT detector. We characterized the bump yield by measuring the resistance of each channel, and (to check for shorts) the resistance between neighboring channels.

4. Results

4.1 AIT detectors with aluminum base metalization

These detectors have 30 micron pitch indium bump-bonds. The pads and the strips (20 micron wide, 2 micron thick, and 5230-11130 micron long) are aluminum. The channels have 28 or 32 daisy-chained bumps (see Fig. 1). We studied a subset of these detectors and observed that most of the channels were either open or had high resistance (~100 KOhms). In Fig. 2 we show the resistance over the daisy-chained bumps of some channels before and after applying various voltages. As seen from the figure, the application of voltage cured the channels by significantly reducing their resistances. Aluminum surface oxidization before the sputtering of under bump metal (UBM) is significant, causing the connectivity problems. According to the vendor, this is caused by the fact that the sputtering process was not done long enough to remove the oxide

completely. Believing that we can not fix the problem at this stage of testing, we abandoned the study and concentrated on the AIT detectors with gold base metalization.

4.2 AIT detectors with gold base metalization

These detectors also have 30 micron pitch indium bumps, but with gold base metal. Geometrically, they are identical to the detectors described in Section 4.1 above. Fig. 3 shows the resistance measured over the bumps of a detector via the gold strips and pads. The resistance of the flip-chip assembly is proportional to the length of the gold strips and the pattern is repeated every 4 channels as expected (see Fig. 1). We measured resistance of the gold strips to be 4.63×10^{-2} Ohms/micron. Using this information and the measured length of the strips connecting the bumps to the pads, we deduce that the resistance of each bump is of the order of 1-2 Ohms.

The results of resistance measurement of the channels (over the bumps) of all detectors indicate that one detector had 2 open channels while the others had none. This detector and six other detectors had high resistance channels (over 5KOhms). This translates to a channel yield of 4.7×10^{-2} failure/channel or bump yield of 1.6×10^{-3} failure/bump if we consider the high resistance channels as failures. If we exclude the two detectors with large number of high resistance channels, the rate becomes 3×10^{-4} failure/bump.

We measured the resistance over the adjacent channels. The adjacent channels belong to two separate chains of bumps; therefore they have no electrical connection to each other. We expect then the resistance to be infinite (open channel). But we observed quite a few shorted adjacent channels (resistance similar to the resistance over the bumps), and many high resistance adjacent channels. Some are open as expected. High resistance values varied from ~100 KOhms to ~1 MOhms.

We suspected that the bumps on one end of chains were in contact with the bumps on the other end of the adjacent chain causing the shorts and the high resistance connections. The vendor pulled apart the top layer of a detector and took pictures of such locations. It clearly showed that the bonds are well separated. The vendor observed during the production that the indium diffused beyond the two metal barrier indiffusion layers to make contact with the Au-metallized lines to form an electrical connection. This needs to be substantiated by further measurements.

4.3 MCNC fluxless solder bump detectors

These are the detectors with 50 micron pitch eutectic Pb/Sn (37%/63%) bump-bonds. The base metal for strips and the pads in these detectors is aluminum. The strips are 15 micron wide, 2 micron thick, and 2100-8000 micron long. The channel layout is geometrically very similar to the layout shown in Fig. 1. The number of bumps in each channel is either 14 or 16. The vendor, MCNC, jointly with Unitive Electronics, Inc. produced these detector assemblies with a process called Plasma Assisted Dry Soldering (PADS)[2]. No flux is used. The bumped chip wafer (top plates of the detectors) and un-

bumped substrate wafer (bottom plates of the detectors) were diced and aligned together (flip-chip assembly) before being treated in the PADS process. The joins were then reflowed at 250^{o}C. After being reflowed, the detectors were rinsed with methanol and dried in air.

A scanning electron micrograph of the solder bumps is shown in Fig. 4. The diameter of the bumps is ~40 microns, and the height is ~15 microns after mating. Channels of 14 or 16 daisy-chained bumps were measured for connectivity and adjacent channels were measured for shorts. Fig. 5 shows typical measurements of the channel resistances over the bumps. We measured the aluminum strip resistance to be 6.55×10^{-3} Ohms/micron. Compared to the gold-strip detector resistance measurement (see Fig. 3), the aluminum resistance measurements were less certain. The aluminum was soft and flaky, requiring larger force on the probe to make a good electrical contact and, as a result, there were fluctuations in our measurements. This was true on all measurements involving aluminum pads. Nevertheless, we estimate that the single solder bump resistance is less than 1 Ohm as expected.

Two of the 82 detectors were misaligned to cause a one bump shift resulting in open channels and shorted adjacent channels. Five detectors had over 50% of their channels open or at high resistance. One was sent to MCNC to be examined. It was taken apart and found to have the bumps on the top plate (chip) not touching the pads on the bottom plate (substrate). This was probably due to contamination or debris on the substrate on that particular location. In the following analysis, we exclude these seven detectors.

None of the detectors had adjacent channel shortages, but some had open daisy-chained bump channels. Some of these open channels could be cured to be closed again by applying voltage over the bumps. Fig. 6 shows a histogram of the cure voltages. After attempting to cure all the open channels, those that remained open are histogrammed in Fig. 7 and those cured are histogrammed in Fig. 8. We do not understand the curing mechanism. First of all, the cure was permanent, i.e. we remeasured some of the cured channels a few days after and found them still cured. Voltage application might be burning out some residues or debris, or even the aluminum oxidization. A possible explanation for this is that the aluminum pads were not properly prepared for bump bonding. The UBM was put on by deposition instead of sputtering, and therefore the oxide layer formed on some of the aluminum pads may not be removed completely.

All this results in an assembly yield of 91.5% (75 good out of 82). For the good detectors, a channel yield of 99.32% or 6.8×10^{-3} failed-channel/channel (106 open or high-resistance channels altogether), and with 14 or 16 bumps per channel and with the assumption that only one bump is bad, a bump yield of 99.95% or 4.5×10^{-4} failure/bump.

4.4 MCNC fluxed solder bump detectors

These detectors are identical to the ones produced by the PADS process except that the soldering procedure involved a mildly activated flux. After being reflowed, the assemblies were cleaned in a typical flux-cleaning solvent and rinsed in isopropyl alcohol. These detectors failed the connectivity test badly, having many channels either open or at very high (~ 100 KOhms) resistance. This problem was cured for some channels by applying a voltage (~5V) over the bumps. But the cure was short lived on most cured channels and in same cases not reproducible. The detectors were visibly messy with stains of flux and cleaning procedure. Therefore we think that the residuals of flux and cleaning solvent are causing the open and high resistance bump connections. After testing six of these detectors, we discontinued the test and focused on the tests of the fluxless detectors.

5. Conclusions

Indium bump bonding is proven to be capable of successful fabrication at 30 micron pitch and small sizes. We observed high yield ($3x10^{-4}$ failure/bump) with gold metalization, but unpredictable and unacceptable results with aluminum metalization due to oxidization of aluminum pad and insufficient removal of the oxide layer. The indium bump resistance was measured to be ~1-2 Ohms. The oxidation effect is eliminated by applying a voltage across the bumps. Solder bumps at 50 micron pitch yielded much better results with the fluxless PADS processed detectors than the detectors produced with flux. The latter procedure produced a lot of visible residue and an unacceptable rate of open and high resistance bumps. The PADS process yielded a failure rate of $4.5x10^{-4}$ per bump and a bump resistance of much less than 1 Ohm. This is adequate for our needs and our tests have validated it as a viable technology. The test results and procedure helped us to identify problematic areas in the assembly, and have led to a validation procedure for process and vendors. A common problem to both technologies is the removal of the oxide on the Al pads. This has to be done thoroughly by careful sputtering.

Acknowledgments

We wish to thank Zaheed Karim of Advanced Interconnect Technology Ltd. (AIT); Richard LaBennett, Phil Deane and Sundeep Nangalia of MCNC for useful discussions.

References

[1] Proceedings of PIXEL 98, Fermilab-CONF-98/196. Ed. D. Anderson and S. Kwan.
[2] Fluxless No-Clean Assembly of Solder Bumped Flip Chips, N. Koopman, S. Nangalia, V. Rogers, presented at 46th ECTC'96, Orlando, Florida, May 28-31, 1996.

Table 1
Characteristics of indium and solder bumps.

Technology	Indium Bumps	Pb/Sn Bumps
Melting Point	156 ^{o} C	Varies. Eutectic: 183 ^{o} C
Minimum Bump Size	12 microns	15 microns
Minimum Bump Height	8-10 microns	15 microns
Minimal Pitch Available	18 microns	20 microns
Bump Resistance	1-2 Ohms	2-3 microOhms
Mechanical Strength	Low	High

Table 2
Parameters of the dummy detectors used in the test.

Vendor	No of Detectors	Pitch (Micron)	Bump Material	Base Metal	No of Channels
AIT	76	30	Indium	Aluminum	200
AIT	25	30	Indium	Gold	200
MCNC	82	50	Solder(fluxless)	Aluminum	196
MCNC	38	50	Solder(fluxed)	Aluminum	196

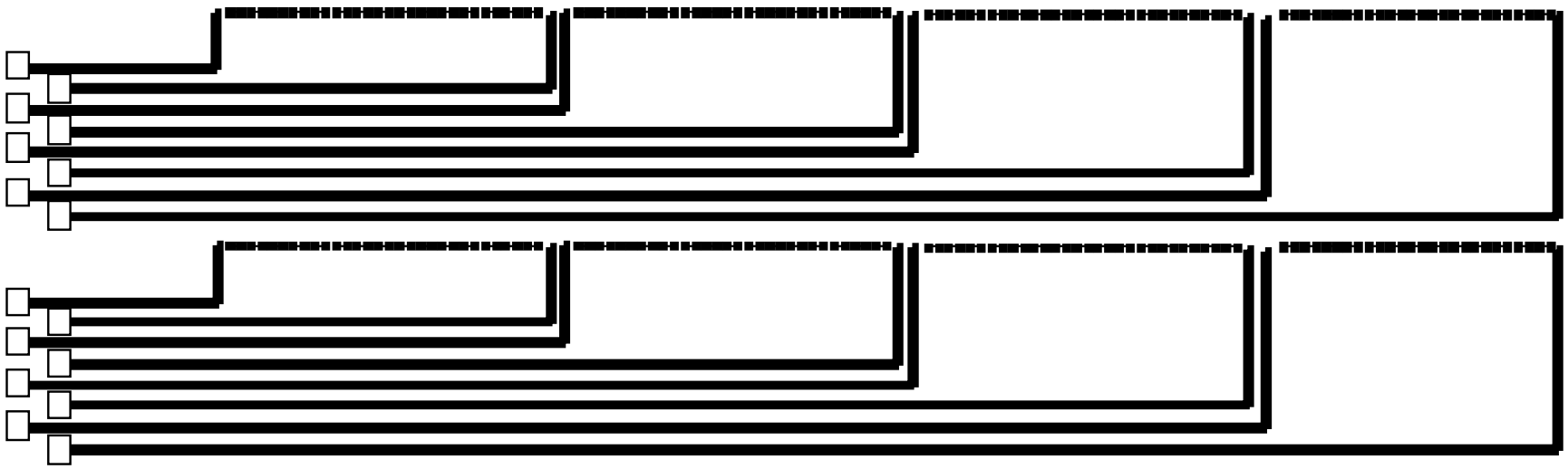

Fig. 1) Schematic layout of a portion of an AIT detector.

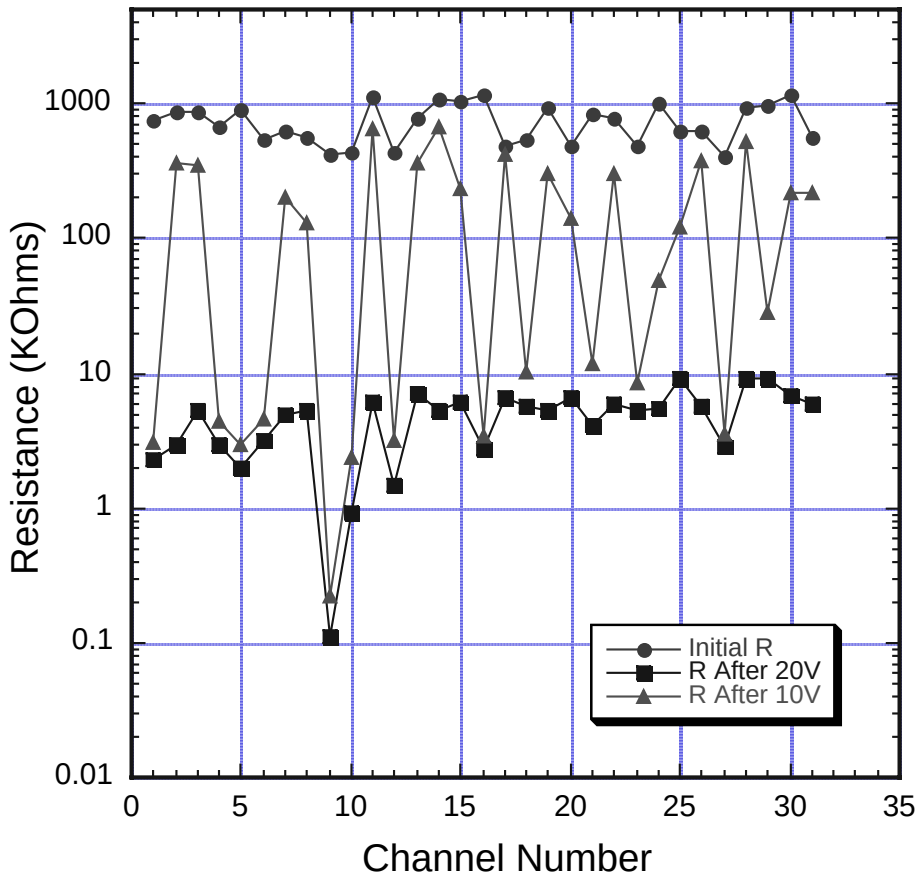

Fig. 2) Resistance of some channels of daisy-chained indium bumps on AIT detectors with Al metalization before and after applying various voltages.

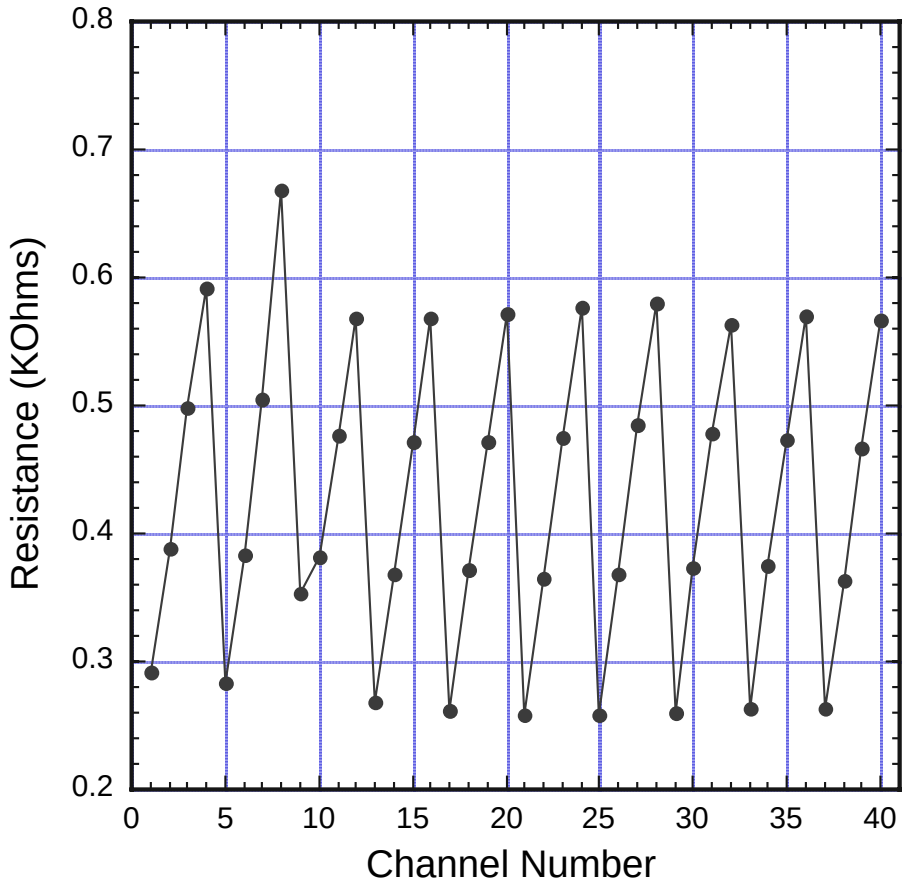

Fig. 3) Resistance of some channels of daisy-chained indium bumps on an AIT detector with Au metalization.

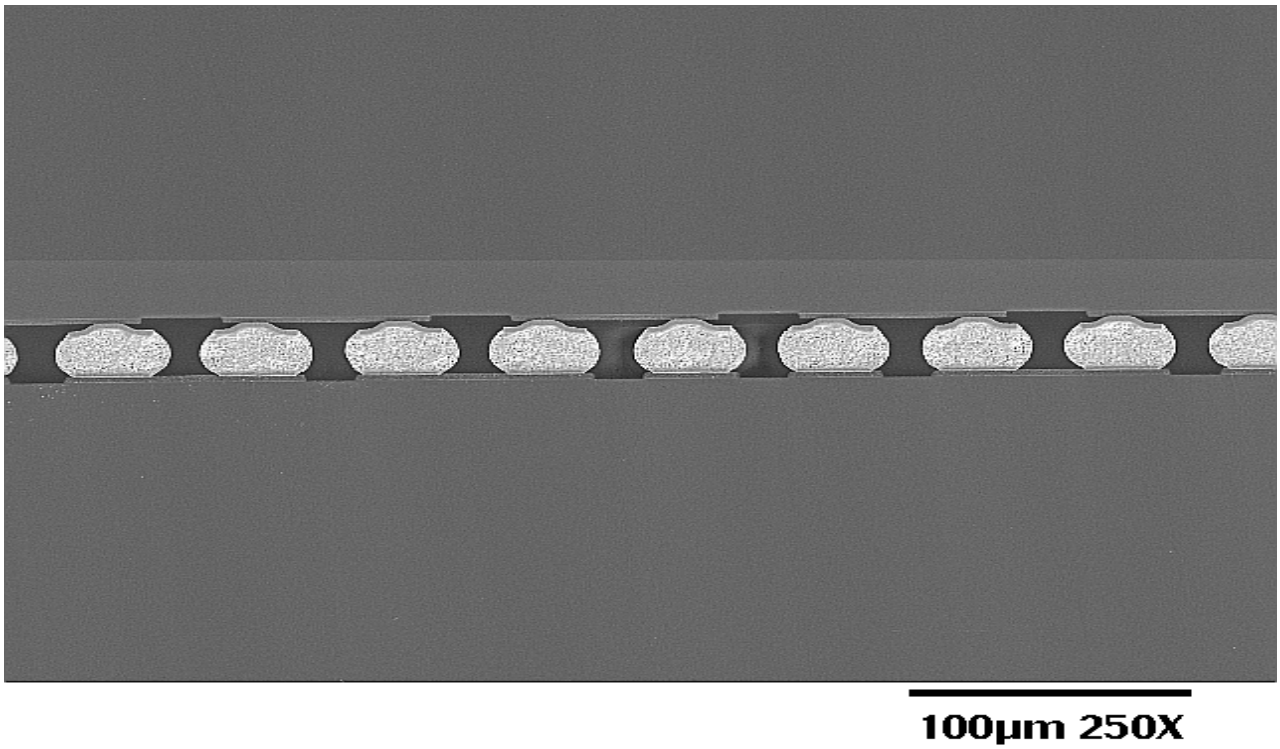

Fig. 4) A scanning electron micrograph of the solder bumps on a fluxless MCNC detector.

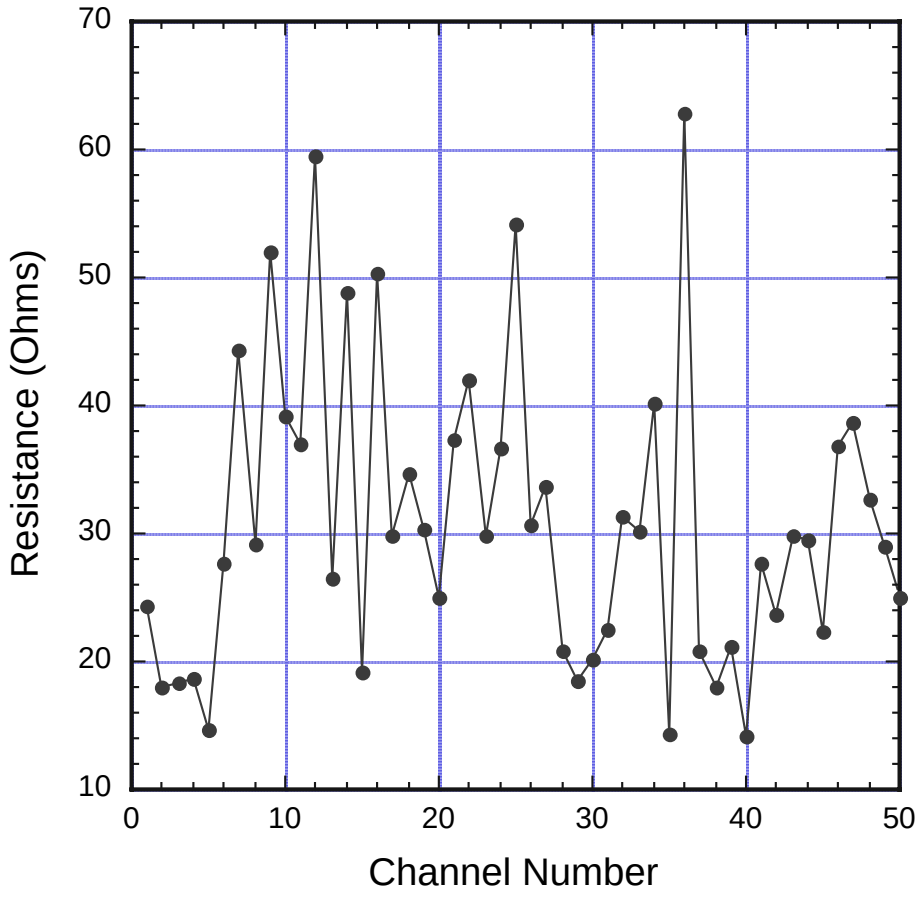

Fig. 5) Resistance of some channels of daisy-chained solder bumps on a fluxless MCNC detector.

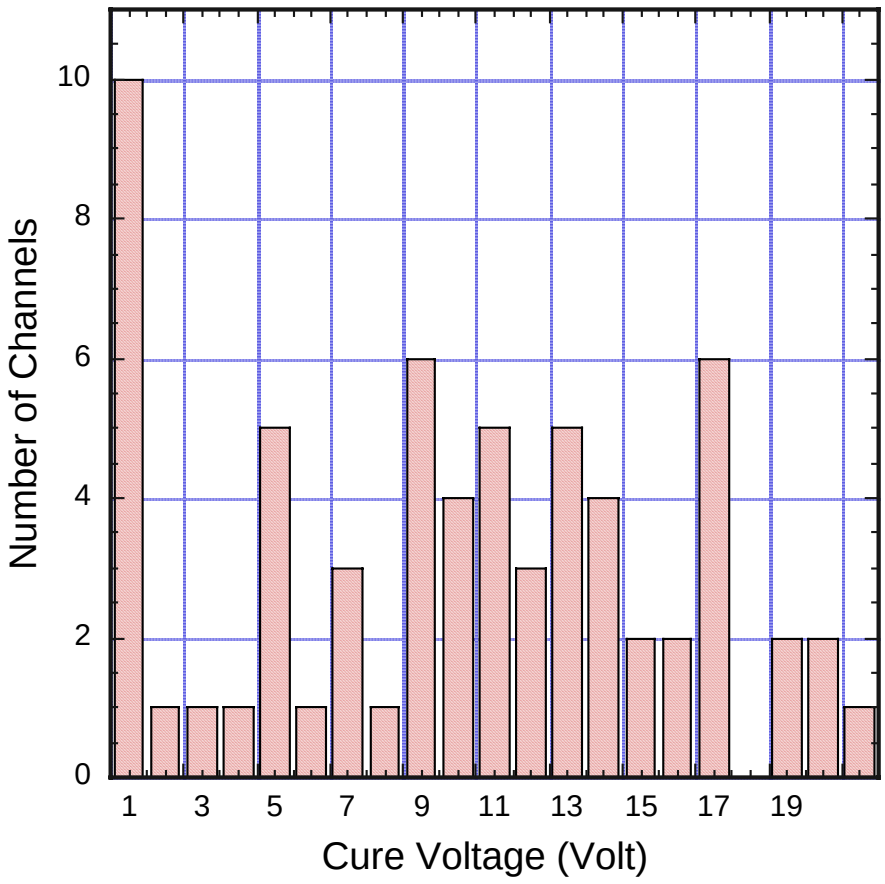

Fig. 6) Histogram of voltages that cured the open channels of MCNC fluxless detectors.

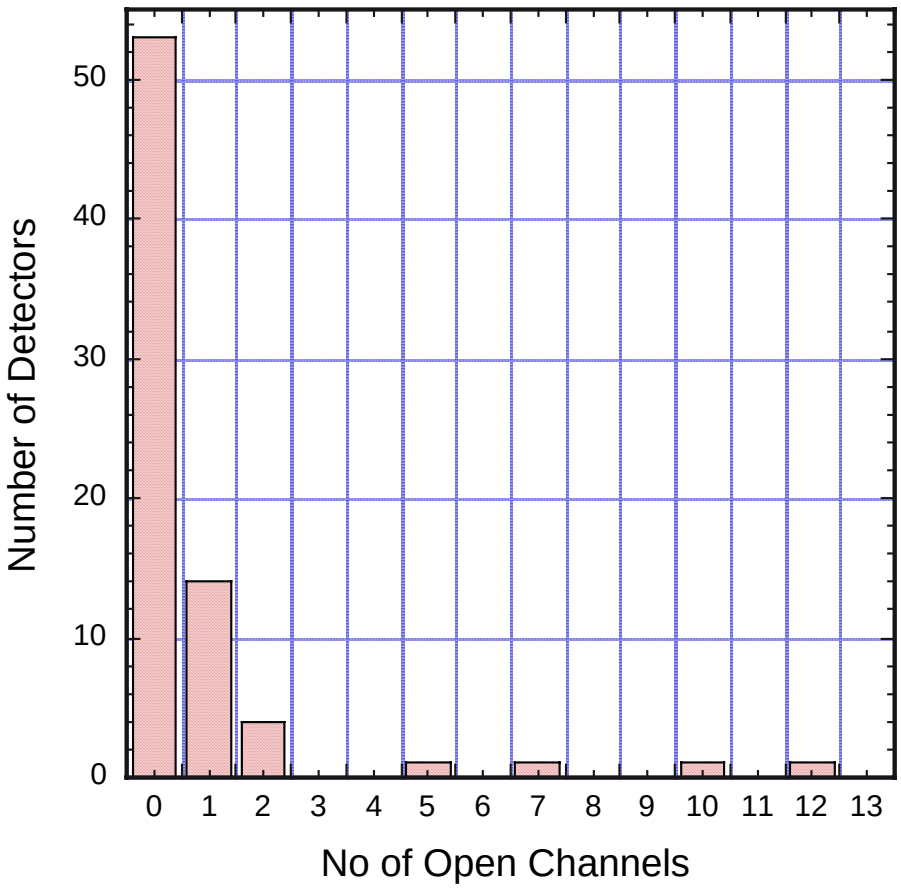

Fig. 7) Histogram of number of open channels of MCNC fluxless detectors.

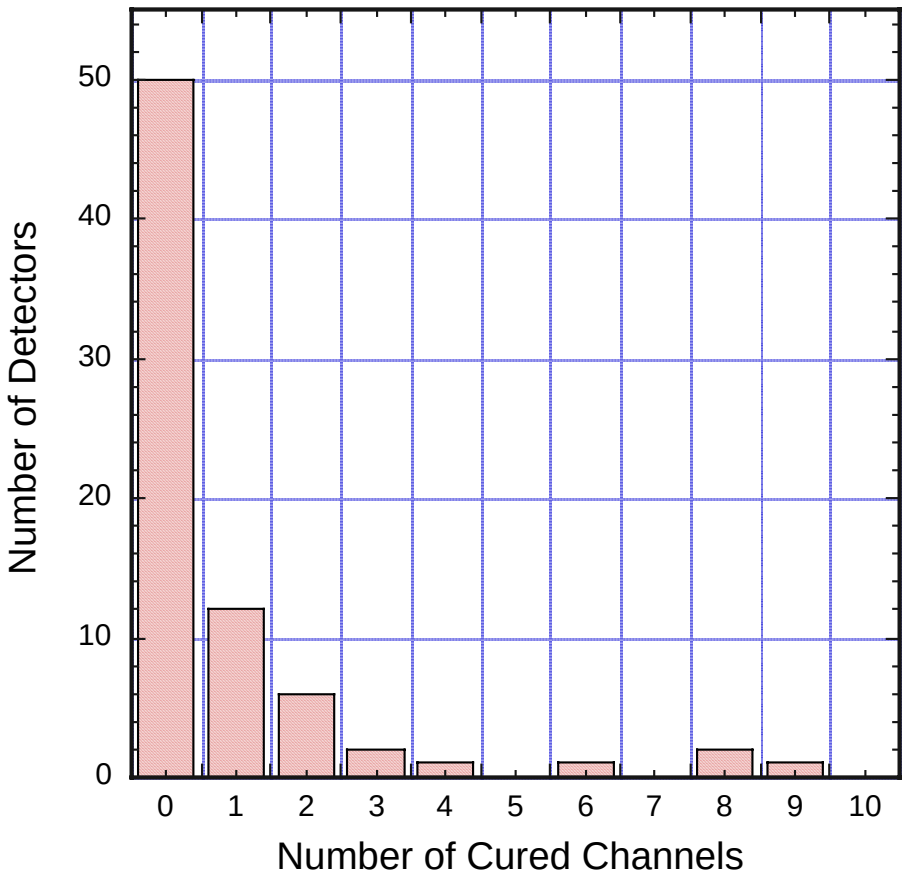

Fig. 8) Histogram of number of cured channels of MCNC fluxless detectors.