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Abstract

The worst case bias during total dose irradiation of partially depleted SOI transistors (from SNL and from CEA/LETI) is correlated to the device architecture. Experiments and simulations are used to analyze SOI back transistor threshold voltage shift and charge trapping in the buried oxide.

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I. Introduction

The last two years have seen the development of SOI technologies for high performance and low power circuits addressing the growing market of communication, fast computers and consumer electronics [1]. SOI is used by several companies to improve their product characteristics [2, 3]. SOI is also referenced in the 1999 international roadmap of semiconductor technologies. This evolution of SOI from military and space market to mainstream applications has been possible thanks to the drastic improvement of the SOI substrate quality which allows yield improvement and cost reduction for complex circuits.

However, civil SOI technologies are not fully adapted to hardened applications. The buried oxide isolation and the small volume of silicon present many advantages for speed, density, and transient irradiation [4]. But, unless radiation hardened [5], the buried oxide also induces total dose leakage currents [6].

Worst-case bias conditions have been partially described in Ref. [5] for 0.35µm gate length transistors processed on standard SIMOX. Extrapolation to other gate lengths and buried oxide thicknesses has only been studied with device simulation without modeling the dose induced charge trapping in the buried oxide. The purpose of this paper is to determine the worst-case bias of un-hardened SOI NMOS transistors through extensive experimental analysis. Simulations of the total dose trapping in oxide, and comparison of two different SOI technologies will also be used to show the influence the SOI process and architecture.

II. Device and Experiment Description

The studied NMOS/SOI transistors are fabricated either by CEA/LETI, or by Sandia National Laboratories (SNL). The technologies are both partially depleted, but they show different features, like gate length, buried oxide and silicon film thicknesses. Table 1 summarizes the respective features of each technology. In particular, the CEA/LETI transistors are processed on both UNIBOND and medium SIMOX. The SNL transistors are processed on standard SIMOX.

Tested devices are either edgeless floating body transistors (without body tie), or transistors with external body contacts. They are irradiated with 10 keV X-rays at a dose rate of 1 krad(SiO_2)/s for CEA/LETI transistors and 1.667 krad(SiO_2)/s for SNL ones.

The bias conditions under irradiation are consistent with usual polarization of transistors in digital circuits (cf Table 2). They correspond to on-state (ON) and off-state (OFF) in inverter gate, and transmission-gate (TG) like access transistors in memory cells. We also tried to connect the source, drain, gate and body to 0V (0V all) and to the supply voltage (V_{DD} all) with the substrate grounded. It should be noticed that the supply voltage of the SNL technology is 5V, while the supply voltage of the CEA/LETI technology is 2V.

Table 1:
Main characteristics of the CEA/LETI and SNL SOI technologies.

Origin	CEA/LETI		SNL
type	partially depleted		partially depleted
isolation	LOCOS		shallow trench
silicon film thickness	0.1 µm		0.15 µm
minimum gate length	0.25 µm		0.5 µm
Supply voltage	2V		5V
Buried oxide	UNIBOND	medium SIMOX	standard SIMOX
Buried oxide thickness t_{BOX}	413 nm	140 nm	370 nm

Table 2:
Bias conditions under irradiation of the CEA/LETI and SNL NMOS/SOI transistors. The supply voltage V_{DD} is 5 V for SNL transistors, and 2 V for CEA/LETI ones. The transistors are either edgeless floating body (without body ties), or with external body contacts.

	source	drain	gate	body	substrate
ON	0V	0V	V_{DD}	0V	0V
OFF	0V	V_{DD}	0V	0V	0V
TG	V_{DD}	V_{DD}	0V	0V	0V
0V-all	0V	0V	0V	0V	0V
V_{DD}-all	V_{DD}	V_{DD}	V_{DD}	V_{DD}	0V

III. Experimental Results

The use of external body contacts and edgeless transistors avoids the appearance of lateral leakage current induced by trapping in LOCOS isolation [7]. Moreover, using LOCOS with body contacts prevents any interaction of the gate polarization on the buried oxide as occurs with mesa [8]. Furthermore, the front gate oxides of both technologies are thin enough to avoid any significant modifications of the front transistor characteristics. The front gate threshold voltage shift at 1 Mrad is lower than 10 mV for CEA/LETI transistors and 300mV for SNL ones. The source of leakage current comes from the threshold voltage shift of the back transistor due to charge trapping in the buried oxide. In the following, we concentrate on the buried oxide total dose behavior as a function of bias during irradiation and transistor geometry (gate length, buried oxide thickness).

A. Influence of Bias During irradiation

Fig. 1 shows the threshold voltage shift of the back transistor with different bias under irradiation on SNL transistors. The case V_{DD}-all induces the weakest shift. The polarization of the entire silicon film (source, drain and body) to a positive voltage drives the holes created during irradiation towards the back interface of the buried oxide, while electrons escape to the silicon film. Trapped holes near the back interface have a small electric influence on the silicon film and do not induce an important shift.

The ON case shows the same shift as the 0V-all case. This demonstrates that the threshold voltage shift of the back transistor only depends on the silicon film bias (source, drain, body), and is not influenced by the gate bias.

The TG case is the worst case bias up to 1 Mrad. At higher dose the TG curve saturates while the OFF curve shows a higher shift. The TG and OFF curves of the 0.6µm SNL NMOS cross each other precisely at 1 Mrad. This competition between OFF and TG will be investigated further by looking at the transistor architecture.

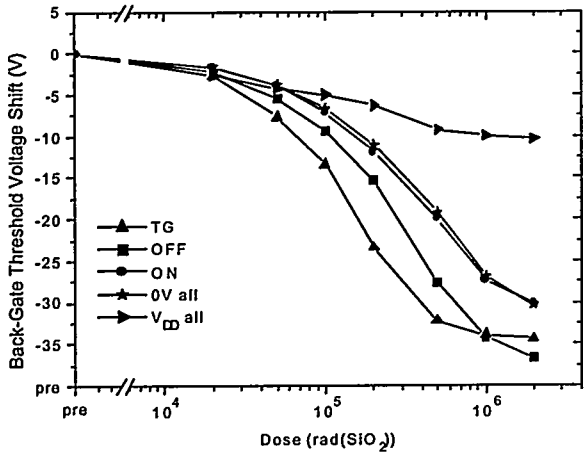

Figure 1 : Back gate threshold voltage shift versus dose of a 0.6µm gate length SNL NMOS/SOI processed on standard SIMOX with external body contacts. The back gate threshold voltage is extracted from Id-Vb characteristics at a drain voltage of Vd=1V.

B. Influence of Gate length

Fig. 2 shows the back transistor threshold voltage shift of CEA/LETI transistors with different gate lengths, irradiated in the TG configuration. The shift is strongly influenced by gate length with a maximum shift for the 0.6µm transistor. Shorter transistors (0.25µm) show a smaller shift with an earlier saturation. Longer transistors also show a smaller shift, but generally, as gate length increases, the saturation phenomenon seems to be postponed to higher doses.

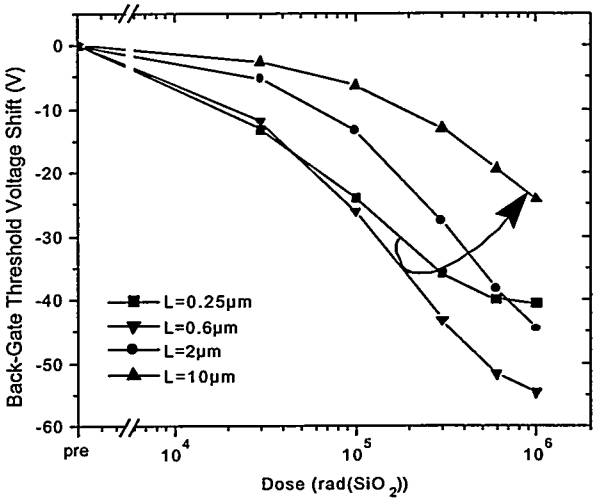

Figure 2 : Back-gate threshold voltage shift versus dose of CEA/LETI NMOS/SOI processed on UNIBOND with external body contacts and different gate length. The transistors are biased according to the TG case during irradiation The back gate threshold voltage is extracted from Id-Vb characteristics at a drain voltage of Vd=0.1V.

The back transistor threshold voltage shift at 1 Mrad is plotted on Fig. 3 for different bias conditions on CEA/LETI transistors with either floating body or external body contacts.

As expected, and already seen on SNL transistors (Fig. 1), the polarization of the silicon film at a positive voltage with the 2V-all case on transistors with body contacts (drain, body and source at 2 V) induces the weakest shift since trapping mainly occurs near the back interface of the buried oxide. The floating body transistors with the TG configuration have the same behavior. This is easily explained by the fact that the floating body potential is biased by the source and drain at 2V.

The cases ON and 0V-all for both types of transistors (floating body and body contacts) are quite similar since in both cases the entire silicon film is grounded. Trap sites are located in the volume of the buried oxide, and trapping is determined by built-in field and space charge effects as dose increases [9].

For the OFF case both transistors with floating body and external body contacts have the same behavior. This shows that the body potential of the floating body transistor is efficiently grounded by the source and that the potential distribution of both transistors are similar.

The TG case of the transistor with external body contacts is the worst case, except for the shortest gate length, 0.25µm.

The TG and OFF shift at 1 Mrad crosses at a gate length of 0.3µm. The same phenomenon (identical TG and OFF shifts at 1 Mrad) occurs on 0.3µm CEA/LETI transistors and on 0.6µm SNL ones (Fig. 1).

We can notice that adding body contacts to a transistor avoids lateral leakage, but induces the worst back gate threshold voltage shift to happen with the TG case for a wide range of gate lengtlis. For floating body transistors, OFF state is the worst case irradiation bias and TG case only induces a weak shift.

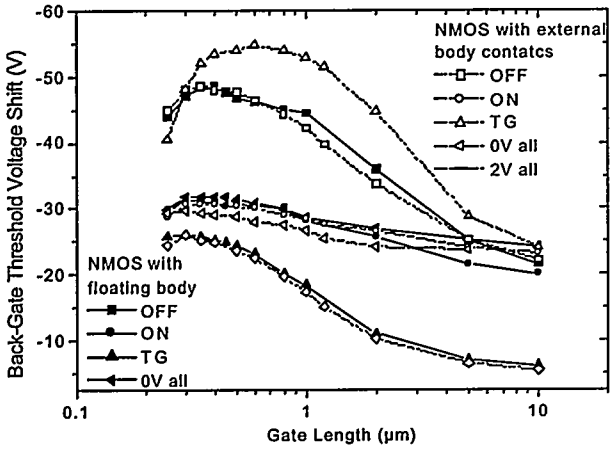

Figure 3 : Back-gate threshold voltage shift versus gate length of NMOS/SOI (UNIBOND) transistors measured on the Id-Vb characteristics at drain voltage of Vd=0.1V at a dose of 1Mrad(SiO_2).

C. Influence of Buried oxide thickness

Fig. 4 still shows the competition between TG and OFF for transistors with external body contacts. For the 0.25µm gate length transistor, OFF state is the worst case bias when processed on UNIBOND. However, if the transistor is processed on a thinner buried oxide (medium SIMOX), TG is the worst case.

IV. DISCUSSION

2D simulations with Dessis from ISE [10] are used to analyze hole trapping in the buried oxide during total dose irradiation. A specific module has been developed in cooperation with ISE, to self-consistently solve trapping equations with Poisson and carrier continuity equations in the oxide. It models the field collapse and enhancement effect [11].

Fig. 5 shows the trapped hole concentration in the buried oxide of a 0.5 µm gate length SOI/NMOS processed on 0.4µm thick buried oxide. In this simulation, only hole trapping is simulated since considered as the dominant phenomenon, especially at low dose, below 1 Mrad.

When a transistor with external body contacts is OFF biased, the field lines induce hole trapping near the back interface and under the body region, and few holes are trapped in the bulk of the oxide. Trapping at the back interface has a weak electric influence. However hole trapping under the body region determines back gate transistor conduction. The simulated 2D hole trapping configuration will help us to interpret the experimental data.

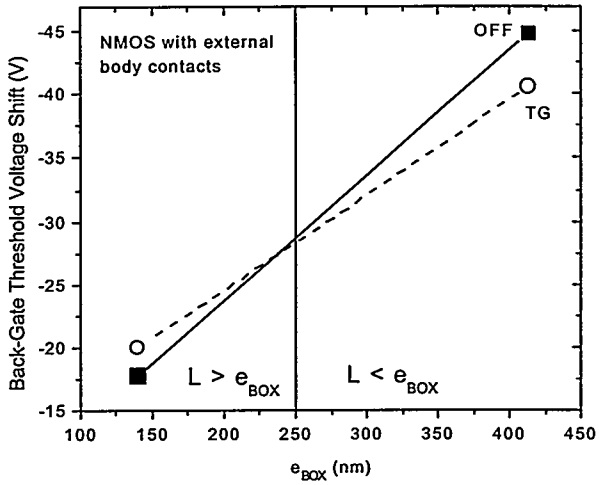

Figure 4 : Back-gate threshold voltage shift versus buried oxide thickness of 0.25µm gate length of NMOS/SOI transistors measured on the Id-Vb characteristics at a drain voltage of Vd=0.1V and at a dose of 1Mrad(SiO_2).

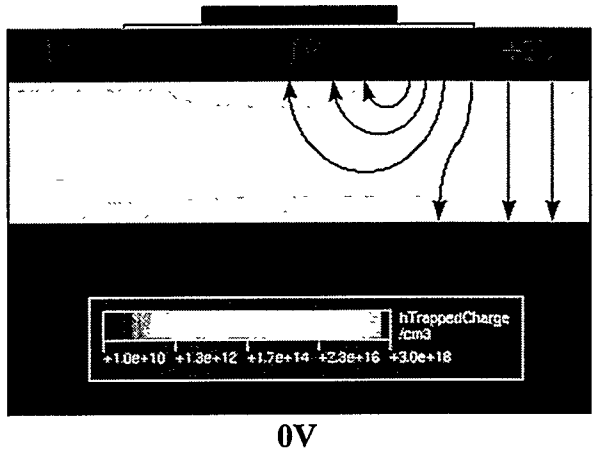

Figure 5 : Simulated hole trapping in the buried oxide of OFF biased NMOS/SOI transistors at 100 krad(SiO_2), and schematic field lines.

By comparing Fig. 3 and Fig. 4 it appears that OFF state is the worst case bias for short gate length transistors processed on thick buried oxide. Otherwise TG is the worst-case bias configuration. This can be expressed by using the ratio gate length on buried oxide thickness L/t_{BOX} [11] : if $L/t_{BOX} \ll 1$, OFF state is the worst-case; if $L/t_{BOX} \gg 1$, TG is the worst-case. Furthermore, both TG and OFF curves versus gate length (Fig. 3) show a maximum value, at about 0.3-0.4 µm for OFF ($L/t_{BOX} \approx 1$), and 0.5-0.8 µm for TG ($L/t_{BOX} \approx 1.5$), and a strong decrease at longer gate length.

Fig. 6 shows schematic field lines and hole trapping in SOI devices with varying L/t_{BOX} ratio in the OFF configuration. If $L/t_{BOX} \approx 1$, field lines turn up from the drain to the body, and trapping occurs with a maximum electrostatic efficiency under

the body which induces an inversion layer at the back interface of the silicon film and a parasitic back transistor conduction.

If $L/t_{BOX} >> 1$, trapping occurs mainly below the drain region where the electric field drop is maximum. But under the body, far from the drain, a region of low field prevents high trapped hole concentration. This 2D effect in long gate length transistors makes them less sensitive to total dose than short gate length transistors (Fig. 2 and Fig. 3).

If $L/t_{BOX} << 1$, the back transistor threshold voltage shift decreases. This can be explained by considering that the neutral part of the body is reduced as gate length decreases, while the body-drain space charge region due to the polarization of the drain during irradiation remains roughly unchanged. The field lines turn up towards the neutral region of the body tends to be less important. This phenomenon occurs at longer gate length for TG than for the OFF case ($L \approx$ 0.5-0.8µm instead of 0.3-0.4µm with UNIBOND wafers). The TG configuration implies that both drain and source are biased at V_{DD}, while the body is grounded (symetric configuration). In the TG case, the neutral body is then still more reduced to the benefit of the body-source and body-drain space charge regions than in the OFF case.

The transition point, where the TG curve crosses the OFF one at 1 Mrad (cf Fig. 3), occurs at a gate length of 0.3µm on the CEA/LETI transistors. The same crossing point between the TG and OFF curves occurs on the SNL transistors for a 0.6µm gate length transistor at the precise dose of 1 Mrad on Fig. 1. This points out the difference between the two processes with different 2D doping profiles. The ratio L/t_{BOX} describing the OFF and TG behaviors must be adapted to each technology since L can not be simply defined by the front transistor gate length, but rather by the back transistor effective gate length.

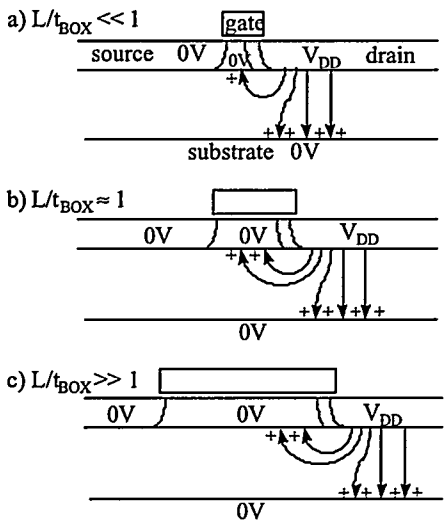

Figure 6 : Schematic representation of field lines and hole trapping in the buried oxide of NMOS/SOI transistors with varying L/t_{BOX} ratio. The transistors are biased according to the OFF case during irradiation

V. CONCLUSION

In this paper, we determine the worst-case bias during total dose irradiation on SOI technologies as a function of their architecture. For floating body transistors, off-state (OFF) is the worst-case whatever the gate length. For transistors with grounded body, transmission-gate (TG) is the worst-case except when the gate length is short compared to the buried oxide thickness. The transition between TG and OFF as a worst case depends on the body doping profile which determines the back transistor effective gate length. The final article will contain extensive simulations of charge trapping in the buried oxide during irradiation in OFF and TG configurations.

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