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The LANL Neutron-Science-Center Time-of-Flight/Position-Sensitive-Detector Module: Status and Progress

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Abstract

This paper describes the progress and current status of a joint collaboration between Argonne National Laboratory (ANL) and the Los Alamos National Laboratory (LANL) Manuel Lujan Neutron Science Center (MLNSC) to develop and implement a Time-of-flight (TOF)/Position-Sensitive-Detector (PSD) VXI-based C-size neutron-event data-collection module.

The LANL module, based on the ANL-developed hardware which uses field-programmable gate arrays (FPGAs) and analog-input-signal conditioning modules for a flexible topology capable of accepting either eight or 16 input channels, has been programmed and modified to incorporate more LANL-specific features such as improved peak detection, 24-bit time stamps, and 16-bit channel identification numbers which are all part of a 64-bit event record (2 by 32-bits wide). Using a backplane 10-MHz clock, timing resolution is ± 50 ns. The module uses two, frame first-in-first-out buffers (FIFOs), each 2-kwords deep, to accumulate event data at up to 330 kEvents/sec during a frame until the host computer can read it out. One FIFO is read while the other is being filled.

The module does not use the ANL token-passing configuration for accessing data. Rather, it uses direct logical-address and register-based addressing modes. To interface with analog signals from the neutron detectors, the module incorporates eight 72-pin single-inline-memory-module-size plug-in boards, called SIMs, which contain differential receivers, analog threshold comparators, and 8-bit analog-to-digital converters. A total of 16-analog channels are available if used in TOF mode, or eight channels if used in PSD mode.

I. INTRODUCTION

The Los Alamos Manuel Lujan Center and Argonne National Laboratory both have facilities for neutron generation, detection and related data acquisition systems. Given this common interest, a joint collaboration was formed to develop neutron time-of-flight (TOF) and position-sensitive-detector (PSD) VXI modules for use with neutron instruments. Argonne had developed a VXI module using Field-Programmable-Gate-Arrays (FPGAs) that met ANL's but not LANL's specific needs. Thus, the joint effort has been to use the ANL hardware and reprogram the FPGAs to meet LANL's requirements. These requirements are described in this paper as well as a description of the module, the SIMs, and the overall performance to date.

II. MODULE DESCRIPTION

A simplified block diagram of a TOF/PSD module is shown in figure 1. The board contains sockets for up to eight daughter-card Single-Inline-Modules (SIMs), a total of 16 channel-FPGAs designated as even and odd channels, even- and odd-frame FIFO buffers each 32-bits wide by 2k deep, a Readout-Control (RDC) FPGA, a VXI-interface FPGA, and miscellaneous interface and control circuitry. Each system-wide T-zero pulse toggles data operations such that one FIFO, either the even or the odd, is loaded with event data during the frame while the other is being read by the host computer.

Figure 1 Simplified block diagram of the TOF/PSD module.

The VXI-interface XC5206 FPGA loads at power-up from an on-board programmable-read-only-memory (PROM) chip. Once programmed, the interface handles bus operations for A16/D16 and A16/D32 register-based modes. Registers within the VXI-interface address space also are used to upload to the RDC and channel FPGAs, select channels, write to the 32 12-bit DAC channels, and control bus interface functions such as enabling the input TTL trigger lines. Normal VXI read and write operations are A16/D16 but when reading the FIFOs containing event data, the reads are performed in A16/D32. After power up, the host CPU loads the RDC and channel FPGAs according to the desired mode—TOF or PSD.

The RDC FPGA generally controls all operations with the frame FIFOs such as reset operations, writing and reading them.

The channel FPGAs, numbered 0 through 15, are programmed with all the even channels the same, all the odd the same, or both even and odd the same.

A. TOF Mode

In TOF mode, the even and odd channel FPGAs are each programmed with identical code and each channel operates independently of the others. In this mode, an event on a SIM triggers its respective channel FPGA. The channel FPGA generates a time stamp, reads the value from the SIM's on-board ADC, compares the digital value to a digital threshold value, and if less than this limit, sets a data_available flag for the RDC FPGA indicating valid data is available to be moved to the frame FIFO.

The RDC FPGA uses a priority decoding scheme to read the channel FPGAs with channel zero being the highest priority. Upon receipt of a data_available signal, the RDC selects the appropriate channel FPGA, then clocks out two words from it into the frame FIFO. If other channels have asserted their data_available lines, then the RDC sequentially selects them based on priority level and clocks out their data to the frame FIFO. This process continues until all the channels have their data moved to the frame FIFO.

B. PSD Mode

In PSD mode, the even and odd channel FPGAs are loaded with different configurations. All the even channels are programmed identically with one set of instructions and all the odd channels are programmed identically in another way. In this mode, each SIM operates with one even/odd-channel FPGA pair to handle events and alert the RDC that data is available.

When an FPGA pair has data available, it operates in the same fashion as the TOF mode. The RDC reads the data available lines and moves data to the selected frame FIFO. In this mode of operation, there are only eight channels to read instead of the 16 for TOF mode.

III. SIM DESCRIPTION

The SIMs are based on the same-size footprint as the standard 72-pin single-inline-memory module. Each SIM contains two identical channels that can be configured to act independently as Time-of-Flight (TOF) channels or configured together to act as one Position-Sensitive-Detector (PSD) channel. A simplified block diagram of a SIM is shown in figure 2.

Figure 2 Simplified block diagram of a SIM.

The two channels on each SIM are identical and each consists of a high-speed differential receiver, a peak-detect circuit, an 8-bit ADC, and ADC reference, threshold and control signal lines. The top portion of the SIM is referred to as the A channel and the bottom is called the B channel.

When configured for TOF mode, the sum circuit is ignored and each channel acts independently in time and amplitude. If an input pulse exceeds its respective channel lower-level threshold value, it peak detects and holds the input pulse and sends an event signal to the channel FPGA.

When configured for PSD mode, the sum circuit is used to decide which events should be digitized and recorded. The SUM threshold must be exceeded in order for either channel to be peak detected and digitized.

The reference voltage on each ADC can be set and controlled by separate 12-bit DACs. Because of this, the effective gain of each SIM channel can be controlled and adjusted to compensate for gain errors in other parts of the system such as in the neutron detector tubes or the preamplifiers. In PSD mode, this ability to individually adjust the gains of each channel is particularly useful in calibrating the system.

IV. DATA STRUCTURE

The data structure for each PSD-type event consists of two 32-bit words as shown in figure 3.

Figure 3 Data structure for a PSD-type event.

The first word contains the value of the A-channel ADC, eight undefined bits, and 16-bits used for channel identification. The second word has the eight bits of the B-Channel ADC and 24-bits of time stamp. For a TOF-type event, the digitized ADC value is placed in both words

labeled ADC-A and B. With the 10-MHz backplane clock, timing resolution is ± 50 ns.

Position is calculated using the common algorithm, difference-over-sum as shown below.

$$position = \left(\frac{A - B}{A + B} \right) \times scalefactor \quad (1)$$

The difference-over-sum technique is one of several self-normalizing techniques used to measure position [1], [2], [3]. Although other techniques are algorithmically simpler, this function can be easily performed by the host processor in non-real time.

V. PERFORMANCE & RESULTS

The modules have been successfully programmed to operate in both TOF and PSD modes and in each case use the 64-bit, two-word format. In PSD mode, the position resolution has been calculated to be less than about 0.9 inches on 36-inch tubes. A typical position histogram is shown in figure 4.

Figure 4. Data showing PSD histogram for slits 14-inches apart.

The histogram shows accumulated events using two neutron-transparent slits one-inch wide, spaced 14-inches apart. The data were taken at a 20-Hz repetition rate using 36-inch tubes.

VI. CONCLUSIONS

The ANL/LANL VXi-based TOF/PSD module has been shown to be sufficiently flexible to be configured and programmed for either TOF or PSD mode. It has successfully taken data in both modes including writing data to the frame FIFOs containing channel ID numbers, both ADC values, and 24-bit time stamps.

The SIMs have successfully been tested and proven their ability to be configured via on-board jumpers to be either TOF or PSD mode compatible.

Plans for the TOF/PSD module include upgrading the frame FIFOs to units 4k deep instead of 2k deep and including two-deep FIFOs in each channel FPGA so as to

prevent lost or overwritten data in the channels while they are waiting to be read by the RDC.

VII. ACKNOWLEDGEMENTS

The foresight of the Argonne engineers and staff, Mr. Weizeorick and others, in designing a TOF/PSD module with a large amount of flexibility so as to be useful to many users for many purposes is to be commended.

VIII. REFERENCES

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