Nitrogen Passivation of the Interface States Near the Conduction Band Edge in 4H-Silicon Carbide

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ABSTRACT

This paper describes the development of a nitrogen-based passivation technique for interface states near the conduction band edge [$D_{it}(E_c)$] in 4H-SiC/SiO₂. These states have been observed and characterized in several laboratories for *n*- and *p*-SiC since their existence was first proposed by Schorner, et al. [1]. The origin of these states remains a point of discussion, but there is now general agreement that these states are largely responsible for the lower channel mobilities that are reported for *n*-channel, inversion mode 4H-SiC MOSFETs. Over the past year, much attention has been focused on finding methods by which these states can be passivated. The nitrogen passivation process that is described herein is based on post-oxidation, high temperature anneals in nitric oxide. An NO anneal at atmospheric pressure, 1175°C and 200-400sccm for 2hr reduces the interface state density at $E_c-E = 0.1\text{eV}$ in *n*-4H-SiC by more than one order of magnitude - from $> 3 \times 10^{13}$ to approximately $2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$. Measurements for passivated MOSFETs yield effective channel mobilities of approximately 30-35cm²/V-s and low field mobilities of around 100cm²/V-s. These mobilities are the highest yet reported for MOSFETs fabricated with thermal oxides on standard 4H-SiC and represent a significant improvement compared to the single digit mobilities commonly reported for 4H inversion mode devices. The reduction in the interface state density is associated with the passivation of carbon cluster states that have energies near the conduction band edge. However, attempts to optimize the the passivation process for both dry and wet thermal oxides do not appear to reduce $D_{it}(E_c)$ below about $2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ (compared to approximately $10^{10} \text{cm}^{-2} \text{eV}^{-1}$ for passivated Si/SiO₂). This may be an indication that two types of interface states exist in the upper half of the SiC band gap – one type that is amenable to passivation by nitrogen and one that is not. Following NO passivation, the average breakdown field for dry oxides on *p*-4H-SiC is higher than the average field for wet oxides (7.6MV/cm compared to 7.1MV/cm at room temperature). However, both breakdown fields are lower than the average value of 8.2MV/cm measured for wet oxide layers that were not passivated. The lower breakdown fields can be attributed to donor-like states that appear near the valance band edge during passivation.

INTRODUCTION

Silicon carbide, the group-III nitrides (GaN, AlN and BN) and diamond have great potential for semiconductor applications under extreme operating conditions (high temperature, high power, high frequency and high radiation). Diamond technology is presently embryonic, and GaN and AlGaN are direct gap semiconductors that promise improved performance for high frequency and blue-UV optoelectronic applications. Silicon carbide is the most developed of the wide gap semiconductors, and the 4H and 6H polytypes of SiC are commercially available in 5cm diameter wafers. Silicon carbide material properties [2] such as large band gap, high thermal conductivity, high breakdown field strength and high saturated electron drift velocity make this semiconductor ideally suited for applications where high temperature, high power and high radiation must be considered. The 4H polytype has a larger band gap energy and a higher, more isotropic electron mobility, and is therefore the polytype of choice for high power applications.

Silicon carbide is the only wide band gap semiconductor that has a native oxide. Device-quality silicon dioxide can be grown on SiC using techniques that are basically the same as those used to grow SiO₂ on Si. Compared to the other wide gap materials, this native oxide makes SiC much more attractive for the fabrication of MIS (metal-insulator-semiconductor) devices. Silicon carbide *n*-channel inversion-mode MOSFETs have been fabricated with both the 4H and 6H polytypes. Blocking voltages for 4H-SiC MOSFETs have been improved significantly over the past 10 years; however, almost no progress has been made in reducing the on-resistance of these devices. The on-resistance for a vertical power MOSFET is the sum of the source/drain contact resistance, the resistance of the inversion channel layer and the resistance of the lightly doped drift region. The on-resistance is currently dominated by the inversion channel resistance that is high because of a low channel mobility. The high channel resistance severely limits the current handling capability (and as a result the power handling capability) of the device.

The poorer performance of 4H-SiC MOSFETs has been linked to a large, broad interface state density located at approximately 2.9eV above the valence band edge. This interface state density exists in all the polytypes of SiC [1]. For 6H-SiC ($E_{\text{gap}} \sim 3\text{eV}$), these localized states lie mostly in the conduction band, and hence have little effect on inversion channel mobility. However for 4H-SiC ($E_{\text{gap}} \sim 3.3$), the interface states lie mostly in the band gap where they act to reduce channel mobility through field termination, carrier trapping and Coulomb scattering. High integrated interface state densities the order of 10^{13}cm^{-2} have been observed for both *n*- and *p*-4H-SiC [3-5]. These states are believed to result from carbon clusters that remain at the interface and defects in a near-interface sub-oxide that are produced when the oxidation process is terminated [6,7]. This defect density may be compared to a defect density of approximately 10^{10}cm^{-2} that is routinely achieved for Si/SiO₂. Assuming an inversion channel depth of 10nm and an inversion channel carrier concentration of 10^{19}cm^{-3} for two MOSFETs, one Si and one SiC, the surface carrier concentration in the channel during device operation (i.e., in inversion) is approximately 10^{13}cm^{-2} for both devices. It follows therefore that, for any assumed trapping efficiency (1carrier/trap, 0.5 carriers/trap, etc.), carrier trapping is a much more serious problem for SiC MOSFETs than for Si devices. Carrier trapping lowers channel mobility and results in a reduced current handling capability for the MOSFET.

A number of different approaches have been undertaken to improve the *n*-channel mobility for 4H-SiC MOSFETs. Sridevan, et al. [8] reported effective mobilities as high as $128\text{cm}^2/\text{V-s}$ for deposited oxides that were annealed sequentially in wet nitrogen at 1100°C , Argon at 1100°C

and wet nitrogen at 950°C. However, these results have not been widely duplicated. Ogino, et al. [9] used low dose nitrogen implants in the *n*-channel region to control threshold voltages and reported higher mobilities ($\sim 99\text{cm}^2/\text{V}\cdot\text{s}$) following implantation. Promising results have also been obtained Yano, et al. [10] who reported effective channel mobilities of approximately $30\text{cm}^2/\text{V}\cdot\text{s}$ and low field mobilities of around $90\text{cm}^2/\text{V}\cdot\text{s}$ following oxidation of the (11 $\bar{2}$ 0) surface (the a-face) of 4H-SiC. (The low field mobilities were calculated using analysis techniques that eliminate the source/drain contact resistance as a source of error [11]). However, a problem with this approach is that a-face wafers are not currently available as standard items from commercial suppliers.

Li et al. [12] reported improvements in the interface characteristics of 6H-SiC MOS capacitors following high temperature anneals in nitric oxide (NO). We have applied similar techniques to 4H-SiC to develop a passivation process that reduces the interface state density near the conduction band edge by more than one order of magnitude for *n*-4H-SiC MOS capacitors [13]. This process is described in this paper together with results [14] that show that nitrogen passivation improves the effective channel mobility by factors of $\times 10$ - $\times 15$ for lateral, *n*-channel MOSFETs fabricated with standard 4H-SiC.

We have also carried out passivation anneals with ammonia (NH₃) and forming gas (N₂/5% H₂). Anneals in forming gas at temperatures up to 1000°C resulted in an improvement of about a factor of two for D_{it} at $E_c - E = 0.6\text{eV}$; however, at 0.15eV below the conduction band edge, no noticeable improvement was observed. Ammonia appears to be just as effective as NO in reducing $D_{it}(E_c)$ [15]; however, breakdown field strengths were found to be much lower for oxide layers passivated with NH₃. We attribute the lower breakdown field strengths to the fact that nitrogen appears uniformly throughout the oxide layer as well as at the SiC/SiO₂ interface following NH₃ anneals, while nitrogen accumulates almost entirely at the interface following NO passivation anneals [16]. Furthermore, for similar anneal conditions, the amount of incorporated nitrogen is approximately 100 times higher for NH₃ compared to NO. Considering both interface state passivation and oxide breakdown, we have achieved our best results using nitric oxide. The results of our NO passivation studies for 4H-SiC/SiO₂ are described in the remainder of this paper.

EXPERIMENTAL PROCEDURE

Epitaxial layers grown by Cree Research, Inc. on standard 4H-SiC wafers were used for studies of *n*-4H MOS capacitor and *n*-channel 4H MOSFETs. The nitrogen doping concentration and epilayer thickness were $8 \times 10^{16}\text{cm}^{-3}$ and $5\mu\text{m}$ for the MOS capacitors, and mobility measurements were made for lateral MOSFETs fabricated by dry oxidation of $10\mu\text{m} / 8 \times 10^{16}\text{cm}^{-3}$ epilayers and wet oxidation of $3\mu\text{m} / 1 \times 10^{16}\text{cm}^{-3}$ epilayers – both doped with Al. Prior to oxidation, all samples were cleaned using procedures that have been described previously [17]. Oxide layers with thicknesses typically between 40 and 80nm were grown in a high-purity quartz tube using standard thermal oxidation techniques and the procedures shown in Fig. 1. These procedures include the use of an H₂O bubbler (85°C, $\frac{1}{10}$ of the O₂ flow), a TCA bubbler (23°C, $\frac{1}{10}$ of the O₂ flow) for control of mobile ions in the oxide layers and a “re-oxidation” step for the termination of the oxidation process. Re-oxidation effectively reduces the interface state density near mid-gap [18,19]. Dry oxides were grown using the same procedures shown in Fig. 1, except that the TCA and H₂O bubblers were bypassed.

Figure 1. Standard thermal oxidation process. The TCA bubbler is used to control mobile ions that sometimes appear in wet oxide layers in spite of our best efforts to prevent such contamination. Dry oxides are grown using the same process conditions except that the H_2O and TCA bubblers are bypassed.

MOS capacitors were characterized using standard high-low (1MHz-quasistatic) C-V techniques applied at room temperature for measurements near the conduction band edge and at 320°C for measurements of D_{it} deeper in the band gap. Sputtered Mo was used for 350 μ m diameter gate contacts and large area (> 25mm²) backside contacts were formed on the n^+ -substrates using Ag colloidal paste. Capacitance-voltage measurements of the distribution of interface states near the conduction band edge were verified for several samples by conductance measurements performed at Purdue University and Cree Research.

Lateral MOSFETs were fabricated with both wet and dry oxides. Forty nanometer wet oxides were grown and passivated on whole wafers provided by Cree ($N_a = 1 \times 10^{16} \text{cm}^{-3}$). Source/drain nitrogen implants on these wafers had been previously activated at Cree with 3hr anneals at 1200°C in Ar. After oxidation and passivation, Mo was sputter-deposited over the whole epilayer surface, and the wafers were returned to Cree for processing and characterization. The Mo layer was patterned to form 250 μ m x 250 μ m gate contacts. Long channel lengths and a “fat FET” design (i.e. large S/D dimensions) were used to minimize the source/drain resistance relative to the channel resistance. The source/drain contacts were not annealed prior to characterization.

MOSFETs with dry oxides were processed entirely at Auburn using 10 μ m p^- -epilayers. Prior to oxidation, nitrogen source/drain implants were annealed at 1575°C for 30min inside a polycrystalline SiC pillbox in 1atm of flowing Ar. Devices were fabricated with a gate length of 120 μ m and source/drain dimensions of 200 μ m (length) x 400 μ m (width). After oxidation, Mo was sputter-deposited to form gate contacts, and Ni was deposited on the source/drain regions. However, as with the wet oxide devices characterized by Cree, the source/drain contacts were not annealed prior to making channel mobility measurements. Effective channel mobilities for both dry and wet MOSFETs were extracted from plots of drain current as a function of gate voltage for a fixed drain voltage of 50mV. Low field mobilities [10] were also computed in order to eliminate errors that affect the measured transfer characteristics [i.e., $I_d(V_g)$] when the “fat FET” design does not make the source/drain contact resistance small enough compared to the channel resistance of the device.

RESULTS

The distribution of interface states in the SiC band gap for 4H-SiC/SiO₂ is shown in Fig. 2 prior to any passivation anneal. Three observations are noteworthy. (1) The density of states is much higher near the conduction band edge than near the valance band edge. (2) The re-oxidation step that terminates the oxidation process is effective in reducing D_{it} near mid-gap for p -SiC. (3) Re-oxidation is not effective in reducing the trap density near the conduction band edge $D_{it}(E_c)$. We initiated the development of a nitrogen-based passivation process for $D_{it}(E_c)$ by concentrating on room temperature C-V measurements for n -4H-SiC/SiO₂ capacitors under the assumption that p -4H-SiC/SiO₂ has the same distribution of states near E_c . This assumption has recently been confirmed by direct measurement of $D_{it}(E_c)$ for p -4H-SiC [5].

Post-oxidation anneals in NO were carried out for various times and temperatures to optimize these parameters for the passivation process. Based on results similar to those shown in Fig. 3, our standard NO anneal is now performed for 2hr at 1175°C. The thickness of the original oxide layer increases by less than 10% [16] during the 2hr/1175°C passivation anneal, and $D_{it}(E_c)$ is a minimum for NO flow rates between about 200-400sccm. The complete anneal process is described as follows:

- NO purity ~ 99.5%.
- Insert sample at room temperature.
- Ramp at 17°C/min to 1175°C. Start 200-400sccm NO flow at 400°C.
- 2hr at 1175°C.
- Furnace off. Continue NO flow to 400°C.
- At 400°C, flush with Ar for 3min.
- Remove samples at 400°C.

Figure 2. High-low (1MHz-quasistatic) C-V measurements for n - and p -4H-SiC/SiO₂ following wet oxidation but prior to passivation with NO. Measurements near mid-gap were made at 320°C, and measurements near the band edges were made at room temperature.

Figure 3. Interface state densities measured during optimization studies for the NO passivation process. Measurements similar to these were used to develop a standard passivation anneal that is now conducted for 2hr at 1175°C in 1atm of flowing NO (200-400sccm).

The effect of the NO passivation process on $D_{it}(E_c)$ is shown in Fig. 4. The magnitude of the interface state density for n -4H-SiC is reduced significantly to a value that is “6H-like” following the anneal in NO. These results are in good agreement with the assertion by Schorner, et al. [1] that substantially more interface states exist in the upper half of the band gap for 4H-SiC than for 6H-SiC. We attribute the reduction in $D_{it}(E_c)$ to the passivation of carbon cluster interface states that have energies in the top half of the SiC band gap [13,20]. As illustrated in Fig. 5, nitrogen introduced during the NO passivation anneal reacts with the clusters to shift their energies into

Figure 4. The interface state density near the conduction band edge in n -4H-SiC/SiO₂ before and after nitrogen passivation. Results for D_{it} for n -6H-SiC/SiO₂ are also shown for comparison. The results for 4H and 6H-SiC are in agreement with the description of SiC/SiO₂ interface states in [1].

Figure 5. Nitrogen passivates carbon cluster states that have energy levels in the top half of the 4H-SiC band gap [6]. Passivation shifts the level energies to the bottom of the gap or into the valence where the effect of these states on channel mobility is negligible [13,20].

the lower half of the band gap. Near the valence band edge ($E - E_v = 0.1 \text{ eV}$), we have observed an increase in D_{it} from about $1.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ to approximately $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ following NO passivation. This is an indication that a significant portion of the passivated states have energies below the valence band edge, and as a result, have no effect on inversion channel mobility.

The effect of nitrogen passivation on the effective mobility of 4H MOSFETs is shown in Fig. 6 where a $\times 10$ - $\times 15$ improvement can be observed compared the single digit mobilities commonly reported for standard 4H devices. Considering the difference in epilayer doping concentrations - $8 \times 10^{16} \text{ cm}^{-3}$ (dry) and $1 \times 10^{16} \text{ cm}^{-3}$ (wet) - and the fact that measurements were made at Auburn for the dry oxides and at Cree for the wet oxides, the results do not appear to be significantly different. This observation suggests that a completely dry oxidation process may be used for MOSFET fabrication in order to take advantage of the higher breakdown voltage of dry oxides [20]. Low field mobilities [11] were also computed for the dry oxide MOSFETs. Results varied somewhat from device to device – perhaps as a result of the analysis technique. However, for four dry MOSFETs, an average low field mobility of $104 \text{ cm}^2/\text{V-s}$ can be compared to a peak effective mobility of about $30 \text{ cm}^2/\text{V-s}$. We have only preliminary results for mobility measurements above room temperature, and we have not yet accurately determined the effect of temperature on the effective mobility of passivated devices.

We have conducted a limited number of current-voltage measurements in order to study the effect of the passivation anneal on the breakdown characteristics of the oxide layers. Results are shown in Fig. 7. For wet and dry oxides on n -4H-SiC, the NO passivation anneal results in a significant improvement in breakdown performance at room temperature and at 290°C . For oxides on p -4H-SiC, the passivated dry oxides have higher average breakdown fields at room temperature and 290°C compared to the passivated wet oxides. However unlike n -4H-SiC, both average fields (wet and dry) for the passivated oxides on p -4H-SiC are lower compared to the average field of the corresponding unpassivated wet oxides. The lower breakdown fields for p -4H-SiC may be related to the introduction of positive oxide charge during the passivation anneal. For n - and p -MOS capacitors, we have observed that our C-V curves shift towards negative bias voltage following NO anneals [8]. For n -MOS capacitors, this shift is consistent with the removal from the upper half of the band gap of acceptor-like states that are filled (and therefore

Figure 6. The effect of nitrogen passivation on the effective channel mobility of lateral 4H-SiC MOSFETs fabricated with dry and wet oxides. Drain current - gate voltage characteristics for the wet oxide devices (right) and effective channel mobilities for the dry oxide MOSFETs (left) are shown before and after passivation with nitrogen. The peak effective mobility of approximately $30\text{cm}^2/\text{V}\cdot\text{s}$ for the passivated dry oxide may be compared to an average low field mobility of $104\text{cm}^2/\text{V}\cdot\text{s}$. (Wet oxide measurements courtesy M. Das, Cree Research).

negatively charged) in accumulation. If these states become donor-like when they are shifted to the lower half of the band gap, they will be filled and therefore uncharged in accumulation. However for p -MOS capacitors, acceptor-like states in the upper half of the gap are above the Fermi level in accumulation and are therefore uncharged. When these states are passivated (shifted to the lower half of the band gap), they remain above the Fermi level and act as a source of positive charge at the interface – if the states become donor-like states when they are passivated. According to Klein [21], positive charge in the oxide can produce field enhancement

4H-Sample	E_{bdwn} (MV/cm) @ $10^{-4}\text{A}/\text{cm}^2$			
	25°C		290°C	
N: Wet Reox	7.7 (0.5)	8.5	3.7 (0.03)	3.8
+ NO	9.9 (0.9)	9.7	5.4 (0.2)	5.6
N: Dry Reox	9.5 (0.7)		7.7 (1.3)	9
+ NO				
P: Wet Reox	8.2 (0.2)	8.6	7.8 (0.8)	8.6
P: Wet Reox	7.1 (2.0)	8.8	5.6 (1.5)	7.3
+ NO				
P: Dry Reox	7.6 (0.5)	8.3	6.3 (0.5)	7.2
+ NO

Figure 7. Breakdown characteristics for oxide layers on n - and p -4H-SiC. The breakdown voltage was defined as that voltage at which the measured current density reached $10^{-4}\text{A}/\text{cm}^2$. The voltages used to calculate the breakdown field strengths were corrected for flatband shifts. Field strengths are averages for measurements on 6-8 MOS capacitors, and the standard deviation σ was determined from the averaging process.

at the cathode (metal layer) of the MOS capacitor. Cathode field enhancement leads to increased carrier (electron) injection at the cathode and therefore to a higher probability for avalanche breakdown. The result is a decrease in the breakdown field strength of the oxide.

We have also processed n -4H MOS capacitors with a simulated source/drain ohmic contact anneal ($\sim 950^\circ\text{C}/3\text{min}$) in order to assess the effect of the contact anneal on the passivated interface. We observe an increase in $D_{it}(E_c)$ of about $\times 2$ following the contact anneal for MOS capacitors fabricated with wet and dry oxides. However, this increase can be avoided by using ONO (oxide-nitride-oxide) dielectric layers that have been developed recently [21] for SiC MOSFET applications. The ONO layers on p -4H-SiC were formed in the following manner. A thin (10nm) dry thermal oxide was grown and passivated with NO. Cree then deposited a 40nm Si_3N_4 layer using low-pressure CVD techniques. The nitride layer was subsequently oxidized with wet oxygen for 3hr at 950°C to grow an oxide layer of thickness 5-10nm on the surface of the Si_3N_4 . Note that the oxidation of the nitride layer subjects the passivated SiC/SiO₂ interface to the same conditions of time and temperature that are required for the formation of low resistance Ni_2Si source/drain ohmic contacts for n -channel MOSFETs.

Results for the ONO structures and the simulated ohmic contact anneals are shown in Fig. 8 where the legends indicate the order of processing for each MOS capacitor. For Fig. 8(a), we suggest that the nitride layer in the ONO structure prevents NO reaching the oxide-semiconductor interface during subsequent passivation anneals of structures that were not passivated prior to Si_3N_4 deposition. Likewise, the nitride layer prevents the loss of nitrogen from the passivated oxide-semiconductor interface during oxidation of the Si_3N_4 . Fig. 8(b) shows the effect of a simulated source/drain contact anneal ($950^\circ\text{C}/3\text{min}$ in Ar) on MOS capacitors fabricated with dry thermal oxides and ONO layers. Clearly the ONO layer prevents the tendency for $D_{it}(E_c)$ to increase during the anneal process. We would be concerned that an increase in $D_{it}(E_c)$ as the result of a source/drain contact anneal would cause a

Figure 8. (a) Interface state densities for dry thermal oxides and ONO layers on n -4H-SiC before and after NO passivation. The legend indicates the order of processing for each sample. (b) The nitride layer in the ONO structure prevents the loss of nitrogen from the interface during simulated source/drain ohmic contact anneals and thereby preserves the quality of the interface (i.e., maintains low D_{it}). (ONO layers courtesy L. Lipkin, Cree Research. See text for explanation of the ONO growth process).

corresponding decrease in channel mobility. However, we understand that contact anneals have recently been performed for FETs fabricated with passivated thermal oxides, and that mobilities similar to those shown in Fig. 6 ($\sim 30\text{cm}^2/\text{V-s}$) have been obtained [23]. This is good news and indicates that a decrease in mobility as the result of increasing $D_{it}(E_c)$ may be more than offset by an increase that is realized when the contribution to the total on-resistance from the source/drain contacts is reduced by the contact anneal. However, if the contact anneal eliminates the source/drain resistance (i.e., makes the S/D resistance negligible compared to the channel resistance), then the effective mobility measured for devices with annealed contacts would be expected to compare more favorably with the low field mobility measured for devices with non-annealed contacts. However, the peak effective mobility ($30\text{-}35\text{cm}^2/\text{V-s}$) reported herein is substantially lower than the low field mobility ($\sim 100\text{cm}^2/\text{V-s}$). Further work is necessary to understand the reasons for this difference and to ensure that proper analysis techniques are applied to extract mobility information from carefully designed devices.

CONCLUSIONS

A nitrogen-based interface passivation process has been developed for 4H-SiC MOSFETs. The process is based on post-oxidation, high temperature anneals in nitric oxide and results in a $\times 10\text{-}\times 15$ increase in the effective channel mobility for devices fabricated with either dry or wet thermal oxides. Peak effective mobilities of $30\text{-}35\text{cm}^2/\text{V-s}$ and low field mobilities of about $100\text{cm}^2/\text{V-s}$ are the highest yet reported for devices fabricated with thermal oxides and standard 4H-SiC. These results represent a significant improvement compared to the single digit mobilities commonly reported in the past.

Passivated dry oxides on *p*-4H-SiC have somewhat higher room temperature breakdown fields than do wet oxides, although both have breakdown fields that are slightly lower than the breakdown field strength for unpassivated wet oxides (and presumably for unpassivated dry oxides, as well). This observation is consistent with the introduction of positive charge at the *p*-4H-SiC/SiO₂ interface during the passivation anneal. For an accumulated *p*-MOS capacitor, the NO anneal turns uncharged acceptor-like states in the upper half of the band gap into positively charged donor-like states in the lower half of the band gap.

Ohmic contact anneals ($\sim 950^\circ\text{C}/3\text{min}$) that are required for power MOSFETs appear to drive nitrogen from the passivated oxide-semiconductor interface, thus resulting in an increase in the density of interface states near the conduction band edge and raising concerns about a corresponding decrease in channel mobility. However, this decrease may be compensated by an increase in the effective mobility that results from a lower source/drain contact resistance following the contact anneal. Furthermore, the oxide-semiconductor interface can be protected during the contact anneal by using ONO dielectric layers instead of pure thermal oxides. The nitride layer in the ONO structure acts as a diffusion barrier and prevents the loss of nitrogen from the interface during the contact anneal.

We have observed that, for dry oxides, wet oxides, thin oxides ($\sim 40\text{nm}$) and thick oxides (80nm), our optimized NO passivation process results in an interface state density of around $2 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$ for *n*-4H-SiC at $E_c - E = 0.1\text{eV}$. This interface state density may be compared to a trap density of approximately $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ for passivated Si/SiO₂. We must therefore consider the possibility that two kinds of interface traps exist in the upper half of the 4H-SiC band gap – one that is amenable to passivation, and one that is not. Further work is necessary to determine

conclusively whether a second distribution of states exists, and if so, to develop additional passivation techniques for use with or in place of the NO process.

ACKNOWLEDGEMENTS

This work was supported by DARPA Contract MDA972 98-1-0007 (program manager, Daniel Radack; technical program monitors, John Zopler and George Campisi) and EPRI Contract W0806905 (former program manager Jerry Melcher; current program manager, Ben Damsky; technical program monitor, Frank Goodman). The authors would like to thank Mrinal Das and Lori Lipkin at Cree Research for assisting with the mobility measurements and supplying the ONO structures and to acknowledge many helpful discussions with Jim Cooper at Purdue University and Anant Agarwal at Cree. Work done at Oak Ridge National Laboratory, which is managed by UT-Battelle, LLC, for the U.S. Dept. of Energy, was funded under contract DE-AC05-00OR22725.

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