Conceptual Design of the GEM Data Acquisition System

Superconducting Super Collider Laboratory
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CONCEPTUAL DESIGN OF THE GEM DATA ACQUISITION SYSTEM

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Abstract

The design of a large scale data acquisition system for the GEM detector at the Superconducting Super Collider (SSC) is presented. This architecture supports high-bandwidth data transfer using parallel point-to-point links and a scalable switching network. Substantial buffering enables the use of high latency, selective triggering based on either hardware or software implementations. The system throughput can be expanded to greater than 40 Gbps per second at trigger rates of 100 KHz.

I. INTRODUCTION

The GEM detector contains four major subsystems with a combined total of approximately 10,000 data sources. Compressed data is moved off the detector following the first-level trigger. Event sizes of 200–400 KBytes are expected, at a nominal trigger rate of 10–20 KHz, for a total bandwidth of less than 10 Gbps. However, a trigger rate of 100 KHz must be supported for future luminosity improvements. The data is transmitted via fiber-optic links to a group of 512 Data Collectors (Fig. 1), which buffer the events pending a decision by the second-level trigger. This trigger is initially implemented in software, in the same processor array used for third-level trigger analysis. Provision is also made for hardware or combined hardware/software implementations of the Level Two Trigger. Large buffers in the Data Collectors allow second-level trigger latencies of several hundred milliseconds, as compared to more traditional latencies of a few hundred microseconds.

Fig. 1. System Overview.

Data is transferred to the processor array through a modular switching network-based Event Builder. Although the Event Builder is scalable to the full Level One data bandwidth, a more economical mode of operation involves selective readout of data by the second-level algorithm based on categorical and spatial information from the first-level trigger.

A control network allows each processor to independently issue data requests to specific Data Collectors or predefined groups of Data Collectors. This selected data is then used in the second-level trigger, with the remaining data transferred only if the third-level trigger is invoked.

The key features of this system are the readout of all data following the Level One Trigger and the increase in second level trigger latency afforded by the large off-detector data buffers. This allows a range of Level Two Trigger implementations, including the use of general-purpose proces-
ors with access to all Level One data. The drawback is the increase in digitization rate and volume of data leaving the detector.

II. COMPONENTS

A. Data Links

All communication in this system is based on point-to-point serial data links. Data is transmitted directly from the front-end modules using 60-Mbps synchronous fiber links. Control signals are distributed to the front-end modules using similar fiber links.

After the data is multiplexed in the Data Collectors, transmission through the Event Builder and Data Distributors is handled by 1-Gbps serial links.

B. Data Collectors

The Data Collectors perform three important functions. First, they provide the local control and data multiplexing for a group of front-end modules. Secondly, they provide a large buffer space during the Level 2 Trigger decision. And finally, they provide the queuing and data packet ordering necessary for efficient utilization of the Event Builder.

C. Event Builder

The Event Builder is implemented as a simple, high-bandwidth synchronous time-division multiplexed (TDM) switch. The switch is modular, allowing expansion from the initial $512 \times 128$, 10 Gbps configuration to $512 \times 512$ and 40 Gbps (Fig. 2). Future versions of commercial ATM or Fibre Channel switches may also be suitable. With the exception of bandwidth, the requirements for a switching network used in event building are not as stringent as those of a general-purpose network since operation is inherently unidirectional and deterministic.

In the initial design, there is a 200-Kbps virtual channel between every Data Collector and every Data Distributor in the system. The switch is operated in a barrel shift rotation to avoid output blocking, and full bypass input queuing is used to eliminate input blocking. The fixed barrel shift rotation also eliminates the need for an expanded center stage or path setup logic.

D. Data Distributors

The Data Distributors receive data packets from the Event Builder, perform the final event assembly, and provide an interface to the processors. To support partial event readout, data requests from the processors are transmitted through the Data Distributors.

E. Control Network

The Control Network links the Data Collectors, Data Distributors, and Trigger Supervisor. It is used primarily in the selective readout mode, where it must support broadcast messages.

F. Trigger Supervisor

The Trigger Supervisor serves as the central clearinghouse for the assignment of event numbers to processors. It may improve system performance by uniformly distributing event assignments across the system (to balance switching network data flow), but it is not involved in the data transfer.

![Event Builder Bandwidth](image)

Fig. 2. Event Builder Bandwidth.

The use of a synchronous TDM switch simplifies the implementation of the Event Builder, but it places some requirements on the configuration of the overall system for high-bandwidth operation. In particular, the average volume of data transmitted from each Data Collector and received by each Data Distributor should be balanced over time. If the data rate in any one channel of the switch exceeds its maximum capacity for an extended period of time, the trigger rate must be reduced. Fortunately, the GEM architecture simplifies this load balancing. All major components of the data acquisition system are located in an easily accessible Electronics Room, removed from the detector. The data links connecting the front-end modules to the Data Collectors can be rearranged (within a partition) to optimize system performance.

III. OPERATION

Triggers are generated by the Level One Trigger system and distributed via the Trigger Supervisor and Gating Logic to front-end modules. The data in each front-end module is then compressed and transmitted to a Data Collector. The Trigger Supervisor maintains an event number queue (one queue for each partition) of events passing the Level One Trigger.

Processors with free event buffers will send an event-request message to the Trigger Supervisor. This message may optionally specify a partition. After receiving an event-assignment message from the Trigger Supervisor, the processor may then request blocks of data directly from the Data Collectors. Event-request, event-assignment and data-request messages all flow through the Control Network.

Allocating the data request function to the processors accomplishes two purposes. First, it distributes the data flow management task across the processors, eliminating a centralized buffer manager. Secondly, it allows processors to request only the data needed by the algorithm, which reduces the bandwidth requirements of the Event Builder.
In this "selective" readout mode, the processor uses information from the Level One Trigger system to identify Data Collectors for readout. The processor may make multiple requests based on progression of the algorithm. If the Level Two Trigger passes, the processor will typically issue a request for all data related to that event. The Level Three Trigger will then execute in the same processor.

Although the Level Two processing time is limited to an average of 5 ms (approximately 2 million instructions with the predicted processors) at the peak 100 KHz Level One rate, the total Level Two latency may be as high as 1000 ms. Some of this latency is used in the transfer of data through the Event Builder. To avoid idle time during the data request and data transfer, each processor will operate on a large number of Level Two events simultaneously. This allows a context switch to another pending event during the Event Builder data access time (in the same way that a context switch normally occurs if the processor makes a disk access).

The architecture places no restrictions on the implementation of the second-level trigger. Special-purpose hardware can be used in place of, or in combination with, the general-purpose processors on the output side of the Event Builder. Trigger processors may also be implemented at the input side of the Event Builder, with the results made available to the general-purpose processors in parallel with the Level One data.

IV. CONCLUSION

The conceptual design for a very-high-bandwidth data acquisition system has been outlined. This description forms the basis for the data acquisition system of the proposed GEM detector at SSC [1]. The distinguishing feature is readout of data following the first-level trigger. With large off-detector buffers, the second-level trigger latency can be substantially increased. This allows the use of general-purpose processors and naturally leads to some merging of second- and third-level triggers.

The system supports a data rate as high as 40 Gbps and provides full access to all Level One data by the Level Two and Level Three Triggers. To achieve the full system bandwidth, the average data volume in each Data Collector must be balanced. This requirement is easily accommodated in the GEM architecture. Initial simulations [2] indicate reasonable performance of this architecture over the full design operating range.

V. REFERENCES