The Xyce™ Parallel Electronic Simulator – An Overview*

S. Hutchinson[1], *E. Keiter*[1], *R. Hoekstra*[1], *H. Watts*[2]
A. Waters[3], *R. Schells*[3], *S. Wix*[3]

[1]Computational Sciences Department
[2]Microelectronics Validation Department
[3]Component Information & Models Department
Sandia National Laboratories
Albuquerque, NM 87185, USA
http://www.cs.sandia.gov/Xyce/

ABSTRACT

The Xyce™ Parallel Electronic Simulator has been written to support the simulation needs of the Sandia National Laboratories electrical designers. As such, the development has focused on providing the capability to solve extremely large circuit problems by supporting large-scale parallel computing platforms (up to thousands of processors). In addition, we are providing improved performance for numerical kernels using state-of-the-art algorithms, support for modeling circuit phenomena at a variety of abstraction levels and using object-oriented and modern coding-practices that ensure the code will be maintainable and extensible far into the future.

The code is a *parallel code* in the most general sense of the phrase – a message passing parallel implementation – which allows it to run efficiently on the widest possible number of computing platforms. These include serial, shared-memory and distributed-memory parallel as well as heterogeneous platforms [1]. Furthermore, careful attention has been paid to the specific nature of circuit-simulation problems to ensure that optimal parallel efficiency is achieved even as the number of processors grows.

1. INTRODUCTION

The Xyce™ Parallel Electronic Simulator under development at Sandia National Laboratories is aimed at supporting the laboratory's electrical designers as part of U.S. Department of Energy's Accelerated Strategic Computing Initiative (ASCI). This initiative uses high performance computational simulation to help offset the lack of underground testing and is pushing the limits of scientific computing with a goal of reaching a 100 TFlops capability in the near future. As part of this initiative, the code is targeted at very large (~1000 processors) distributed-memory parallel computing platforms and will provide improvements over existing technology in several areas. Eventually, the Xyce™ Parallel Electronic Simulator will provide simulation at a variety of levels of fidelity including digital, mixed signal and at the device PDE level. This paper describes the current work being done to provide the analog simulator portion of the project.

In addition to providing support for the simulation of circuits of unprecedented size via large-scale parallel computing, novel approaches to critical numerical kernels such as improved time-stepping algorithms and controls, better nonlinear convergence and improved device models are being implemented. These improvements aim to minimize the amount of simulation "tuning" required on the part of the designer and facilitate the code's successful usage.

Another feature required by designers is the ability to easily add device models to the code, many of which are specific to the needs of Sandia. To this end, the device package in the Xyce™ Parallel Electronic Simulator is designed to support a variety of device model inputs. These input formats include the typical, so called, analytical models, behavioral models, look-up tables and support for conductance values extracted from device-scale PDE models. Combined with this flexible interface is an architectural design that greatly simplifies the addition of circuit models.

This paper discusses these features and continues in the next section with a description of the overall code architecture including support for the parallel circuit topology and load balance methods. Following this we discuss the device interface and parallel linear solver methods. The paper ends with some preliminary results and a summary of this work.

2. THE Xyce™ CODE ARCHITECTURE

From the beginning, the Xyce™ Parallel Electronic Simulator was designed not as simply a "parallelization" of an existing circuit simulation capability. Providing parallel capability to any simulation code involves more than parallel data structures. Overall design and, in particular, algorithms designed for parallel computing must be used if one hopes to achieve high parallel efficiency. To this end modern coding-design and leading edge parallel algorithms were utilized from early in the design phase. Included in these are UML (Unified Modeling Language) tools for object-oriented design. Figure 1 illustrates the overall code architecture for the analog simulation kernels currently within the Xyce™ Simulator.

* Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

DISCLAIMER

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

production. Sandia developed a maskless SF_6/O_2 plasma process using Reactive Ion Etching, RIE, that leads to a needle-like texturing in the nanometer scale (Fig. 1) with a black look and excellent low reflection on mc-Si (Fig. 2).

In order to remove plasma-induced damage, different damage removal etches (DRE) were evaluated: etching in KOH or etching in an HNO_3/HF mixture for varying amounts of time. Even though damage etching removes some texture, fairly low reflectance can be maintained. Another crucial step in solar cell processing is the wafer cleaning, which should not remove the texture. A sequence with diluted H_2SO_4/H_2O_2 and HCl/H_2O_2 treatments, respectively, followed by HF dips has been found not to affect the visual appearance of the textured wafers.

Table 1. Weighted reflectance of different silicon surfaces before and after processing (spectral reflectance integrated between 400 nm and 1100 nm and weighted with the AM 1.5 global spectrum).

Texturing Process	Before cell processing	After processing and SiN ARC
RIE	10.0 %	3.9 %
RIE + KOH	20.9 %	5.8 %
RIE + HNO_3/HF	25.4 %	6.9 %
planar	34.8 %	10.4 %

In terms of reflectance control, texturing competes with antireflection coatings (ARC). A standard silicon nitride (SiN) ARC reduces the weighted reflectance on a planar surface from 35 % to 10 % (Table1). However, the initial reflectance of an RIE-textured surface is already 5.4% and drops to as low as 3.9% after SiN deposition. Samples with slightly removed texturing still show excellent reflectance of 11%. After SiN ARC, the reflectance is reduced to 4.3%. The reflectance curve of the mc-Si wafer with no DRE is flat and shows no dependence on wavelength. The planar mc-Si with the single layer ARC shows the characteristic minimum around 600nm. As the DRE time increases the reflectance curves approach the planar reflectance curve as is apparent in Fig. 2. The 20 second DRE etch matches the planar reflectance curve over a large wavelength range. This shows that the RIE texturing can effectively be cancelled if the DRE time is not properly considered.

DOSS DIFFUSION

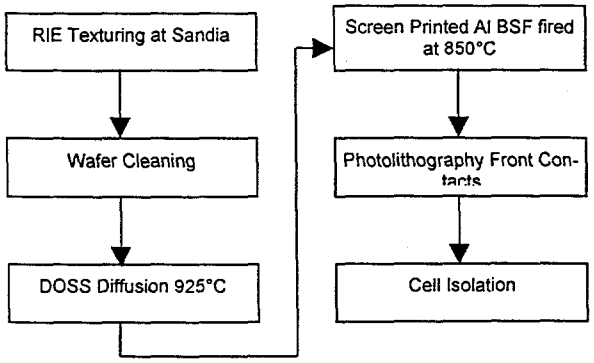

Fig. 3. Process Flow Chart

The emitter diffusion was performed by using the dopant oxide solid source (DOSS) process. Source wafers with spin-on dopant applied to both sides have been introduced to the furnace together with the samples so that every sample is stacked in front of a source wafer on one side only. This diffusion technique was used to take advantage of the in-situ oxide grown in the same furnace cycle as the phosphorus diffusion. An added benefit of this process is no phosphorsilicate glass (PSG) removal step is required. PSG removal could also remove some of the RIE texturing inadvertently. Phosphorus released from the source wafers at 925 °C diffuse into the samples leading either to the symmetric $n^{++}n^{-}n^{++}$ structure for J_{oe} measurements or to the emitter formation only, depending on the stacking. For J_{oe} and lifetime measurements high resistivity (>100 Ω·cm) n-type float zone silicon wafers were used, while solar cells were made from ~1.0 Ω·cm mc-Si. The actual diffusion time was one hour, followed by an oxidation step for 15 min to obtain the in-situ oxide. This one step furnace process leads to phosphorus diffusion, textured, in-situ oxide passivated solar cells that are immediately ready for metallization with no further processing steps. The complete process sequence is shown in Fig. 3.

SURFACE PASSIVATION AND EMITTER PROPERTIES

The challenge in surface texturing of solar cells is to find a way to increase photon absorption in the cell while maintaining low recombination losses at the surface. A rougher surface is harder to passivate. The DOSS process already includes an approximately 10 nm in-situ oxide for passivation, which (after a 15 min forming gas anneal (FGA)) leads to sufficiently low surface recombination velocities (SRV) on planar surfaces (Fig. 4).

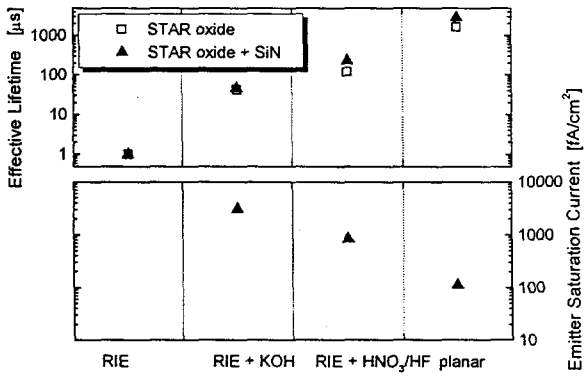

Fig. 4. Effective lifetime and corresponding emitter saturation current of differently textured silicon wafers after DOSS diffusion with in-situ oxide, and additional SiN deposition, respectively.

However, oxide passivation was not sufficient on these RIE-textured surfaces. Only samples with a DRE by HNO_3/HF show sufficiently high effective lifetimes, which correspond to sufficiently low J_{oe} or SRV (notice the logarithmic scale in Fig. 4). To make use of the well-known passivation ability of silicon nitride deposited by plasma enhanced chemical vapor deposition (PECVD), a 63 nm

layer of SiN was deposited on top of the oxidized surfaces. This stack passivation leads to excellent effective lifetimes on planar samples and to good results on the HNO_3/HF etched textured samples. RIE-textured surfaces with no post-treatment or with subsequent KOH etching still show insufficiently low effective lifetimes, corresponding to high J_{oe} and SRV's. The same results were found with a stack passivation consisting of an RTO and ~70 nm of PECVD SiN, but are not shown here. The high quality of the DOSS-diffused emitter and the SiO_2/SiN stack passivation results in low emitter saturation current (J_{oe}) on the planar samples ~100 fA/cm^2 for a 100 Ω/sq. emitter (Fig. 4). However, surface passivation and emitter quality of the textured samples is poor leading to high J_{oe} values (for the samples with no DRE after RIE, it was impossible even to extract a J_{oe}). Emitter saturation current for the best RIE sample is still 5 times higher than a J_{oe} for a random pyramid sample processed similarly. Even the samples that were HNO_3/HF etched after RIE texturing and show decent surface passivation have excessively high J_{oe} values that may limit the performance of high lifetime cells. This indicates poor emitter quality due to plasma-induced damage from the RIE texturing process. Multi-crystalline silicon with much smaller lifetimes is dominated by the base saturation current J_{ob} rather than by J_{oe}. Therefore, RIE texturing may be well suited for such materials because the gain in J_{sc} due to texturing and light absorption is still able to maintain a sufficient V_{oc}, as will be addressed and demonstrated below.

SOLAR CELLS

Table 2. I-V Data for RIE Multi-Crystalline Solar Cells

Wafer Treatment	Voc (mV)	Jsc (mA/cm^2)	FF	η (%)	Increase
planar controls	574	22.20	0.759	9.7	0%
conditioned texture 20 sec nitric Al-assisted	560	27.02	0.695	10.5	9%
20 sec nitric Cr-assisted 8-min KOH	576	24.77	0.756	10.8	11%
conditioned texture ~ 20-25 sec nitric Al-assisted	573	25.83	0.739	10.9	13%
15-sec nitric, conditioned texture 15 sec nitric	582	26.96	0.748	11.7	21%
conditioned texture 10 sec nitric Cr-assisted no DRE	578	27.14	0.748	11.7	21%
	583	29.18	0.756	12.9	33%

Table 3. I-V Data for SiN Coated Solar Cells

Wafer Treatment	Voc (mV)	Jsc (mA/cm^2)	FF	η (%)	Increase
planar controls	584	28.25	0.772	12.7	0%
conditioned texture 20 sec nitric	575	28.93	0.757	12.6	-1%
conditioned texture 10 sec nitric	587	30.84	0.751	13.6	7%
Cr-assisted, No DRE	591	30.63	0.759	13.7	8%

Table 2 shows the averaged efficiencies obtained on mc-Si with RIE texturing for various damage removal etches. Table 3 shows the efficiencies after the application of a 55nm SiN layer which was determined to be the optimal single layer anti-reflection coating (SLARC) by using the Sunrays modeling program. Also shown in the tables is the percent increase in efficiency gained by using RIE texturing compared to the planar surface, relatively. The results clearly show that there is a definite increase in both current collection and overall efficiency by using RIE texturing regardless of the DRE. The efficiency improvement is due largely to the increased current collection while maintaining similar open circuit voltages. In examining table 2 it is apparent that the shorter the DRE the higher the current collection which is supported by the reflectance data (Fig. 2). The longer the DRE time, the higher the average weighted AM1.5 Global reflectance. The improved efficiency is somewhat surprising, because of the extent of the surface damage expected in the "no DRE" case. Excessive carrier recombination and a drop in V_{oc} would be predictable. This is not the case. The in-situ oxide is able to passivate the textured surface sufficiently to maintain ~575 mV V_{oc} that is observed on the planar mc-Si. The increased current collection allows for even higher V_{oc}'s ~585 mV. A more clear understanding is obtained by examining the external quantum efficiency, EQE, depicted in Fig. 5. The blue response of the samples is in agreement with the surface passivation measurements made earlier in Fig. 4. The samples that received a DRE show a better blue response below 450nm demonstrating the superior front surface passivation. The IQE data for these samples, not shown here, also support this claim. However, the improved blue response is not sufficient to compensate for the increased current collection in the "no DRE"

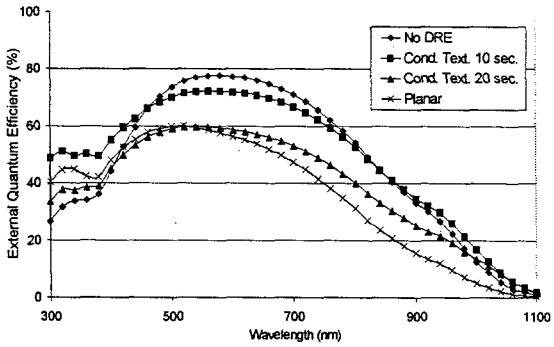

Fig. 5. External Quantum Efficiency of RIE textured samples with different Damage Removal Etches applied.

case. The RIE textured samples out perform the planar sample by collecting over 2 mA/cm^2 more photocurrent. Examining the efficiencies in table 3 and the reflectance curves in Fig. 2 the "10 second nitric" sample closely resembles the "no DRE" in all aspects. The weighted reflectance is 4.2% compared 3.9% after SiN SLARC application. This suggests that a short DRE may achieve an even better efficiency by slightly improving the blue response while still maintaining a low reflectance. The application of the RIE textured surfaces results in 33% initial

improvement and a 8% relative improvement over planar mc-Si samples used in this experiment.

CONCLUSIONS

RIE textured surfaces show excellent reflectance but poor surface quality in general, unless the RIE textured surface receives the proper damage removal etch (DRE). Even after diffusion and surface passivation by a stack of either (thermal) DOSS oxide and PECVD silicon nitride, or rapid thermal oxide (RTO) and PECVD SiN, the surface recombination is still about a factor 5 times higher than that of typical random pyramid surface. Chemical etching after RIE removes the texture to some extent leading to higher initial reflectance. However, these can still have much lower reflectance than planar samples, and the surface passivation is improved at least a little. Especially samples with a HNO_3/HF DRE show decent SRV and therefore might be a good compromise relative to reflectance and surface passivation properties. This is most evident after the application of a SLARC. Solar cell performance is enhanced to a much greater extent when compared to a sample that had no DRE. Efficiency jumps 1.9% absolute for a short DRE with nitric and only 0.8% for no DRE. Even though these samples suffer from damage of the emitter region from the RIE process, solar cells show improved performance compared to planar references. Recent improvements to the DRE process show promise for more complete damage removal, which should result in better cell performance, especially for (lower lifetime) mc-Si solar cells.

REFERENCES

[1] M.A. Green, *Solar Cells: Operating Principles, Technology and System Applications*, vol. 1. Kensington, New South Wales: University of New South Wales, 1982.

[2] J. Zhao, A. Wang, M.A. Green, et al., "19.8% efficient "honeycomb" textured multicrystalline and 24.4% monocrystalline silicon solar cells", *Appl. Phys. Lett.* 73, 1998, pp. 1991-1993.

[3] R. Einhaus, E. Vazsonyi, F. Duerickx, et al., "Recent Progress with Acidic Texturing Solutions on Different Multicrystalline Silicon Materials including Ribbons", *Proc. 2nd WCPEC*, 1998, pp. 1630 - 1633.

[4] R.R. Bilyalov, R. Lüdemann, W. Wettling, et al., "Multicrystalline Silicon Solar Cells with Porous Silicon Emitter", *Sol. Ener. Mater. Sol. Cells* 60, 2000, pp. 391 - 420.

[5] M. Schnell, R. Lüdemann and S. Schaefer, "Stain Etched Porous Silicon - A Simple Method for the Simultaneous Formation of Selective Emitter and ARC", *Proc. 16th EU PVSEC*, 2000, pp. in print.

[6] H. Jansen, M.d. Boer, R. Legtenberg, et al., "The black silicon method: a universal method for determing parameter settings of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control", *Journal of Micromechanics and Microengineering* 5, 1995, pp. 115-120.

[7] Y. Inomata, K. Fukui and K. Shirasawa, "Surface texturing of large area multicrystalline silicon solar cells using reactive ion etching mehod", *Sol. Ener. Mater. Sol. Cells* 48, 1997, pp. 237.

[8] S. Schaefer, H. Lautenschlager, G. Emanuel, et al., "Plasma Etching and its Effect on Minority Charge Carrier Lifetimes and Crystalline Silicon Solar Cells", *Proc. 16th EU PVSEC*, 2000, pp. (in print).

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.