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LDRD Final Report

Investigations of the Impact of the Process Integration of Deposited Magnetic Films for Magnetic Memory Technologies on Radiation Hardened CMOS Devices and Circuits LDRD Project (FY99)

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LDRD Final Report

Investigations of the Impact of the Process Integration of Deposited Magnetic Films for Magnetic Memory Technologies on Radiation-Hardened CMOS Devices and Circuits LDRD Project (FY99)

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Abstract

This project represented a coordinated LLNL-SNL collaboration to investigate the feasibility of developing radiation-hardened magnetic non-volatile memories using giant magnetoresistance (GMR) materials. The intent of this limited-duration study was to investigate whether giant magnetoresistance (GMR) materials similar to those used for magnetic tunnel junctions (MTJs) were process compatible with functioning CMOS circuits. Sandia's work on this project demonstrated that deposition of GMR materials did not affect the operation nor the radiation hardness of Sandia's rad-hard CMOS technology, nor did the integration of GMR materials and exposure to ionizing radiation affect the magnetic properties of the GMR films. Thus, following deposition of GMR films on rad-hard integrated circuits, both the circuits and the films survived ionizing radiation levels consistent with DOE mission requirements. Furthermore, Sandia developed techniques to pattern deposited GMR films without degrading the completed integrated circuits upon which they were deposited.

The present feasibility study demonstrated all the necessary processing elements to allow fabrication of the non-volatile memory elements onto an existing CMOS chip, and even allow the use of embedded (on-chip) non-volatile memories for system-on-a-chip applications, even in demanding radiation environments. However, funding agencies DTRA, AFRL, and DARPA did not have any funds available to support the required follow-on technology development projects that would have been required to develop functioning prototype circuits, nor were such funds available from LDRD nor from other DOE program funds.

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Accomplishments

Per the program plan, Sandia's technical work supported under this LDRD:

1. Provided a concrete demonstration that giant magnetoresistance (GMR) films could be deposited on functioning CMOS circuits without degrading circuit performance. The ability to insert GMR films onto functioning circuits enables the development of embedded non-volatile memory for system-on-a-chip applications with development of an appropriate integration technology. The films used for GMR depositions are also the same materials, deposited under the same conditions as those used for magnetic tunnel junctions.
2. Demonstrated that GMR films could be deposited on radiation-hardened CMOS circuits without degrading the radiation hardness of the as-fabricated circuit. This key result overcomes a major obstacle to the development of fast-write, low-voltage non-volatile memory for radiation-hardened circumvention memories for DOE applications. When combined with the radiation testing of the GMR films described in the next result, this result indicates the viability of a GMR non-volatile, rad-hard memory for DOE systems applications.
3. Demonstrated that GMR films deposited on radiation-hardened CMOS circuits could absorb megarad (SiO_2) doses of ionizing radiation with negligible degradation of their initial (unirradiated) magnetic properties. This key result overcomes a major obstacle to the development of fast-write, low-voltage non-volatile memory for radiation-hardened circumvention memories for DOE applications. When combined with the radiation testing of the CMOS circuits described in the previous result, this result indicates the GMR films are viable for non-volatile, rad-hard memory for DOE systems applications.
4. Developed an approach to patterning GMR films deposited on functioning CMOS circuits without degrading the as-fabricated properties of the CMOS circuit. This result is necessary to pattern the deposited films into individual memory elements, as would be required for GMR-based memories.

These results demonstrate that a rad-hard, non-volatile, GMR-based integrated-circuit technology could be developed if provided sufficient future investments.

I. Introduction

I.1. *Non-Volatile Memory Technology*

Most computer systems rely on either static or dynamic random-access memories to store information for processing. Both static and dynamic memories represent *volatile* storage of information, as they lose information once power to the chip is interrupted. In contrast, a different class of semiconductor memories, referred to as *non-volatile* semiconductor memories, continue to store that data for later retrieval even should power to the memory be interrupted during any time after the write cycle. In all non-volatile semiconductor memories, information must be stored by changing the physical properties (capacitance, resistance, etc.) of a circuit element.

A variety of physical phenomena have been applied to provide non-volatile information storage. Presently, Sandia's systems for the Department of Energy rely on charge that is trapped in a floating-gate memory cell (the silicon-oxy-nitride-oxide-silicon (or SONOS) memory [1]. These non-volatile memories can be hardened against the effects of ionizing radiation but require relatively high operating voltages (> 10 V) to write the data into the memory element.

The search for lower-power non-volatile memories has led some investigators to consider memories based on ferro-electric (PZT and PLZT) effects. Other investigators have examined non-volatile memories based on magnetic phenomena. Piezoelectric memory elements are fabricated from elements that contaminate silicon-based transistors, and thus have been difficult to fabricate. Until recently, magnetic memories have suffered from small changes in physical properties that have made reading the stored information difficult. However, recent advances in magnetic materials, particularly the development of giant magnetoresistance films and magnetic tunnel junctions that exploit quantum-mechanical phenomena, have made magnetically based memory elements again interesting from a technological viewpoint.

I.2. *Candidate Technologies for Magnetic Memory Element*

To retain information in the absence of continuous electrical power, magnetic non-volatile memories align the magnetization of special permanent magnets (deposited magnetic materials) embedded in the semiconductor circuit.

Historically, the first to be developed is anisotropic magnetoresistance (AMR). More recent work has developed films that exhibit an order-of-magnitude greater change in properties, which has become known as "giant" magnetoresistance (GMR). Most recently, magnetic tunnel junctions (MTJ) have exhibited the same magnitude of change in properties but in a different physical configuration that allows current to flow perpendicular to the plane of the device

In the case of anisotropic magnetoresistance or giant magnetoresistance, changes in the magnetization result in changes in the electrical resistance of the magnetic materials, which is sensed to read the data.

With magnetic tunnel junction technology, a thin, electrically insulating barrier separates two layers of ferromagnetic materials. Changes in the relative magnetization directions of the two layers change the probability of the electrons tunneling between the layers, and thus alter the electrical resistance for current between the two layers.

The following sections will describe the physical phenomena available for creating magnetic memory elements in the order of their development. Following this discussion, we will describe a non-volatile memory circuit based on magnetic tunnel junction technology in order to provide the proper perspective for the work performed in this limited-duration LDRD project.

1.2.1 Anisotropic MagnetoResistance (AMR)

The first magnetic phenomenon proposed to create a non-volatile memory element relied on anisotropic magnetoresistance (Figure 1).

Anisotropic magneto resistance (AMR)

$$R = R_0 + \Delta R \cos^2 \Theta$$

$$\text{Typical } R_0 = 10 - 100 \, \Omega, \Delta R/R_0 = 2\%$$

Figure 1. Principles of operation of anisotropic magnetoresistance memory element. Current passes through a magnetic material whose magnetization occurs at an angle Θ to that of the electrical current (I).

Anisotropic magnetoresistance elements sense changes in the amount of current flowing through a magnetic material. Misalignment of the current direction to the direction of a magnetic field embedded in the magnetic material increases the resistance of the film over the resistance that would be obtained were the fields orthogonal. However, typically, the change in resistance is typically only 2% for most embodiments, which is insufficient for most applications. Furthermore, current flows in the plane of the magnetic material, which makes creating a high-density array of these elements challenging from the viewpoint of circuit topology.

1.2.2 Giant MagnetoResistance (GMR)

The next magnetic technology to be pursued for non-volatile memory elements was Giant Magnetoresistance (GMR).

Giant magneto resistance (GMR)

$$R \propto R_0 + \Delta R \cos \Theta$$

$$\text{Typical } R_0 = 10 - 100 \, \Omega, \Delta R/R_0 = 25\%$$

Figure 2. Principles of operation of giant magnetoresistance (GMR) memory element. Current passes through a layer embedded between two magnetic materials in which the magnetization of the first layer occurs at an angle Θ to that of the second layer.

Unlike anisotropic magnetoresistance, which was a single-layer technology, Giant magnetoresistance relied on current flowing in two layers of magnetic material. This technology was able to obtain difference in resistance between the aligned and misaligned states of up to 25%, which made the technology viable for memory elements. In typical scientific fashion, the order-of-magnitude increase in the size of the effect lead to the new descriptor “Giant” as applied to the change in magnetoresistance. However, in these devices, the electrical current resides in the same plane as the magnetic thin film, which is an obstacle to creating high-density circuits.

1.2.3 Magnetic Tunnel Junctions (MTJ)

Most recently, researchers around the world have developed magnetic tunnel junctions for memory elements. In these devices, two materials exhibiting giant magnetoresistance are separated by an insulating barrier, as illustrated in Figure 3.

Figure 3. Material composition of the multilayer magnetic-tunnel-junction (MTJ) memory stack. The thin Al₂O₃ layer provides an insulating barrier between the two stacks of magnetic materials. Note that the magnetic materials used in the MTJ stack are the same as those used for magnetic tunnel junction technology.

With magnetic tunnel junction technology, a thin, electrically insulating barrier separates two layers of ferromagnetic materials. When the magnetization directions of the ferromagnetic

materials are parallel, there is a high probability of the electrons tunneling between the layers, and thus the electrical resistance is low. In contrast, when the magnetization directions are anti-parallel, the tunneling probability is low and the resistance is high. The two layers of the magnetic tunnel junction are chosen such that one layer is more easily magnetized (softer ferromagnet) than the other layer (the harder ferromagnet). This process is illustrated in Figure 4, below, which illustrates the tunneling current between the two layers.

Magnetic tunnel junction (MTJ)

Typical $R_0 = 1\Omega$, $\Delta R/R_0 = 25\%$

Figure 4. Principles of operation of magnetic-tunnel-junction (MTJ) memory element. The electrical of resistance of the memory element depends on the probability of electrons tunneling between the two layers, which is either larger or smaller depending on whether the magnetization M of the layers are parallel or anti-parallel.

Non-volatile memory elements based on magnetic tunnel junction MTJ technology have the significant advantage that current now passes perpendicular to the plane of the magnetic material, enabling high-density layout of the memory elements and a simpler conceptual layout of the memory cell.

1.2.4. Magnetic Non-Volatile Memory Technology

Semiconductor memories are arranged in a two-dimensional (x-y) grid. Information is stored as bits of information inside “words” of data. Thus, to retrieve information, one sequentially interrogates each bit of data in the chosen word of information (Figure 5).

Figure 5. Schematic layout of a semiconductor memory based on magnetic tunnel junctions.

To utilize this physical phenomena in a non-volatile memory, one would rely on a physical layout similar to that illustrated in Figure 6, below.

Figure 6. Schematic illustration of the circuit layout of the magnetic tunnel junction memory cell. An approach to fabricate the non-linear switching element has been developed by workers at Lawrence Livermore National Laboratories, and is not considered in this Sandia-specific project.

To write data into an MTJ memory cell, one applies current through the bit line and through the word line. The combined magnetic fields from currents through bit and word line combine to switch magnetization vector of the soft ferromagnetic film of the magnetic tunnel junction.

To read the data out of an MTJ memory cell, one passes a sense current through the MTJ materials. The sense current creates a voltage across cell proportional to the resistance of the MTJ, which allows the sense circuit to determine whether the MTJ is in the high resistance state R_H or the low resistance state R_L , determined by alignment of magnetization vectors.

II. Potential Benefits

Of all potential semiconductor-based, non-volatile memory technologies, the MTJ technology has the greatest potential for simultaneously achieving high density and speed in operations. If successfully developed, MTJ technology could easily become the nonvolatile memory of choice for the semiconductor industry. SRAM and DRAM technologies would also be threatened.

Our MRAM technology promises greatly improved performance even over that of the unhardened E^2 -PROMs which dominate the non-volatile memory market (\$5.5 B in 1998) for consumer (non-radiation, terrestrial) applications. Demonstration of a working version of our cell would be a *major breakthrough for random-access memories*. Thus, our technology not only addresses niche markets for DOE and space applications, but it could make strong inroads into the market for commercial memories. An appropriate post-processing approach to merge the technology onto an existing CMOS chip further would enable embedded non-volatile memories for "system-on-a-chip" applications, including embedded magnetic sensors.

Radiation-hardened non-volatile memories are important for DOE Defense Programs (DOE/DP) weapon applications for code storage and circumvention. They are used in DOE Nuclear Nonproliferation (DOE/NN) and commercial satellite applications to conserve power. Presently these needs are satisfied through the use of electrically-erasable, programmable read-only memories (E^2 -PROMs). Commercial E^2 -PROMs are vulnerable to ionizing radiation and electro-magnetic-pulse (EMP) effects, which are major concerns for any DOE/DP or DOE/NN application. DOE presently meets its non-volatile memory requirements through a custom, radiation-hardened non-volatile E^2 -PROM technology developed by Sandia and produced by Northrop-Grumman Corporation. The radiation-hardened (rad-hard) E^2 -PROM non-volatile semiconductor memories used by DOE require higher voltages (~ 10 V) for writing information than most modern chip technologies (3 to 5 volts). However, the need for an additional supply voltage greatly complicates system architectures.

Successful demonstration of a functioning rad-hard MRAM memory prototype enables an integrated-circuit-compatible, radiation-hard, non-volatile memory that does not require additional power supply voltage. Read/write times for this memory approach that of the fastest competing technologies with densities approaching that of the densest semiconductor memories. Radiation and EMP effects on the stored data are essentially eliminated. This would allow on-board storage of system information for rebooting semiconductor processors affected by radiation or EMP effects (circumvention for DOE/DP systems). The development of a high-

speed, lower-voltage technology would simplify the design of rad-hard systems and allow low-power operation; thereby saving both weight and volume by requiring reduced on-board power supplies. In addition, as future device technologies scale their dimensions, the MRAM technology will also scale, as the basic operation of the cell is independent of the MTJ area.

If successful, this technology would be a dramatic improvement over the commercial E²-PROMs that presently represents a \$5.5B annual market in 1998. By developing an appropriate processing approach to fabricate the non-volatile memory elements onto an existing CMOS chip, this technology may even allow the use of embedded (on-chip) non-volatile memories for "system-on-a-chip" applications-- thereby further expanding the potential market for this technology. These system-on-a-chip applications would further expand the potential market for our MRAM technology.

Our proposed rad-hard MRAM technology would be ideal for that the booming commercial satellite market, which will launch \$3.6 B worth of commercial satellites in the next five years alone. Furthermore, our MRAM technology offers improved performance even over that of the unhardened E²-PROMs which dominate the non-volatile memory market (\$5.5 B in 1998) for consumer (non-radiation, terrestrial) applications. Demonstration of a working version of our cell would be a *major breakthrough for random-access memories*. Thus, our technology not only addresses niche markets for DOE and space applications, but it could make strong inroads into the market for commercial memories. An appropriate post-processing approach to merge the technology onto an existing CMOS chip would enable embedded non-volatile memories for "system-on-a-chip" applications. Success would spawn new commercial start-up companies that would be needed to commercialize the infrastructure required to add the magnetic memory elements onto the MRAM integrated circuits.

III. Project Plan

The objective for the mid-year LDRD consisted of matching efforts at both Sandia and LLNL. The Sandia effort investigated the process integration issues for fabrication of LLNL's MTJ MRAM cell designs on Sandia's rad hard CMOS ICs, along with radiation testing of MRAM cells supplied by LLNL.

This was an ambitious LDRD project, even with its limited scope of demonstrating the feasibility of the required technical elements. This project combines unique capabilities at LLNL and at SNL to attempt a revolutionary advance in non-volatile memory technology for DOE applications. To achieve a fully integrated technology, these magnetic materials must be integrated with functioning integrated circuits in a way that preserves both the quality of the magnetic materials and simultaneously the quality and robustness of the integrated circuits.

The objective for the mid-year LDRD consists of matching efforts at both Sandia and LLNL. The Sandia effort is to understand the process integration issues for fabrication of LLNL's MTJ MRAM cell designs on Sandia's rad hard CMOS ICs, along with radiation testing of MRAM cells supplied by LLNL.

Although it is generally agreed the magnetic materials should be rad hard, to our best knowledge, no radiation-testing information is available for the advanced GMR structures. Thus, the proposed initial experiments are critical for providing a fundamental evaluation of the suitability of magnetic memory chips for DOE applications as well as for other commercial environments. It is estimated that the booming commercial satellite market will launch \$3.6 B worth of commercial satellites in the next five years.

By developing an appropriate processing approach to allow fabrication of the non-volatile memory elements onto an existing CMOS chip, this technology could allow the use of embedded (on-chip) non-volatile memories for "system-on-a-chip" applications— further expanding the potential market for this technology. By investigating the feasibility of such integration (proving that incorporation of magnetic films do not degrade integrated-circuit operation, we intend to develop the confidence required to enable this new capability to be supported as an addition to an existing integrated-circuit process flow. This feasibility demonstration is an essential first step toward expediting the formation of start-up companies required to provide the essential infrastructure (materials, manufacturing equipment, diagnostics, etc.) for manufacturing the MRAM technology.

LLNL developed advanced capabilities in the design, analysis, and deposition of magnetic materials. The work at LLNL was supported through LLNL's own LDRD funds and coordinated with Sandia. Sandia's activity involved substantial technical risk, as is appropriate for Laboratory-Directed Research and Development.

Considerable innovation is required to integrate non-standard materials such as the GMR and MTJ films into a CMOS process that is exquisitely sensitive to contamination. Sandia alone has the facilities, the expertise, and the experience to attempt a monolithic integration of these novel materials systems with a full-flow CMOS process. Sandia possesses uniquely configurable clean rooms. Sandia also has developed extensive experience in integration of other non-standard materials such as ferroelectrics with silicon circuits and through development of other techniques, including post-process integration of compound-semiconductor technologies such as Vertical-Cavity Lasers with silicon-based technologies such as integrated micromachines. Our success in these previous projects gives us the confidence to attempt MRAM integration with CMOS.

IV. Experimental Procedure

Giant-magnetoresistance (GMR) films were deposited on functional CMOS wafers at Lawrence Livermore National Laboratory (LLNL). These materials are the same as those typically used for magnetic-tunnel junctions and thus allow accurate estimation of the impact of depositing magnetic films for either purpose on silicon circuits. The GMR-coated wafers were then irradiated at Sandia in a Co-60 gamma-ray cell to a variety of fluences, up to, and including 1 Mrad(SiO₂).

All transistors and ICs were fabricated in Sandia's Microelectronics Development Laboratory in its baseline technology, a half-micrometer CMOS technology using shallow-trench

isolation (CMOS6r) [2], schematically illustrated in Figure 7. This 5-V technology employs separate wells for the p-channel and the n-channel transistors, as N-channel and P-channel transistors are fabricated in retrograde p- and n-wells, respectively. The technology uses shallow-trench isolation, sidewall implants, and a silicon-nitride cap over the isolation trench. Ion implantations create lightly-doped drain structures. A single level of polysilicon is used for gate control, titanium salicide forms the ohmic contacts, and tungsten fills are used for the inter-level interconnects.

A cross section of the technology is shown in Fig. 1. The gate-oxide thickness for the technology is 13nm. This oxide is somewhat thicker than usual for half-micrometer technologies, but it is necessary to maintain oxide reliability at a 5-V operating voltage (most commercial half-micrometer technologies operate at 3.3V). The effective channel length of this technology is slightly less than 0.5 μm , with 0.6- μm as-drawn gates and 0.7- μm general design rules. The technology incorporates a single polysilicon level for gates, local interconnect, and SEU resistors, and three levels of metal. Only one level of metal is required to fabricate test transistors and the 16K-bit SRAM used in many of our technology evaluations, as the additional metal levels connect the individual 16K-bit blocks into larger on-chip memories. Chemical-mechanical polishing is used extensively in Sandia's CMOS technology to planarize the shallow trench isolation, tungsten via fills, and interlevel dielectrics.

Figure 7. Schematic cross section of Sandia's baseline CMOS technology.

This study examined samples from lot BD14417A, which was processed to the first level of metal interconnect (Metal 1 in Figure 7 above). Following patterning of Metal 1, a one-micrometer thick silicon dioxide film was deposited to serve as the interlayer dielectric for the giant magnetoresistance film. Bond pads were photopatterned and etched using mask set RS144. The test structures were then characterized before deposition of the GMR films. The wafers were re-inserted into the process flow, and a 1.7-micrometer-thick resist (THMR) was patterned using a reverse image reticle of the same mask set (RS144) to prevent GMR film from obscuring the metal bond pads (approximately 100 μm^2) required for post-deposition characterization of the same test structures. To facilitate lift-off (Figure 7) of the deposited films, a 100-nm

undercut oxide etch (100:1 HF acid solution in water) was performed before GMR film deposition.

GMR films were sputter deposited at Lawrence Livermore National Laboratories (LLNL). Depositions consisted of 20-nm and 200-nm thick GMR layers and dummy samples consisting of 20-nm Ti and 200-nm Ni layers. Two types of 200-nm-thick GMR layers also were deposited: 30 periods of (4 nm of NiFeCo)/(3 nm of Co) and 20 periods of (10 nm of FeMn). The 20 nm GMR layers consisted of 5 nm NiFeCo/2.3 nm Cu/2 nm NiFeCo/10 nm FeMn/2 nm Cu.

To evaluate the effect of GMR deposition on functioning CMOS circuits, the 20-nm-thick GMR film was sputter deposited over the patterned wafer. The contacts were then opened using a lift-off process through sonification in an acetone solution. Samples were evaluated for effectiveness of lift-off process on the large-area contact pads. Device parametrics were re-tested for the test structures, and discrete transistors were then tested for the effects of ionizing radiation at various stages during room-temperature irradiation.

Samples for process development for fine-geometry patterning (as would be required for actual memory cells) were milled in the ion mill (Oxford 300+) under the following conditions: RF power = 200 W, beam current = 165 mA, beam voltage = 250 V, acceleration voltage = 250 V, source gas = 8 sccm Ar, plateau - cool (back pressure 10 mbar).

For this study, we characterized the effects of irradiation on standard (transistor type T1: 20 x 0.6 μm) and annual (transistor type T3: 49.5 x 0.6 μm) n- and p-channel transistors with a gate-to-source voltage = 5V. X-ray irradiations were performed using an ARACOR Model 4100 Semiconductor X-ray Irradiator [3]. The x-ray irradiator (including wafer prober) is interfaced to an HP4062 parametric tester for test structure parametric measurements. The x-ray irradiator and the HP4062 parametric tester are controlled by a HP workstation. All irradiations were performed at room temperature. The dose rate of the x-ray source was 1667 rad(SiO_2)/s. Radiation-induced threshold-voltage shifts, ΔV_{th} , as well as shifts due to oxide- and interface-trap charge, ΔV_{ot} and ΔV_{it} , were estimated from transistor current-voltage measurements at room temperature using the midgap charge-separation technique [4]. The n- and p-channel transistor threshold voltages were extrapolated from linear least-square fits to the square-root of the drain-source current versus gate-to-source voltage curve in the saturation region at ± 5 V. The drain-to-source current range used for extrapolation was selected from the linear portion of the square-root of the drain-source current versus gate-to-source voltage curve. The extrapolation range was scaled according to the transistor size.

Test structures/circuits used for evaluation included serpentine/combs, 30/3000 contact structures, capacitors, SEU resistors (polysilicon level), large area diodes, n-channel FETs, p-channel FETs (T1 transistors of 200 μm x 0.6 μm as well as T3 transistors, and 16 kilo-bit (16K) static random-access memories (SRAMs). The 16K SRAM is the smallest functioning block of our baseline and is repeated 16 times on chip to create our 256K SRAM baseline product.

V. Results

V.1 . Effect of film deposition on functioning circuits

Deposition of GMR films caused no degradation in the on-chip passive components.

Following the deposition of the GMR films, no observable shifts were obtained from the following test structures: metal serpentines/combs, single-event upset (polysilicon) resistors, and the n-well and p-well poly capacitors.

As a result of the depositions, contact resistance of Metall (M1) contacts to the N+ diffused regions as measured by discrete Kelvin structures exhibited approximately a 12% improvement. Similarly, the contact resistance of Metall contacts to the P+ diffused regions as measured by discrete Kelvin structures exhibited approximately a 17% improvement, while the contact resistance of the discrete Kelvin structures exhibited about a 40% improvement. No observable shift was detected in the M1/N+, M1/P+, and M1/Polysilicon (N+) 30/3000 contact chains.

Large area diodes (both n+ and p+) appeared to exhibit approximately an order of magnitude decrease in junction leakage current; however, this could not be verified due to differences in the resolution of the different testers used throughout this study. There also were no observable shifts in either the forward-bias turn-on voltage nor the reverse-bias breakdown voltages of the large area diodes.

In examining the effects of GMR deposition on the active devices we find essentially no changes in the transistor characteristics, except for a minor change in the threshold (turn-on) voltage of a minority of the transistors. These sorts of changes appear consistent with the effects of the sputter deposition of the GMR films on the underlying transistors. The magnitude of the changes is within design windows and can be accommodated by standard circuit layout techniques.

Table 1. Summary of the effects of GMR/MTJ Magnetic Material deposition on electrical behavior of functioning circuits.

Parameter	N-channel Transistors	P-channel Transistors
drain breakdown voltage	no change	no change
off current, I_{off}	Approx. an order of magnitude reduction (different testers?)	no change
on current, I_{dsat}	no change	no change
Transconductance, g_m	no change	no change
sub-threshold slope, S	no change	no change
Threshold voltage, V_{tsat}	<p>No change on 90% of sites</p> <ul style="list-style-type: none"> — Approx. 20% reduction on remaining sites — Note: observed only on short-channel devices <p>Plasma effects?</p>	approx. 8% increase

Figure 8. Semilogarithmic plot of the change in N-channel, 20- μm gate width by 0.6- μm gate length transistor characteristics before (black line) and after (red lines) deposition of GMR films (MTJ materials). Excess photocurrent current at low gate-source voltages is an artifact of the measurement.

Figure 9. Semilogarithmic plot of the change in P-channel, 20- μm gate width by 0.6- μm gate length transistor characteristics before (black line) and after (red lines) deposition of GMR films (MTJ materials).

Examination of the 16 kilobit static random access memories indicated no observable degradation of circuit functionality (yield) or performance following deposition of the magnetic materials.

The present feasibility study demonstrated all the necessary processing elements to allow fabrication of the non-volatile memory elements onto an existing CMOS chip, and even allow the use of embedded (on-chip) non-volatile memories for system-on-a-chip applications. To be relevant to DOE missions, however, it is essential to demonstrate that such a technology can still function even in demanding radiation environments.

V.2. Impact of film deposition on radiation-hardness of Sandia's rad-hard CMOS circuits

To determine whether GMR-based or MTJ-based technologies would be suitable for DOE weapons or satellite applications, we irradiated films deposited over Sandia's baseline rad-hard CMOS technology, as described in Section IV to examine whether deposition of magnetic materials degraded the radiation hardness of Sandia's baseline CMOS technology.

In Figure 10 we illustrate typical characteristics of N-channel transistors with deposited magnetic films following various levels of irradiation.

Figure 10. Semilogarithmic plot of the change in N-channel, 20- μm gate width by 0.6- μm gate length transistor characteristics containing deposited magnetic materials following various stages of irradiation. In this figure, the arrows indicate the transistor curves corresponding to each level of irradiation in $\text{rad}(\text{SiO}_2)$.

Data such as presented in Figure 10 was analyzed [4] as described in Section IV to determine radiation-induced shifts in key transistor characteristics: threshold-voltage, ΔV_{th} , as well as shifts due to oxide-trapped charge (ΔV_{ot}) as well as interface-trap charge (ΔV_{it}). The results (presented in Figure 11) indicate that deposition of magnetic material had negligible effects on the radiation-hardness of Sandia's baseline CMOS technology.

Figure 11. Comparison of the radiation-induced shifts in threshold-voltage, ΔV_{th} , as well as shifts due to oxide-trapped charge (ΔV_{ot}) and interface-trap charge (ΔV_{it}) for N-channel, 20- μm gate width by 0.6- μm gate length transistor characteristics containing deposited magnetic materials.

Similar data for the P-channel transistors are presented in Figures 12 and 13, and indicate the same negligible effect of the deposition of magnetic materials on Sandia's baseline CMOS technology.

Figure 12. Semilogarithmic plot of the change in P-channel, 20- μm gate width by 0.6- μm gate length transistor characteristics containing deposited magnetic materials following various stages of irradiation. In this figure, the arrows indicate the transistor curves corresponding to each level of irradiation in rad(SiO₂).

Figure 13. Comparison of the radiation-induced shifts in threshold-voltage, ΔV_{th} , as well as shifts due to oxide-trapped charge (ΔV_{ot}) and interface-trap charge (ΔV_{it}) for P-channel, 20- μm gate width by 0.6- μm gate length transistor characteristics containing deposited magnetic materials.

The data presented above indicate that the total-dose radiation-hardness of Sandia's baseline CMOS technology was not impacted by the deposition of the magnetic films.

{Related radiation testing at LLNL: Additional magnetic films were irradiated at Sandia and then returned to LLNL for characterization of the magnetic films themselves. As would be expected, the irradiated magnetic films exhibited no change in magnetic properties from the total-dose exposure [5]. However, the major concern for the radiation hardness of magnetic memories is the effect of the electro-magnetic pulse associated with the source of the transient radiation. In that regard, separate studies at Lawrence Livermore National Laboratory indicate that an external magnetic field of over 400 oersteds (quite a substantial field strength) is required to switch the magnetization of the deposited magnetic films.

V.3. Patterning technology for deposited magnetic films

We have successfully etched 20-nm, 200-nm thick GMR layers and dummy samples consisting of 20-nm Ti and 200-nm Ni layers. Two types of 200-nm-thick GMR layers were etched: 30 periods of (4 nm of NiFeCo)/(3 nm of Co) and 20 periods of (10 nm of FeMn). The 20-nm GMR layers consisted of 5nm NiFeCo/2.3nm Cu/2nm NiFeCo/10nm FeMn/2nm Cu.

While an actual thickness necessary for an MRAM structure is 20 nm, 200-nm-thick structures were etched as well for the ease of inspection of the cross sectional images in the Scanning Electron Microscope (SEM).

We found that we can ion mill 20-nm layers into stripes of different widths, achieving widths narrower than 1 micrometer. We can also ion mill various thickness GMR films. Typical results are illustrated in Figure 14.

Figure 14. Scanning electron micrograph of the patterned deposited magnetic materials using ion milling before photoresist removal. Note from the scale of the micrograph as the layer has been defined to dimensions smaller than one micrometer indicating our ability to pattern the deposited films to dimensions consistent with high-density semiconductor memories.

In etching the magnetic layers, problems developed related to the removal of the photoresist (PR) mask after milling. Normal procedure includes a 24-hour soak in acetone to remove PR mask, but sometimes some PR remains and we have to do an O₂ plasma clean. Photoresist removal problems are probably related to inadequate plateau cooling inside the ion-milling machine and could be remedied by improving the cooling scheme.

As the data indicates, however, we have found a process for patterning the deposited GMR films (same materials as the MTJ stack) that is compatible with the dimensions required for high-density semiconductor memories.

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VI. Attempts to Develop Follow-On Funding

Personal contacts to potential sponsors by both LLNL and SNL project leaders were followed up by brief e-mail summaries of the results of this project. The e-mail summary was widely circulated within the Department of Defense community. However, no DoD program had funding available to support this innovative alternate technology.

VII. Summary

Per the program plan, Sandia's technical work supported under this LDRD:

1. Provided a concrete demonstration that magnetic materials such as used for Giant MagnetoResistance (GMR) films or Magnetic Tunnel Junctions (MTJ) can be deposited on functioning CMOS circuits without degrading circuit performance in either normal or radiation environments. The ability to insert these magnetic films onto functioning circuits enables the development of embedded non-volatile memory for system-on-a-chip applications after development of an appropriate integration technology. As the films used for GMR depositions are also the same materials, deposited under the same conditions as those used for Magnetic Tunnel Junctions, and thus the results of this study indicate the process compatibility of either type of magnetic memory.
2. Demonstrated that magnetic materials such as used for Giant Magneto-Resistance (GMR) films or Magnetic Tunnel Junctions (MTJ) could be deposited on radiation-hardened CMOS circuits without degrading the radiation hardness of the as-fabricated circuit. This key result overcomes a major obstacle to the development of fast-write, low-voltage non-volatile memory for radiation-hardened circumvention memories for DOE applications. When combined with the radiation testing of the magnetic films described in the next result, this result indicates the viability of a GMR non-volatile, rad-hard memory for DOE systems applications.
3. Demonstrated that GMR films deposited on radiation-hardened CMOS circuits could absorb megarad(SiO_2) doses of ionizing radiation with negligible degradation of their initial (unirradiated) magnetic properties. This key result overcomes a major obstacle to the development of fast-write, low-voltage non-volatile memory for radiation-hardened circumvention memories for DOE applications. When combined with the radiation testing of the CMOS circuits described in the previous result, this result indicates the GMR films are viable for non-volatile, rad-hard memory for DOE systems applications.

4. Developed an approach to patterning GMR films deposited on functioning CMOS circuits without degrading the as-fabricated properties of the CMOS circuit. This result is necessary to pattern the deposited films into individual memory elements, as would be required for GMR-based memories.

These results demonstrate that a rad-hard, non-volatile, GMR-based or MTJ-based integrated-circuit technology could be developed if provided sufficient future investments.

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