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IC-Compatible Technologies for Optical MEMS

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Introduction

Optical MicroElectroMechanical Systems (Optical MEMS) Technology holds the promise of one-day producing highly integrated optical systems on a common, monolithic substrate. The choice of fabrication technology used to manufacture Optical MEMS will play a pivotal role in the size, functionality and ultimately the cost of optical microsystems. By leveraging the technology base developed for silicon integrated circuits, large batches of routers, emitters, detectors and amplifiers will soon be fabricated for literally pennies per part. In this article we review the current status of technologies used for Optical MEMS, as well as fabrication technologies of the future, emphasizing "manufacturable" surface micromachining approaches to producing reliable, low-cost devices for optical communications applications.

Integrated vs. Free Space Optical MEMS

Most Optical MEMS devices can be categorized as using either an Integrated Optics, or Free-Space Optics approach to manipulate a light signal. The Integrated Optics approach relies on waveguides and micromechanical actuators to redirect, modulate, and multiplex a light signal. In free space optics the light signal is manipulated using electromechanical actuators to position optical components, such as reflectors, lenses and diffraction gratings fabricated out of the mechanical material. Both approaches have been studied extensively over the past decade.

Integrated optics is somewhat difficult to implement in conventional silicon technology since the doped oxides and silicon nitride dielectrics typically used for waveguides are attacked by the etches needed to release silicon MEMS. To maintain

compatibility with MEMS processing, researchers are exploring polymer waveguides made from PMMA and polyimides. These films are less susceptible to attack in release etches and are also being explored for their elasto-optic and electro-optic properties. Perhaps a more appropriate materials system for integrated Optical MEMS would be III-V compound semiconductors such as the GaAs/AlGaAs or InP/InGaAsP system, where optical emitters, amplifiers, detectors and MEMS can be integrated onto a single monolithic substrate. Compound semiconductor MEMS is still in its infancy compared to its silicon counterpart, but have the potential to offer more functionality by leveraging the large electro-optical and opto-mechanical effects seen in these materials.

Free-space Optical MEMS is arguably a more manufacturable approach than Integrated Optical MEMS for optical communications. Rather than using compound semiconductors and materials with a range of refractive indexes, free-space Optical MEMS typically employ mechanical polysilicon components to reflect, diffract and modulate a light signal. The force levels available in the microdomain are quite low, on the order of tens of *micro*newtons. However, the inertia of these micromechanical components is also quite low, allowing for high-speed optical switching devices which operate at extremely low power levels. An assortment of optical devices has been demonstrated via free space Optical MEMS [1], including NxN switch matrices, Fresnel lenses, mirrors and blazed gratings, as well as complete systems such as the "Silicon Optical Bench" which integrates several of these components [1]. From a manufacturing standpoint, one of the most compelling reasons to use silicon free-space Optical MEMS is that the fabrication and packaging technologies are very similar to integrated circuits, and are therefore much more amenable to large-scale, low-cost production processes.

The most widely used MEMS fabrication technology today is silicon surface micromachining, where sacrificial oxides are interleaved with mechanical polysilicon layers. The final step in the fabrication sequence is to etch sacrificial oxides in hydrofluoric acid (HF), leaving freestanding mechanical polysilicon structures. Several MEMS foundries in the US and Europe specialize in surface micromachining, with manufacturing capacities ranging from prototype levels to full-scale production. At

Sandia National Laboratories, the four level Sandia Ultra planar Multi-level MEMS Technology (SUMMiT-IV) [2] is available to the public for agile prototyping applications, offering customers access to the most complex MEMS technology available. As shown in Figure 1, the SUMMiT-IV technology has four independent layers of polysilicon, with the first level (Poly 0) typically used as a ground plane and the remaining layers used for free standing mechanical structures. The fabrication sequence in the SUMMiT-IV technology begins with the growth and deposition of a thermal oxide and silicon nitride layer respectively, for dielectric isolation from the substrate. Next, doped polysilicon is deposited and patterned followed by the deposition and subsequent patterning of a sacrificial oxide. This basic sequence is repeated for Poly 1, Poly 2 and Poly 3, producing the layer stack shown in Figure 1. A distinguishing feature of the SUMMiT-IV technology is the use of Chemical Mechanical Polishing (CMP) [3] to planarize the sacrificial oxide (SacOx 3) directly beneath the topmost polysilicon layer (Poly 3). By planarizing SacOx 3, surface topography is not transferred to the optical components, such as mirrors, which are typically made in Poly 3. Further steps are taken during processing to anneal polysilicon structures to relieve built-in stress which can lead to curvature of free standing polysilicon mirrors. The result is an optically flat, smooth polysilicon surface (*see sidebar*) that can be later coated with gold or aluminum to further increase reflectivity.

Researchers at Sandia are developing the next-generation silicon micromachining technology, SUMMiT-V, which will add an additional sacrificial oxide layer, CMP process and a *fifth* mechanical layer of polysilicon to the SUMMiT-IV process. Figure 2 shows a Scanning Electron Microscope (SEM) image of a micromechanical lock made with the SUMMiT-V Technology. In this device, an electrostatic "microengine" is driving a "microtransmission" to assemble a pop-up mirror used to direct an optical signal. A cross section of a component of the micromechanical lock is shown in Figure 4, illustrating the five layers used in this technology, including the laminated Poly 1 and Poly 2 layers, as well as the independent Poly 3 and Poly 4 layers, all above the ground plane, Poly 0. By including two CMP steps and five mechanical layers of polysilicon, we expect the SUMMiT-V to be an enabling technology for advanced optical microsystems.

A major challenge in surface micromachining is to eliminate the tendency for polysilicon layers to stick to the substrate and to each other after the final HF release and H_2O rinse steps. In the microdomain, capillary forces are typically much greater than the elastic restoring forces of 1-2 μm thick polysilicon structures. As a result, freestanding mechanical structures are often pulled into the substrate while drying, where they become permanently bonded, rendering the devices useless. To combat this pervasive "stiction" problem, researchers are adopting freeze dry sublimation and super-critical CO_2 drying techniques for MEMS in an effort to eliminate the liquid – gas interface present during air-drying. While these drying techniques are effective at producing released structures, polysilicon devices quickly oxidize, resulting in a hydrophilic surface where water can condense. This typically leads to in-use stiction problems in humid environments. An alternative approach is to apply anti-stiction coatings to the device, such as PerFlouroTrichloroSilane (PFTS) and Teflon-like fluorocarbon films, after release to create a hydrophobic, water-resistant, "anti-sticton" surface. These films hold great promise for minimizing adhesion energies to their lowest possible values and will play a major role in manufacturing reliable microsystems.

Alternative IC Compatible Micromachining Technologies

Polysilicon and silicon dioxide are clearly the most widely used structural and sacrificial materials in silicon surface micromachining. However, alternative materials combinations have been demonstrated that are also quite compatible with the IC technology base. A notable example is the Digital Micromirror Display developed by Texas Instruments, which uses an aluminum alloy as the structural material and photoresist as the sacrificial material. To release the large array of micromechanical aluminum mirrors, an oxygen plasma is used to etch the sacrificial photoresist. The advantage of this approach is that the release is basically a dry process, which eliminates the capillary forces found with wet etches that so often lead to stiction. Another example of an IC-compatible surface micromachining technology is the process developed by Silicon Light Machines to fabricate the Grating Light Valve (GLV) display. The GLV

uses silicon nitride and aluminum as the structural and conductive materials to form an electrostatically-actuated diffraction grating. The sacrificial material is polysilicon, which is removed at the end of the process using xenon difluoride, a dry isotropic etch that is highly selective to polysilicon. The result is a MEMS technology that is compatible with conventional CMOS processing, which has been used to produce optical switches operating in the megahertz range.

Future Direction of Optical MEMS Technology

The trend in Optical MEMS technology is clearly toward adding greater functionality to micromachined devices to produce the components necessary for optical communications subsystems. In the not too distant future we expect that optics, micromechanics and microelectronics will merge into a single, integrated technology base, that will be capable of producing complete opto-electro-mechanical systems on a chip. In the near term, the best candidate is silicon technology combined with compound semiconductors in hybrid multichip packages. Figure 4 is an example of such a system under development at Sandia for use as a Trajectory Safety Subsystem on a Chip (TSSC) [4]. The TSSC integrates a GaAs-based Photonic Integrated Circuit (PIC) together with a silicon MEMS actuator into a single package, which is powered by an on-board photocell using light delivered by an optical fiber. Although used as a safety subsystem, the same technology used in the TSSC can be used for optoelectronic integrated circuits to control the flow of information for the next-generation of fiber optic communication networks.

Acknowledgments

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Figure Captions

Figure 1. Layer stack for Sandias SUMMiT-IV surface micromachining technology.

Figure 2. Micromechanical lock fabricated in Sandias SUMMiT-V Technology.

Figure 3. Cross section of micromechanical lock component showing all five polysilicon layers.

Figure. Schematic of Trajectory Safety Subsystem on-a-Chip (TSSC).

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1 Ming C. Wu, Micromachining for Optical and Optoelectronic Systems, Proceedings of the IEEE, Vol 85, No. 11, November 1997.

2 For more information, please visit our web site at: http://www.mdl.sandia.gov/Micromachine

3 Dale L. Hetherington, Jeffry J. Sniegowski, Improved Polysilicon Surface-micromachined Micromirror Devices Using Chemical Mechanical Polishing, Presented at the International Symposium on Optical Science, Engineering, and Instrumentation, SPIE's 43rd Annual Meeting, San Diego, CA, July 22, 1998.

4 Marc A. Polosky et.al., Trajectory Safety Subsystem on a Chip, to be Presented at the 10th International Conference on Solid State Sensors and Actuators, June 6-10, 1999, in Sendai Japan.

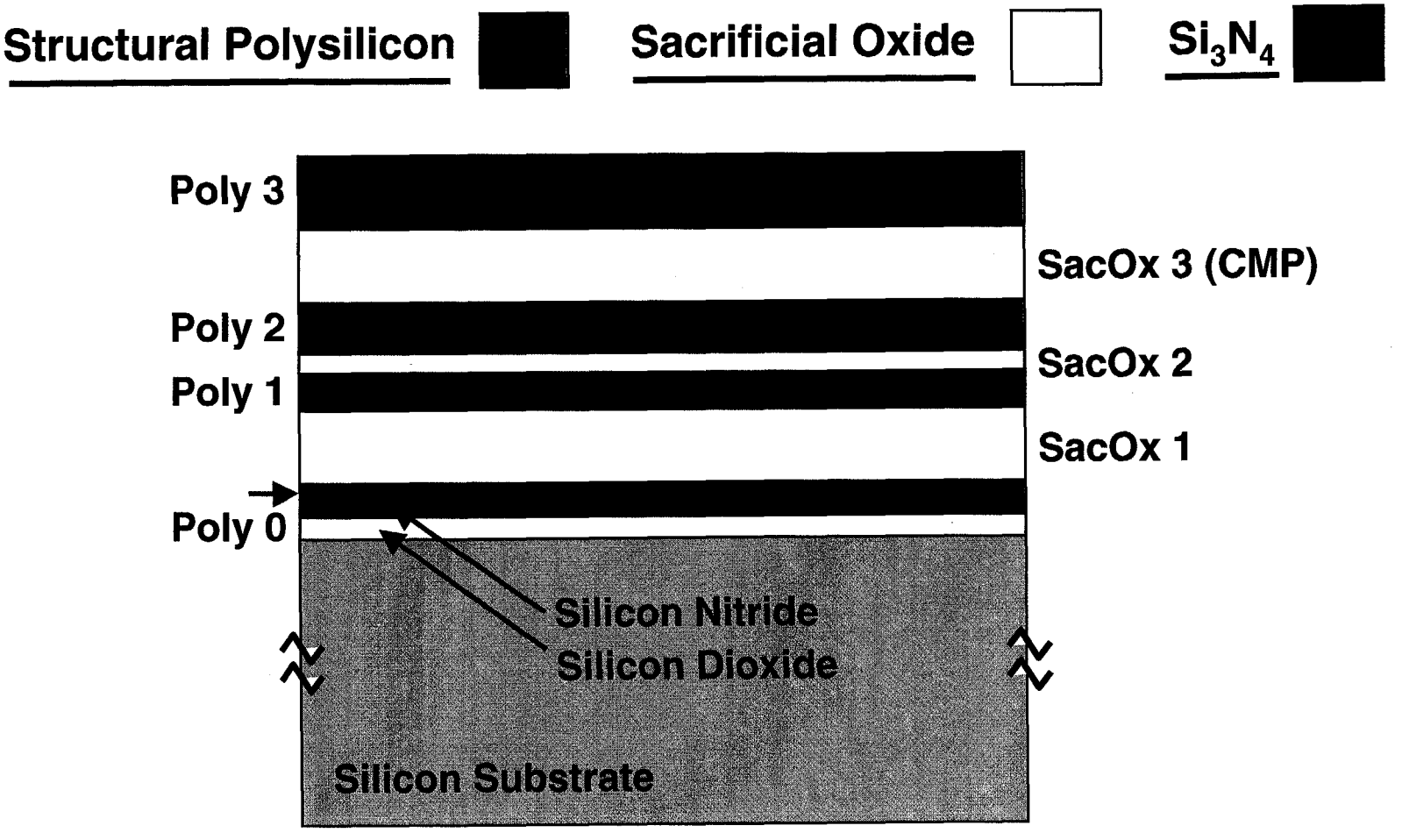
Structural Polysilicon
Sacrificial Oxide
Si_3N_4
Poly 3
SacOx 3 (CMP)
Poly 2
SacOx 2
Poly 1
SacOx 1
Poly 0
Silicon Nitride
Silicon Dioxide
Silicon Substrate

Figure 1

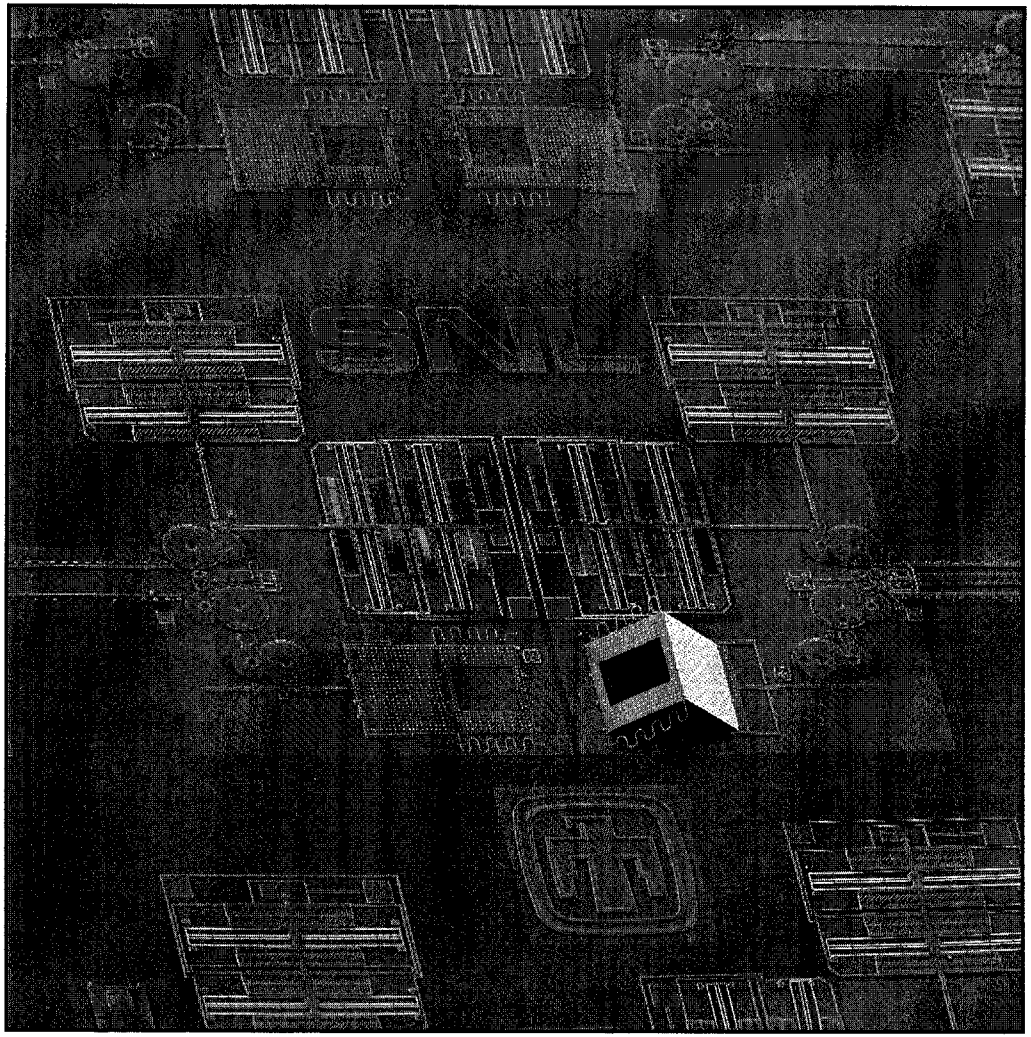

Figure 2

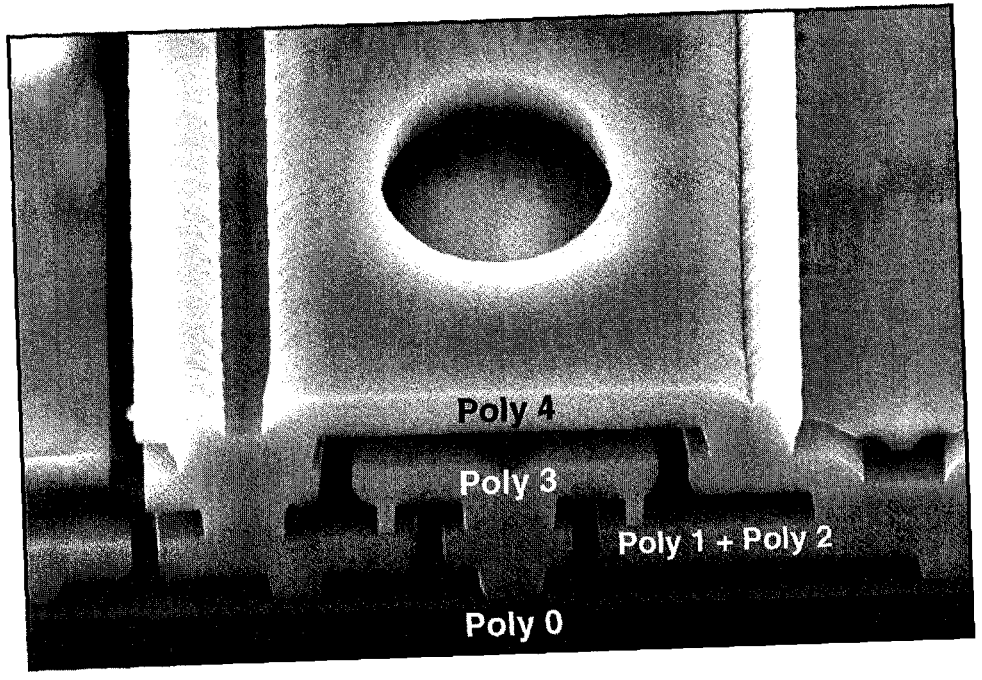

Figure 3

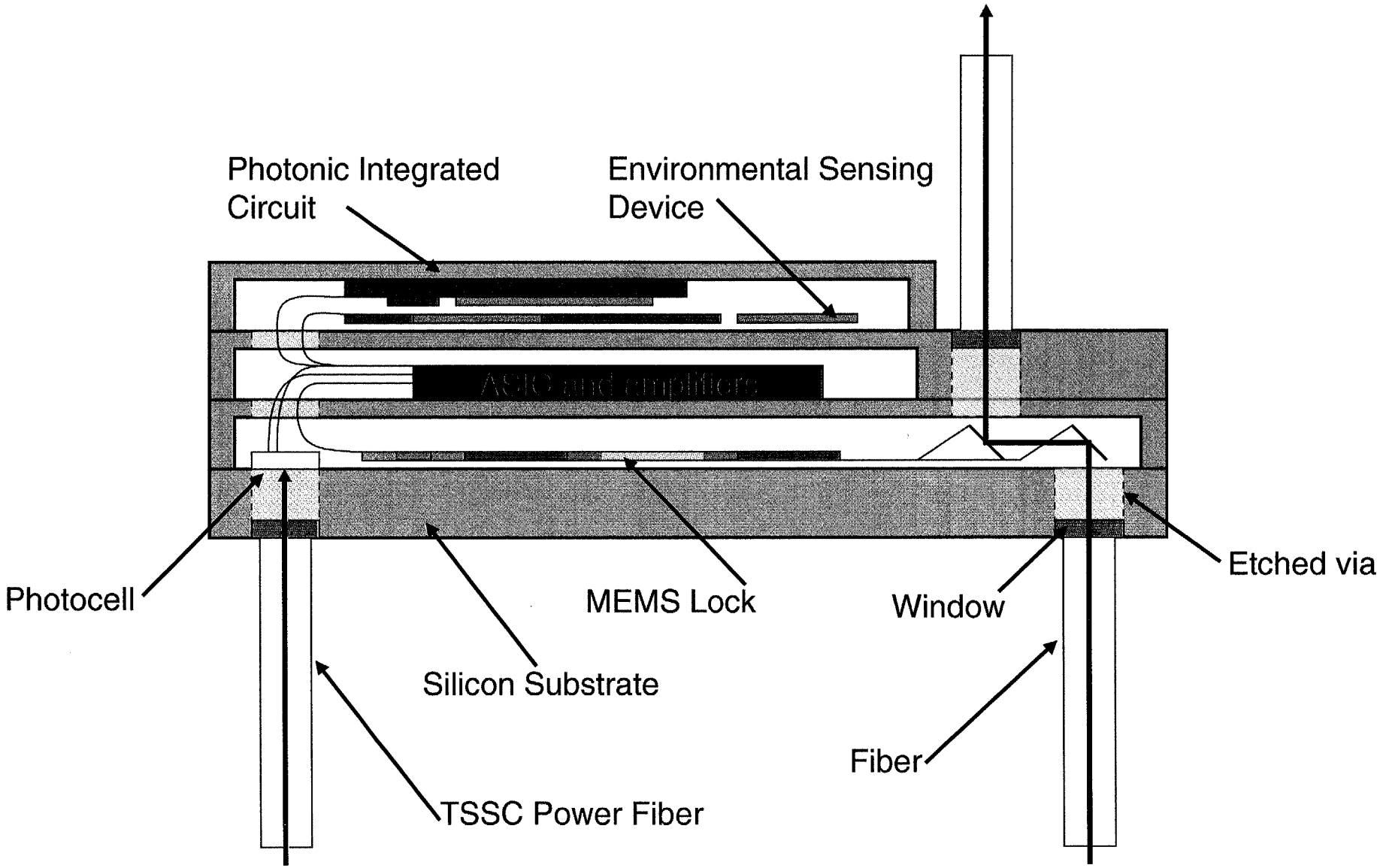
Photonic Integrated Circuit
Environmental Sensing Device
ASIC and amplifiers
Photocell
Silicon Substrate
MEMS Lock
Window
Etched via
Fiber
TSSC Power Fiber

Figure 4

SIDEBAR

Film Flatness (Curl and Topography)

Flatness can be categorized as global and local from a micromachining fabrication perspective. Global flatness is primarily affected by gradients in mechanical stress throughout the film thickness, often producing a "potato chip" effect in micromachined mirrors. Local flatness of the topmost layer, over lateral dimensions of microns to tens of microns, is influenced by the topography of the previously patterned layers.

Figure 1 illustrates the importance of proper thermal annealing cycles to achieve global flatness. The test structures are two 20 μm wide cantilever-supported microbeams, one 600 μm long and the other 1500 μm long. The 600 μm beam has only been subjected to a partial thermal anneal, while the 1500 μm long beam has seen a full thermal anneal at 1100 °C, to relieve residual mechanical stress gradients. The top view of the beams are shown in Figure 1, taken with an interferometric microscope, in which the deflection of the beam (z-height) is calculated from the fringe spacing. For the 600 μm partially annealed beam, the film has significant curl resulting in the end of the beam being deflected approximately 4.5 microns above the base, which corresponds to a radius of curvature of 41 millimeters. In the case of 1500 μm long, fully annealed beam, there is only a 1 micron deflection, corresponding to a much larger radius of curvature of 1 meter, demonstrating a high degree of global flatness.

Chemical Mechanical Polishing (CMP) of MEMS has been developed at Sandia to improve local flatness, by eliminating the topography of previously patterned films on the top mirror surface. Figure 2, an SEM image of a piston mirror fabricated in the SUMMiT-IV Technology, shows how each of the four polysilicon layers are patterned, and the topography that is generated. It is important to note that although significant topography exists in the underlying poly layers, since SacOx 3 (*see article*) is planarized, the top (Poly 3) layer is optically flat, displaying none of the underlying topography.

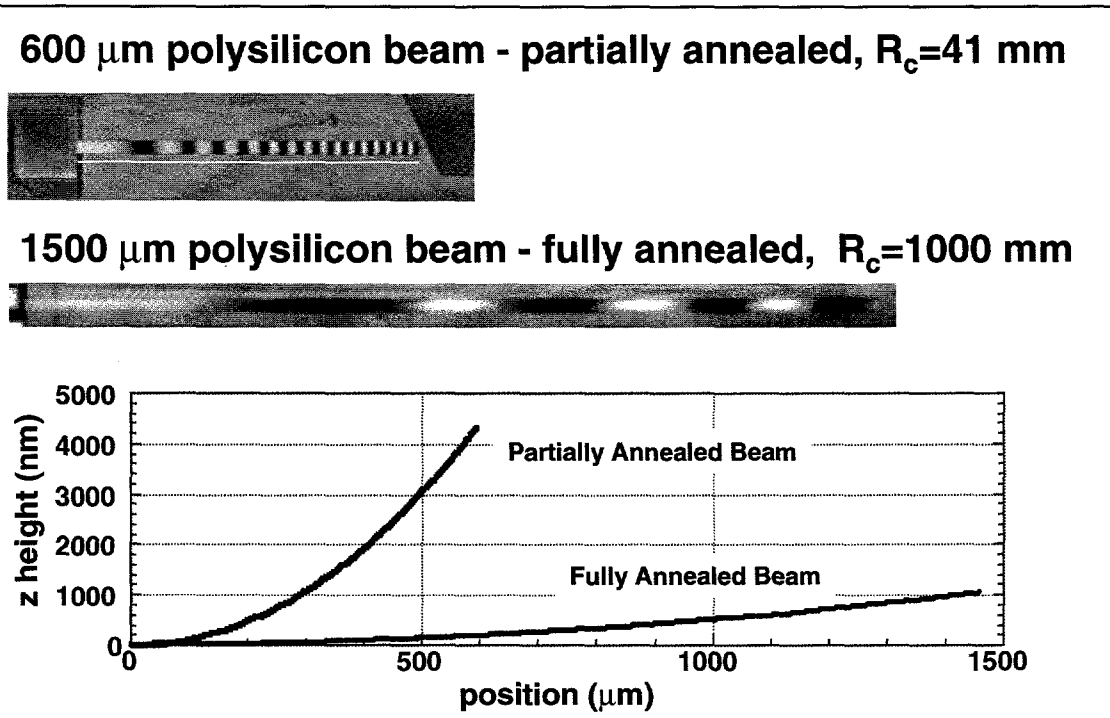

Figure 1 Interferometeric measurements showing the deflection of a 600 μm, partially annealed beam and a 1500 μm long fully annealed beam.

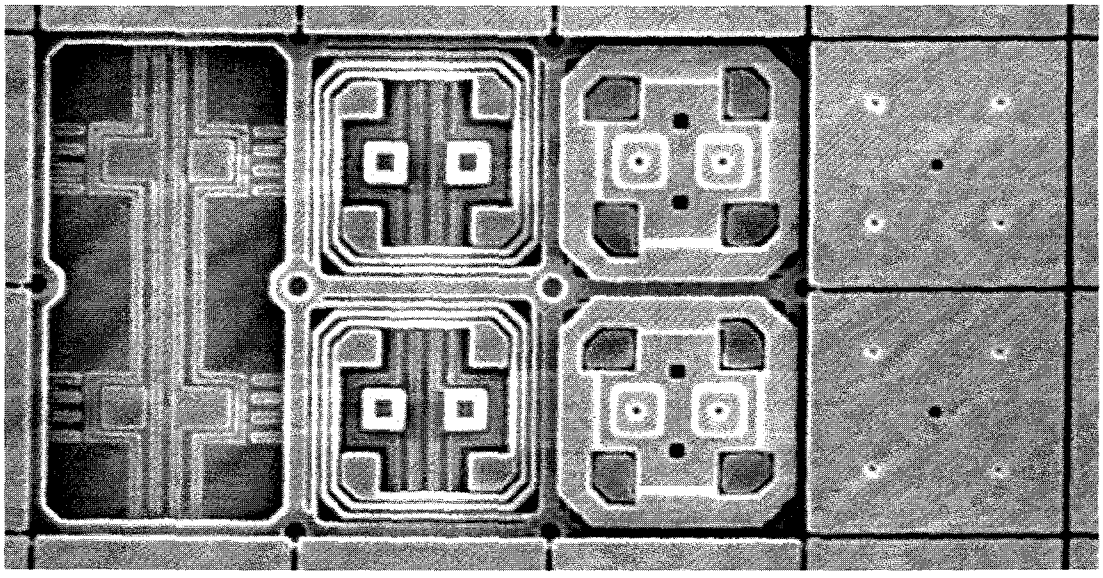

Figure 2 SEM image of a piston mirror showing the underlying topography generated (*left to right*) in Poly 0, Poly 1 and Poly 2. By planarizing the oxide beneath Poly 3, the mirror surface is optically flat (far right).