August 1998 • NREL/CP-520-25232

Eighth Workshop on Crystalline Silicon Solar Cell Materials and Processes

Extended Abstracts and Papers

August 17–19, 1998
Copper Mountain, Colorado
Workshop Chairman: B.L. Sopori

Program Committee:
R. Sinton, T. Tan, J. Kalejs, J. Gee, M. Stavola, T. Saitoh, R. Swanson, and B. Sopori

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
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for the U.S. Department of Energy
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August 1998

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Eighth Workshop on
Crystalline Silicon Solar Cell Materials and Processes

TABLE OF CONTENTS

Title/Author(s): **Page**

Opening Remarks 1
Richard J. King, Photovoltaic R&D Program, U.S. Department of Energy

Workshop Theme: ***Supporting the Transition to World Class Manufacturing*** 7
Bhushan Sopori

Polycrystalline Silicon – World Demand and Supply 10
J. Maurits

Polysilicon Production in the Commonwealth of Independent States 18
D. S. Strebkov, A. Pinov, V. Zadde, Y. S. Tsuo, K. Touryan,
L. Murphy, and J. M. Gee

String Ribbon – A New Silicon Sheet Growth Method 22
R. L. Wallace, R. E. Janoch, and J. I. Hanoka

Status of EBARA Solar, Inc. 26
Daniel L. Meier

Status and Issues of Crystalline Silicon Solar Mateirals and Devices in Japanese PV Market 30
T. Saitoh

Behaviour and Influence of Defects in "Photovoltaic" Silicon Wafers 35
S. Martinuzzi and I. Périchaud

Feedstock Evaluation for Czochralski Grown Silicon Solar Cells 37
J. Palm, A. L. Endrös, G. Mihalik, A. Matthäus, and T. Jester

Physics of Impurity Gettering in PV Silicon 42
T. Y. Tan, P. Plekhanov, S. Joshi, R. Gafiteanu, and U. Gösele

Lifetime Studies of Multicrystalline Silicon 50
Andrés Cuevas

Minority Carrier Lifetime and SPV Investigations in PV 60
Tibor Pavelka and Roy Herlocher

Present Status of the Surface Photovoltage Method (SPV) for Measuring Minority Carrier Diffusion Length and Related Parameters 61
L. Jastrzebski and J. Lagowski

Texturization Technologies of Multicrystalline Silicon 62
Peter Fath

Advances in Solar Cell Metallization in the Manufacturing of High Efficiency Silicon Solar Cells 63
T M Bruton

Selective-Emitter Solar Cells – From Laboratory to Production Processes 69
J. Szlufcik, J. Horzel, F. Duerinckx, R. Einhaus, E. Demesmaeker, J. Nijs, and R. Mertens

PECVD Deposition of Silicon Nitride: Fundamentals and Prospects for Industrial Application 77
Armin G. Aberle, Jens Moschner, and Rudolf Hezel

PECVD Silicon Nitride: Commercially Compatible Process for Solar Cell Fabrication 85
Arun Madan

Recent Progress in Rapid Thermal Processing of Silicon Photovoltaic Devices 86
P. Doshi, A. Rohatgi, A. Ebong, and S. Narasimha

RTP of Silicon Solar Cells – Lifetime Effects and Spectral Engineering 94
R. Schindler

Light Induced Effects in Rapid Thermal Diffusion Processes From Doped Oxide Sources 102
S. Noël, A. Slaoui, J.C. Muller

Recent Experimental and Theoretical Results for H_2 in Si 110
Michael Stavola and S. K. Estreicher

Thin Film Si Solar Cells: A Review of Material Issues and Device Design Concepts 118
Bhushan Sopori and Wei Chen

Thin Crystalline Si Solar Cell Research Activities in NEDO Sunshine Project s 119
Takashi Fuyuki

High Temperature Substrates for Thin Film Poly-Si Electronics 123
Dieter G. Ast

A Review of Hotwire Deposition of Amorphous and Microcrystalline Si 131
Richard Crandall

Poster Papers **Page**

Cross-Contamination as a Novel Technique for Studying Impurities in Multicrystalline Silicon 132
D. Macdonald and A. Cuevas

Defect Characterization in PV Polycrystalline Silicon Using Room-Temperature Photoluminescence 137
Y. Koshka, S. Ostapenko, S. Koveshnikov, and B. Sopori

Interstitial Copper in Silicon 141
Andrei A. Istratov, Christoph Flink, Thomas Heiser, Henry Hieslmair, and Eicke R. Weber

Chemical State and Elemental Distribution of Metal Impurities in Polycrystalline Silicon Solar Cells 145
S. A. McHugo, G. Lamble, I. Périchaud, and S. Martinuzzi

Comparison of Residual Strains in Different Silicon Materials for Solar Application 149
E. Wolf and S. Bergmann

Improvement of Material Parameters of Silicon by Gettering 153
A. A. Istratov, S.A. McHugo, H. Hieslmair, and E. R. Weber

Minority Carrier Lifetime Determination on As-Sawn Ingot Surfaces of Cz-Si 169
D. Sheadel, A. Matthäus, G. Mihalik, A. Smith, J. Coleman, J. Palm and T. Jester

Emissivity Measurements and Modeling – A Summary 174
N. M. Ravindra, F. M. Tong, and S. Abedrabbo, B. Sopori, and W. Chen

Silicide Assisted Crystallization of Thin Poly-Si Films 186
Dieter G. Ast

Nanosized Al and Ag Particulate Contacts to Silicon: Materials Characterization and Preliminary Electrical Results 188
Douglas L. Schulz, Calvin J. Curtis, David S. Ginley, and Fred Tepper

Some Thermochemical Calculations on the Purification of Silicon Melts 192
James M. Gee, Pauline Ho, James Van Den Avyle, and James Stepanek

Emission and Capture Trapping Lifetimes of the n-Type Silicon Wafers Evaluated Using Frequency Resolved Microwave Photoconductance Method 196
A. Romanowski, A. Buczkowski, A. Karoui, and G. Rozgonyi

Applications of PVSCAN5000 for Analysis of Wafer Defects and Solar Cell Performance 199
B. L. Sopori, W. Chen, and J. Madjdpour

Characterization of Phosphorus Gettering Process for Multicrystalline Silicon Wafers by Surface Photovoltage 203
T. Saitoh, S. Inoue, and S. Ishikawa

Light Induced Defect Reactions in Boron-Doped Silicon: Cu versus Fe 207
I. Tarasov, S. Ostapenko, and S. Koveshnikov

Improvement of Carrier Lifetime in Silicon by Gettering of Precipitated Impurities 211
P. S. Plekhanov, U. M. Gösele, and T. Y. Tan

Use of Design of Experiments and Balanced Analysis of Variance for Statistical Wet-Line Process Control 215
Aimée Smith, Vijay Pandrangi, Robert Zinner, John Coleman, Theresa Jester, and Lionel C. Kimerling

Investigation of Post-Growth Treatments of Silicon-Film ™ 219
Y. Bai, M. G. Mauk, J. R. Bower, J. R. Cummings, J. A. Rand, and A. M. Barnett

Film Silicon Solar Cells on Ceramic Substrates 221
A. von Keitz, S. E. A. Schiermeier, A. J. M. M. van Zutphen, C. J. J. Tool, F. Fung, J. A. M. van Roosmalen, and G. M. Christie

Improved Performance of Self-Aligned, Selective-Emitter Silicon Solar Cells 225
D. S. Ruby, P. Yang, S. Zaidi, S. Brueck, M. Roy and S. Narayanan

Recent Advances in Silicon-Film ™ Solar Cell Manufacturing Engineering 229
J. S. Culik, R. Cole, E. DelleDonne, and E. Jackson

Effective Surface and Bulk Defect Passivation of Low Resistivity Multi-crystalline Silicon by Annealed RTO/PECVD SiN Stack 232
A. Ebong, V. Yelundur, and A. Rohatgi

A Rapid Thermal Oxide/PECVD Silicon Nitride Stack for Effective Passivation of Low Resistivity Silicon and Phosphorous Diffused Emitters 236
A. Rohatgi, S. Narasimha, P. Doshi, J. Moschner, and D. S. Ruby

Approach Towards High Efficiency, Manufacturable Thin String Ribbon Silicon Solar Cells 240
V. Yelundur, A. Ebong, S. Kamra, A. Rohatgi, J. Hanoka and A. Gabor

Evolution of Defect Electrical Activity in Silicon Wafers During Processing Steps by LBIC Scan Maps at 80K 244
I. Périchaud

Using PV Optics for Solar Cell and Module Design 247
Bhushan Sopori, Jamal Madjdpour, and Wei Chen

Self-Doping Contacts and Associated Silicon Solar Cell Structures 251
D. L. Meier, H. P. Davis, A. Shibata, T. Abe, K. Kinoshita, C. Bishop, S. Mahajan, A. Rohatgi, P. Doshi, and M. Finnegan

Opening Remarks by
Richard J. King
Team Leader
Photovoltaic R&D Program
U.S. Department of Energy

Photovoltaic Budget
($1000)

	FY 1995	FY 1996	FY 1997	FY 1998
Appropriation	91,000	65,000	60,000	66,511
Uncosted/General Reduction	(6,165)	(4,910)	(4,200)	(4,339)
Total Operating Funds	84,835	60,090	55,800	62,112

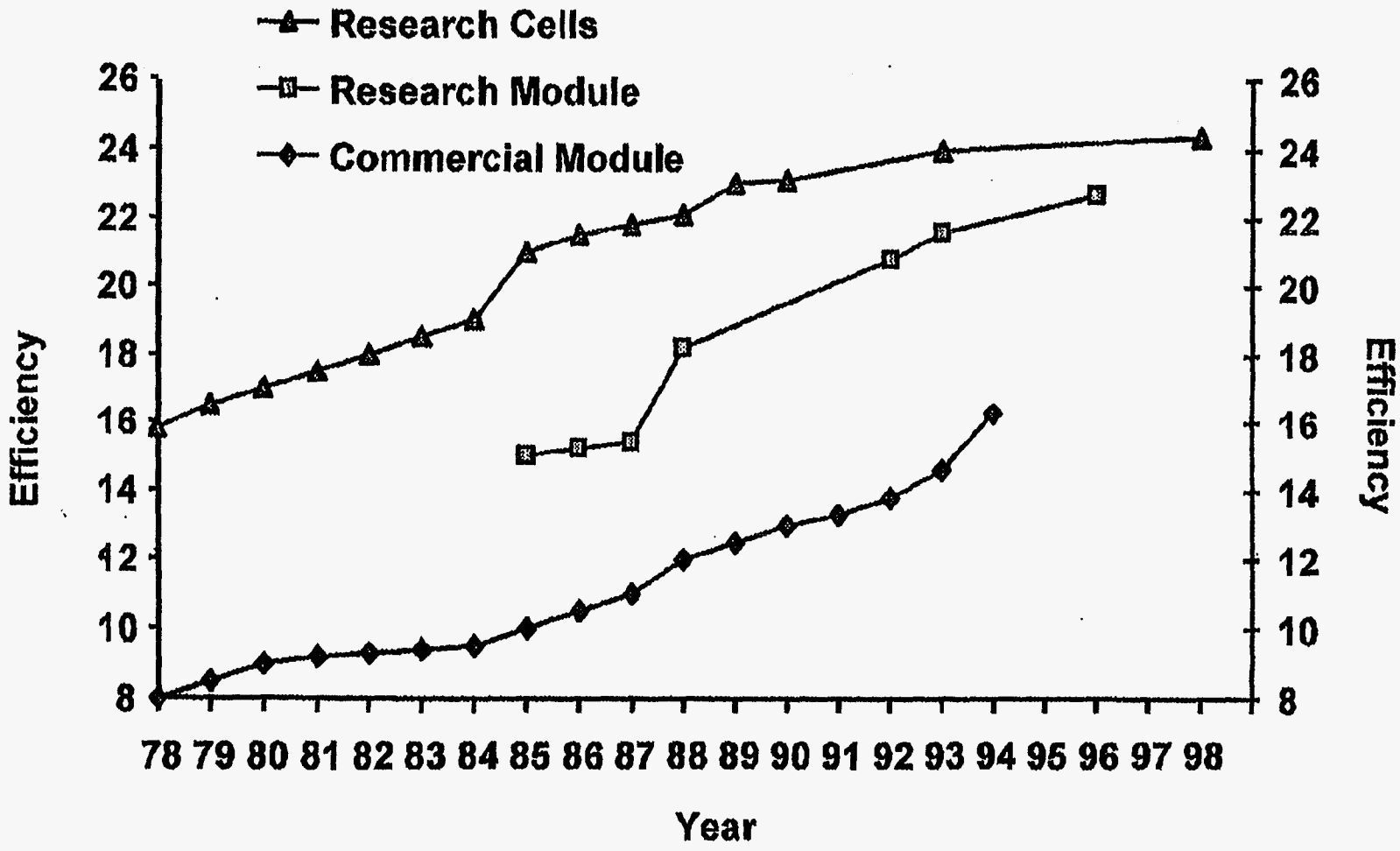
FY 1999 Photovoltaic Budget Request
($ 1000)

Fundamental Research	11,000
Advanced Materials & Devices	27,000
Collector Research & Systems Development	40,800
	78,800

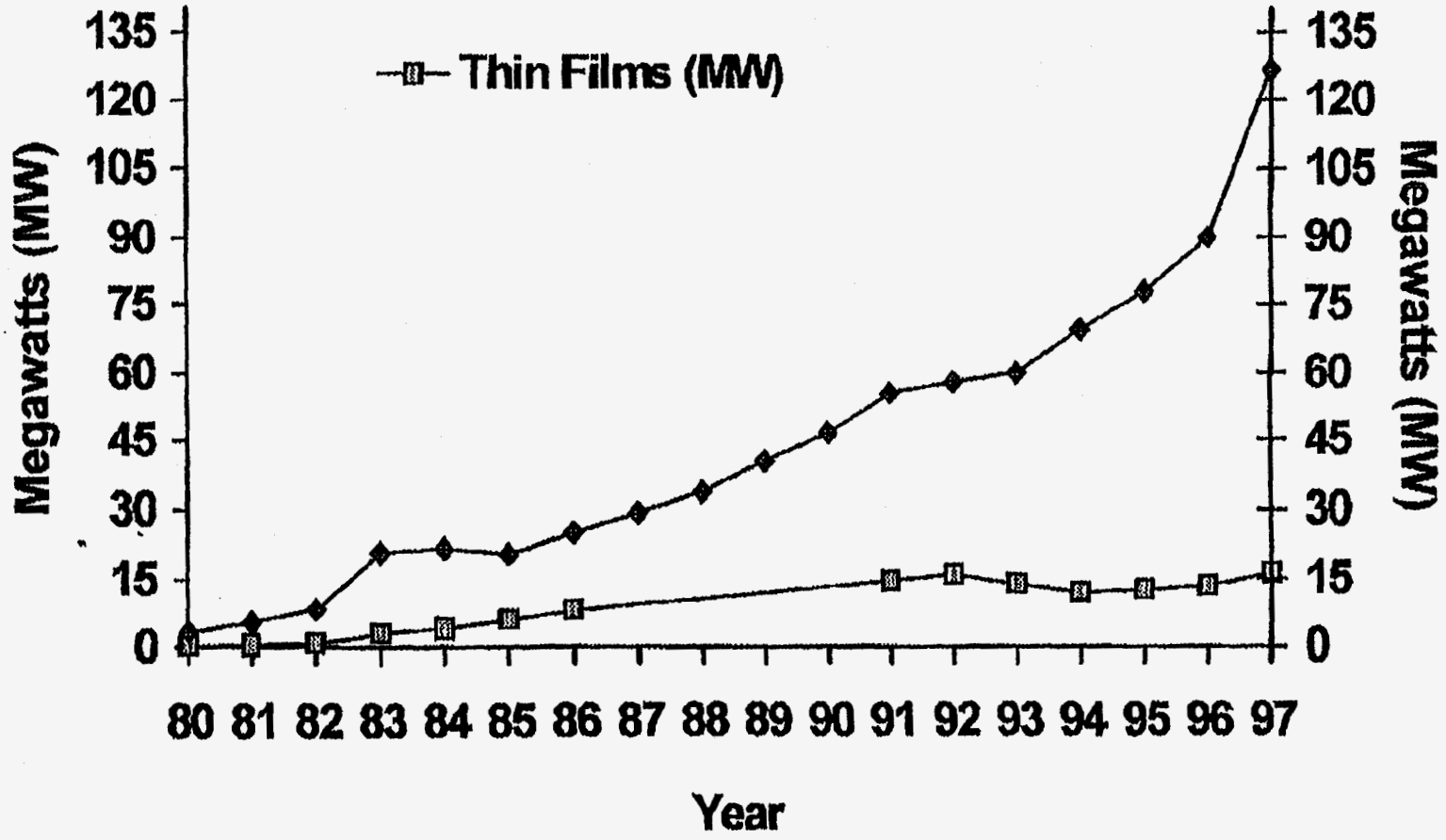
Requested increases in PVMaT, reliability, PV:BONUS and MSR

House Mark:	66,800
Senate Mark:	57,110
Senate Amendment:	72,900
Conference Committee Settlement:	TBD

Crystal Silicon
Cell and Module Efficiency Records



World Photovoltaic Cell and Module Shipments



Impact of Efficiency & Direct Manufacturing Cost for Silicon Technology ($/W)

	$300/m2	$250/m2	$200/m2	$150/m2
10%	$3.0	$2.5	$2.0	$1.5
12%	$2.5	$2.08	$1.67	$1.25
15%	$2.0	$1.67	$1.33	$1.0
18%	$1.67	$1.39	$1.11	$0.83

Cost/Watt ($/Wp) = (Manuf. Cost/m2) / (Watts Output/m2)

Foreign Competition is Strong

Japanese PV manufacturers reported shipment increases of 65%, from 21.2 MW in 1996 to 35 MW in 1997. Kyocera reported that 1997 shipments were up 69% to 15.4 MW. Sharp reported 1997 shipments up 112% to 10.6 MW.

Japanese PV Cell & Module Shipments (MW)

Company	1994	1995	1996	1997
Kyocera	5.3	6.1	9.1	15.4
Sharp	2.0	4.0	5.0	10.6
Sanyo	5.5	5.1	4.6	4.7
Others	3.7	2.2	2.5	4.3
Total	16.5	17.4	21.2	35.0

Kyocera subsidiary Kyocera Solar Corp. (Established November 1996) will spend $83 million to quadruple its annual solar cell production capacity to 60 MW by April 1999 from 15 MW now, and to 36 MW by March 1998 after constructing a new plant next door to its existing Shiga Prefecture plant. The existing plant currently produces 1.3 MW of solar cells monthly for residential solar power-generation systems.

Kyocera is aiming for sales of $500 million in 2000, figuring on a share equivalent to 50 percent of the $1billion Japanese solar market being forecast by Kyocera executives. Kyocera currently claims about half the Japanese residential (subsidized) market for solar cells.

Kyocera is aiming to cut the price of its solar cell systems in half by 2000, so that a 3-kW residential solar cell system will cost $12,500. Kyocera figures the normal household (which pays about $0.25/kWh for electricity) would save $667 yearly on electricity costs (with net metering) using a 3-kW system.

With research support from the Japanese government, Kyocera announced a world-record conversion efficiency of 17.1 % last November for its polycrystalline silicon solar cell with a large 15cm X 15cm surface area. For this product, Kyocera used a reactive ion etching (RIE) method to furnish the solar cell with a textured surface, and to reduce reflections. Current efficiency of the company's volume produced cells is 14.9%, although Kyocera intends to introduce its new RIE technology into its manufacturing process to raise its cells to the 17.1% level by 2000.

This information was obtained from the Department of Energy's Office of Intelligence report "INTERNATIONAL: Solar Cells Outlook" *dated March 1998.*

Two Messages

DOE will continue to support X-Si research. When we look for near- and mid-term results on investment, we believe X-Si research will continue to pay dividends.

Strengthen the partnership between Laboratory/University Research and Industrial Manufacturing.

Supporting the Transition to World Class Manufacturing

(Workshop Theme)

Bhushan Sopori
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1617 Cole Boulevard
Golden, CO 80401

The theme of the 8th workshop is "*Supporting the Transition to World Class Manufacturing.*" This theme reflects a worldwide growing demand for the photovoltaic (PV) energy, and the concomitant issues that will arise as the PV industry undergoes a transition to become a world class manufacturing technology. Figure 1 shows the sales of PV energy in the last seven years. It indicates an average growth of about 20% per year, with a step increase of about 40% in 1997. Figure 1 also shows the breakdown into silicon-based and thin-film-based PV sales. Nearly 90% of the PV industry is Si-based, and this trend is likely to continue in the near future as other materials technologies mature. In 1997, for the first time, the PV sales surpassed a 100-MW mark, representing total sales of about one billion dollars – an indication that PV is beginning to establish itself as a world class industry. This achievement brings a host of new challenges that must be met to support the growth. Of particular interest to this audience is that further advances in both the materials growth and device fabrication need to come from the industry as well as from the academic institutions. Hence, a strong dialogue between industry and academic institutions is essential to help define industry needs and build mechanisms for commercializing research results.

This workshop is one of the ways to collectively address the research issues of interest to the PV community in general, and more specifically to that of the Si-PV industry. It provides an informal forum where industry, academia, and national labs can ponder over the issues and challenges to the Si-PV community. The workshop's objectives include:

1. Identifying research areas of major importance in the Si-PV manufacturing that will help lower the cost of PV energy,
2. Establishing opportunities for performing research collaborations between universities, industry and the national laboratories, and
3. Disseminating the results in a timely manner.

Because these challenges change as the existing technologies mature and new technologies appear, the emphasis of the workshop must address these issues in a timely manner. It necessitates a "dynamic" formulation of the workshop. To this end, we have changed the title of the workshop three times in the last seven years — from Role of Point Defects in Silicon Device Processing, to Role of Impurities and Defects in Silicon Device Processing, to Workshop on Crystalline Silicon Solar Cell Materials and Processes. These changes reflect the emphasis of the basic research under the University Si Program.

The challenges to the PV industry will come from a multitude of directions: identification of the sources of starting materials and attaining self sufficiency in raw materials; inclusion of advanced processes into production to foster higher efficiencies and higher yields in manufacturing; incorporating automation in manufacturing, handling and processing of thin wafers and cells; and increasing the throughput and lowering system costs.

- **Feedstock and wafer supply**: During the last couple of years, there has been a shortage of polysilicon feedstock and wafers available to the PV industry. This seems to have been related to the excess demand posed by the microelectronic industry in a period of gearing up for 300 mm wafers. Continued scarcity could have major detrimental effects on the PV industry. Very recently, however, the growth of the microelectronic industry has slowed down as a result of the shaky Asian economy. This has somewhat helped the polysilicon feedstock availability to PV manufacturers. Clearly, the PV industry would like to see a dedicated supply of "PV-Si." A number of approaches to obtain lower-grade, low-cost, polysilicon are being assessed. Details of these approaches will be covered in Session 1 on "Feedstock Issues and Wafer Supply," and in a discussion following this session.

- **Improved material quality**: Defects, impurities, and impurity gettering has been well investigated in last eight years, and a great deal of new understanding has been acquired. The Si-PV community has learned that very effective gettering of impurities can be performed in most substrates by conventional cell fabrication processes. Recent results have shown that the regions of the cell containing defect clusters are difficult to getter because they are sites of precipitated impurities. In a solar cell these regions appear as shunts that degrade the cell performance. Analysis has shown that in current high-quality, commercial multicrystalline wafers, the primary limiting mechanism is associated with the defect cluster regions. Solar cell performance reaching 18% on these substrates appears to be possible if the effects of these regions can be mitigated. These issues will be addressed in Session 3, "Material Issues" and an "Open Discussion" following that.

- **Advanced diagnostics**: Like many other areas (e.g., device processing), the Si-PV industry has attempted to adopted monitoring methodology similar to that of the microelectronics industry. It is rather clear that the PV industry will require different methods for monitoring wafer quality, surface characteristics, antireflection coating parameters, and junction properties. Session 4 will discuss these issues.

- **Lower-cost solar cell processing**: This is an area in which a high degree of understanding has been acquired. In particular, the understanding of impurity gettering by phosphorous diffusion and of Al alloying has been greatly improved. Other cell processing steps such as PECVD nitride deposition, impurity and defect passivation, and texturing for light trapping have been well developed. It is recognized that conventional methods of processing that address one functional step in one process will be replaced by developing processes that accomplish a number of functions. For examples, simultaneous formation of front and back junctions and contacts, and one-step deposition of AR coating and hydrogenation can significantly lower cell fabrication costs. These processes will be addressed in Session 5.

• **Hydrogen passivation**: Although hydrogen passivation is used commercially, the understanding of passivation mechanisms is very weak. To date, only a few types of substrates respond well to hydrogen passivation. This effect appears to be related to the diffusivity of hydrogen in different types of Si. However, one of the issues not well understood is the mechanism(s) of passivation of transition metals by hydrogen.
These issues will be addressed in the Session 6.

• **Thin film silicon cells**. Thin film Si cells offer an opportunity to not only lower the cost of PV energy but also greatly lower Si consumption. Two essential requirements of a thin cell are to have very effective light trapping and grain size much larger than the film thickness. The low-cost requirement necessitates the use of a low-cost substrate like glass. It is rather clear that very effective light trapping can be accomplished in thin Si. Photocurrents of 26 mA/cm^2 have been attained in 3 μm-thick cells. The major issues are to have large grain size and high purity in thin films so that one can obtain open- circuit voltages in excess of 600 mV.

This workshop will address a number of issues that are important to making Si-PV a world class industry. As in the past, the participants will collectively resolve the issues and define the direction(s) for future research.

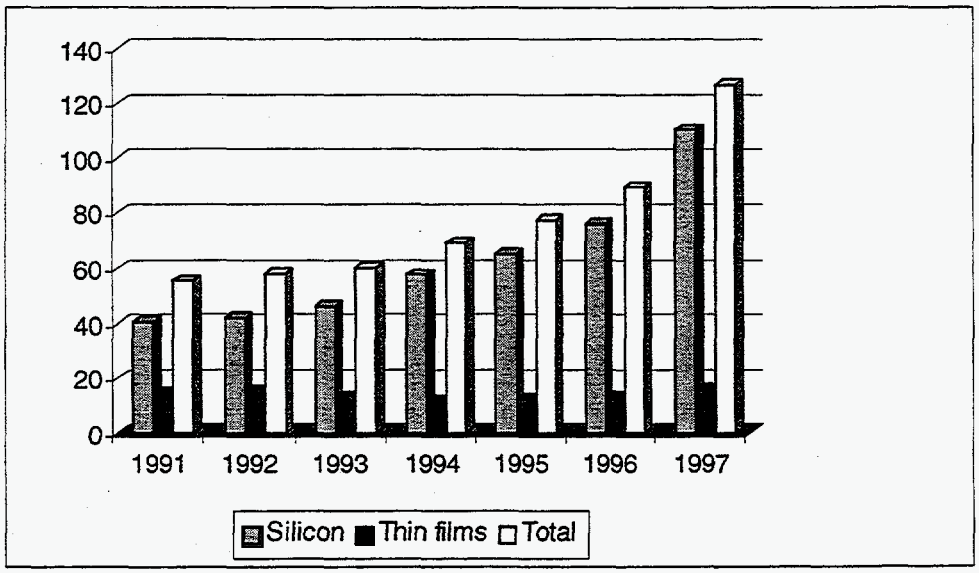

Figure 1. World PV Energy sales (in MW) in last seven years

POLYCRYSTALLINE SILICON – WORLD DEMAND AND SUPPLY

J. Maurits
Advanced Silicon Materials Inc
Moses Lake, Washington

ABSTRACT

The current and forecasted polycrystalline silicon production capacity for the six major producers is charted and discussed. Supply, demand, and pricing for polysilicon for the semiconductor industry are shown, with the forecasted demand for the photovoltaic industry. To obtain inexpensive feedstock, the PV industry has used secondary grade polysilicon. The sources and capacity limitations for this material are discussed. The PV industry will not be able to rely on secondary grade polysilicon for the volumes needed. Options for production of a low-cost solar grade polysilicon feedstock are discussed.

POLYSILICON PRODUCTION

In 1995, a shortage of polycrystalline silicon developed due to rapidly increasing demand from the semiconductor industry; this demand exceeded the installed capacity of the polysilicon producers. As seen in Figure 1, the producers responded with increased capacity and expansion plans to double production by the year 2000. [1-4] An immediate capacity gain, about 10%, was achieved by increasing production to the maximum at existing facilities, upgrading some secondary grade polysilicon, and reducing the amount of secondary grade produced. Major expansions required new facilities and these were designed for 1000 to 5000 metric tons per year for economy of scale. The silicon wafer producers supported funding of the new capacity by long-term contracts for committed volumes and prices, and by equity positions. The installed capacity is designed to produce polysilicon to meet the requirements for high purity, specific size distribution, and clean room packaging at prices of $50 to $60 per kg.

The worldwide shortage continued into 1998, when the new polysilicon capacity came on-stream and demand slowed due to the reduction in DRAM production and the delay in 300 mm wafer production. The current planned capacity expansions are expected to be completed by 2002, at 29,000 metric tons per year. It is expected that the semiconductor industry will continue overall growth at 10 to 15% per year, requiring a new round of capacity expansion by 2002 – 2004.

During the three-year polysilicon shortage, the PV industry found that the traditional sources of secondary grade polysilicon at inexpensive prices, $5 to $20 per kg, were no longer readily available, and prices were significantly higher. The wafer manufacturers used much of this material for monitor wafers and prime wafer production. With the strong growth in the PV market, the PV industry has realized they can no longer rely on inexpensive, secondary grade polysilicon to meet feedstock requirements. Feedstock is a strategic issue that must be addressed to allow continued growth of the market.

Pricing has followed the supply/demand curve, as shown in Figure 2. Semiconductor grade polysilicon prices have been as low as $38 per kg. This price does not allow recovery of new investment costs and does not justify continued expansions of new capacity. Since polysilicon capacity is added in typically1000 ton increments when demand has pushed prices up to justify the investment, the cycle of oversupply and shortage is expected to continue. The major silicon wafer producers have attempted to protect their supply sources by purchasing equity positions in the polysilicon supplier companies, committing to take-or-pay contract amounts, or forming partnerships.

SOLAR GRADE POLYSILICON

The dramatic growth in photovoltaic electrical generating systems since 1996 has focused attention on feedstock as a serious strategic issue. The projected demand [5-6] for solar grade polysilicon is shown in Figure 3, based on a conversion of 20 metric tons of polysilicon for 1 megawatt of electricity. Given current projections of 15 to 20% annual growth, 800 MW (16,000 tons) will be required by 2010. Growth could be as large as 1600 MW (32,000 tons) by 2010, assuming continued governmental subsidies and funding. Historically, the PV industry has used secondary polysilicon, about 10 to 15% of total polysilicon production, as the feedstock for silicon ingot production. This secondary grade material does not meet the purity, size, or cleanliness requirements for the semiconductor industry, so is sold on an as-available basis at prices less than $20 per kg. The projected supply of this secondary material is shown in Figure 3, assuming that 10 to 15% of total poly production is available at < $20/kg. The supply is inadequate to meet demand by 2003. By 2006, assuming 5000 tons of secondary poly is available, the shortfall of PV feedstock will be 3000 tons and may be as much as 11,000 tons. A dedicated source of solar grade polysilicon is needed to support continued growth of the industry.

Polysilicon plants must be designed to produce feedstock at a minimum of 5,000 tons per year and be in production with target prices of $20 per kg by 2003 to assure the projected growth in PV. By 2010, production of PV feedstock at a rate of 8,000 to 24,000 tons per year is needed. This will require a large amount of capital and engineering resources. Construction time for a green-field polysilicon plant, with an established design, is typically 18 to 24 months.

POLYSILICON MANUFACTURING TECHNOLOGY

There have been several approaches to producing a solar grade feedstock. Economic analysis, engineering approaches, and experimental results for most of these have been studied in U. S. Department of Energy programs. [7] To produce a low cost feedstock, attempts have been made to refine metallurgical grade silicon and to reduce silicon oxide. While having the potential of low cost production, the purity has not been acceptable, requiring more expensive refining processes. These approaches have not been able to produce an acceptable feedstock at prices less than $20/kg. With the projected shortage of feedstock, some of these approaches may be revisited.

Semiconductor grade polysilicon is produced by the thermal decomposition of trichlorosilane or silane in large Siemans-type chemical vapor deposition reactors. These reactors are large stainless steel chambers containing a filament mounting and heating system. The source gas is introduced into the chamber and decomposes onto the heated high purity silicon filament, growing into poly rods about 2 meters in length and 125 mm in diameter. The poly rods are then broken into chunks and packaged under clean room conditions. Some of the poly rods are machined into specific sizes for float zone crystal growth. The process at Advanced Silicon Materials is shown schematically in Figures 4 and 5. These systems are designed to produce high purity polysilicon, with boron <0.03 ppba, phosphorus <0.2ppba, carbon <0.2 ppma, and surface metals <5 ppbw.

Polysilicon that does not meet the purity, size, or surface cleanliness/appearance specifications is classified as secondary grade and is available to the PV industry. Sources of the secondary poly are filament pieces, chunks with bulk impurities or surface contamination (metals, powder, stains, surface texture), rod sections with sawn ends/fabricated surfaces, chunks with graphite chuck remnants, small diameter rods, and chips and fines. Each of these is produced in different quantities depending on product mix and processing yield and have different values. Some of the material can be used in the casting processes, but not the Cz processes for PV ingot growth. Total secondary material is about 10% of production, but this is decreasing to about 5% as more efficient reactors, new reactor designs, robotic handling, and process improvements are implemented. In addition, the growing markets for test and monitor wafers, special semiconductor devices, and alloying applications compete for the secondary poly, increasing prices and reducing availability. Secondary grade material is also available from the silicon wafer suppliers; sources are crucible remnants, ingot seed and tang ends, and chips and fines from ingot fabrication. About 10% of the silicon melt remains in the crucible at the end of the growth run. About 20% of the Cz silicon ingot is cut off when removing the seed and tang ends. The crucible remnants require further processing to remove quartz before using. The seed and tang end sections are desirable, but the test wafer market is willing to pay higher prices for this material. The major trend in ingot production is for wafers with heavier doping levels, which limits the usefulness for PV feedstock. It is estimated that total secondary grade material available for PV feedstock at < $20/kg will be 10 to 15% of total polysilicon production.

OPTIONS FOR SOLAR GRADE POLYSILICON

The SOGA Project at Kawasaki Steel, sponsored by NEDO, the Japanese government energy agency, is a process to refine metallurgical grade silicon by multiple purification steps. A pilot production line is expected to be in operation in 1999. Other approaches for production of a PV feedstock are being evaluated.

At this point, we believe there are three options for producing the large volumes of PV feedstock required by 2003 at the price range of $20 to $25 per kg. These are production of solar grade polysilicon in a high efficiency filament reactor, production of low-cost granular polysilicon, and production of fine silicon powder in a free space reactor. Silane is chosen as the source gas because it can be produced economically in a closed loop,

continuous process; can be produced from commercially available, inexpensive raw materials; can be produced with no hazardous wastes; and can be produced in large volumes at high purity. Silane is preferred as the source gas for granular poly production, and for the free space reactor.

ASiMI's silane process, shown in Figure 4, has been designed for production of high purity silane. For solar grade feedstock, the hydrogenation reaction rate could be increased, the final purification step eliminated, and other steps reduced or combined to reduce production costs. This would result in higher levels of light gases and acceptor/donor impurities, but acceptable for PV applications.

To meet immediate and short-term feedstock needs, a high efficiency filament reactor could be used for production of a dedicated volume of solar grade polysilicon. Existing silane capacity and installed reactors could be used to produce a defined reduced purity, with bulk packaging, at about $30 per kg. The price may be higher than the PV feedstock target, but would allow PV production until a lower cost process can be established and installed.

To be in production of <$25/kg solar grade poly by 2003, granular polysilicon is the best option. Advanced Silicon Materials (Union Carbide) studied the production of granular poly from silane in 1974 for the Department of Energy Flat-Plate Solar Array Program. The program was completed and further development halted in 1986. In 1994, ASiMI began development of granular poly for the semiconductor industry, and installed a laboratory scale fluid bed reactor at the Moses Lake plant. Experimental runs are being made with this reactor to define bead size, size distribution, purity levels, operating parameters, run lengths, capacity, and costs. The existing silane capacity and fluid bed reactor could be used to define and develop a solar grade granular poly in one to two years with the allocation of funding and resources. After defining the process, new silane capacity and fluid bed reactors to supply 5000 tons/year could be installed by 2003.

A longer-term option is the production of PV feedstock based on fine powder from a free space reactor. The free space reactor was studied in 1974 for the Flat-Plate Solar Array Program. A fine silicon powder was produced from this reactor. Since the process for melting the powder and loading into a crucible for PV ingot growth was not developed, no further development of the free space reactor was done. This has the potential for being the lowest cost solar grade poly, but needs extensive development.

CONCLUSION

To meet the projected demand for solar grade polysilicon, the PV industry has less than 5 years to select a process technology and design, build, and commission a large capacity production plant. The traditional supply of secondary grade polysilicon at < $20 / kg from the semiconductor poly suppliers is inadequate to serve the current demand and a serious shortfall is expected by 2003. For the short term, until production capacity can be installed, high-efficiency filament reactors can be used to produce dedicated volumes of a defined solar grade polysilicon at prices about $30/kg. Fluid bed reactors producing

granular solar grade polysilicon are the best option for large volume production by 2003 with prices about $20/kg. The free space reactor may be the best option for prices less than $20/kg, but will take significant development. The polysilicon producers need financial and resource commitments from the PV industry to develop the technology and install the necessary capacity.

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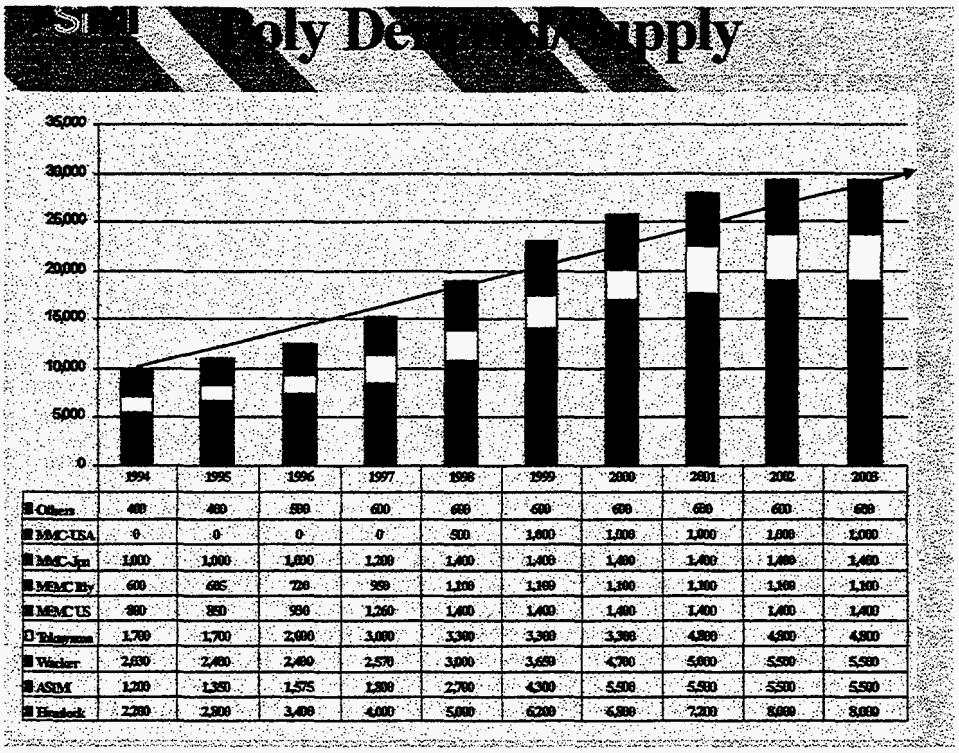
FIGURES



	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003
Others	400	400	500	600	600	600	600	600	600	600
MMC-USA	0	0	0	0	500	1,000	1,000	1,000	1,000	1,000
MMC-Jpn	1,000	1,000	1,000	1,200	1,400	1,400	1,400	1,400	1,400	1,400
MEMC Ity	600	685	720	959	1,109	1,169	1,300	1,300	1,300	1,300
MEMC US	980	980	980	1,260	1,400	1,400	1,400	1,400	1,400	1,400
Tokuyama	1,700	1,700	2,000	3,000	3,300	3,300	3,300	4,800	4,800	4,800
Wacker	2,600	2,400	2,400	2,570	3,000	3,650	4,700	5,000	5,500	5,500
ASiM	1,200	1,350	1,575	1,800	2,700	4,300	5,500	5,500	5,500	5,500
Hemlock	2,200	2,800	3,400	4,000	5,000	6200	6,800	7,200	8,000	8,000

Figure 1. Forecasted Demand (arrow) and Forecasted Supply (bars) for Semiconductor Grade Polysilicon in Metric Tons by Year

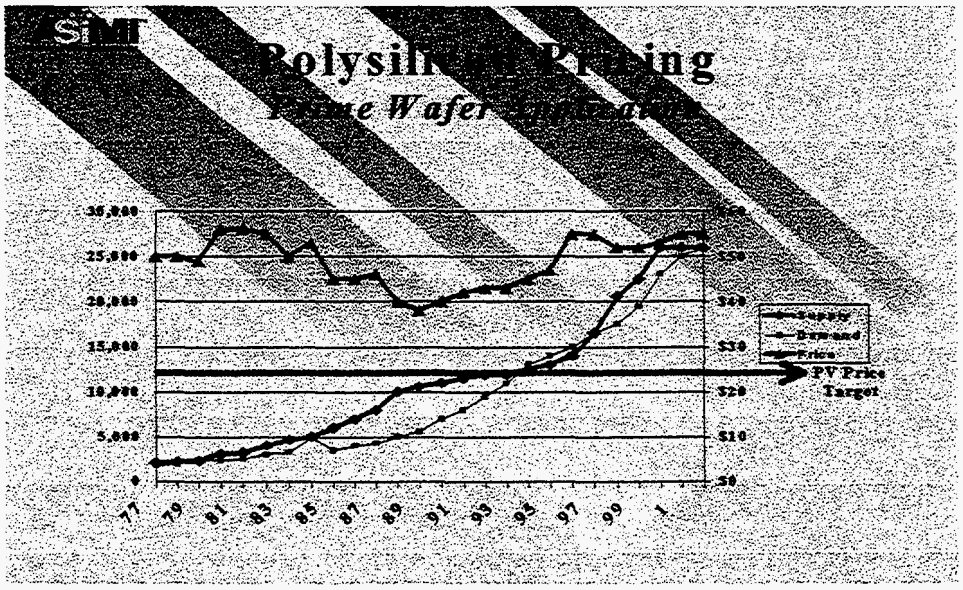


Figure 2. Pricing for Semiconductor Grade Polysilicon as a Function of Supply and Demand by Year

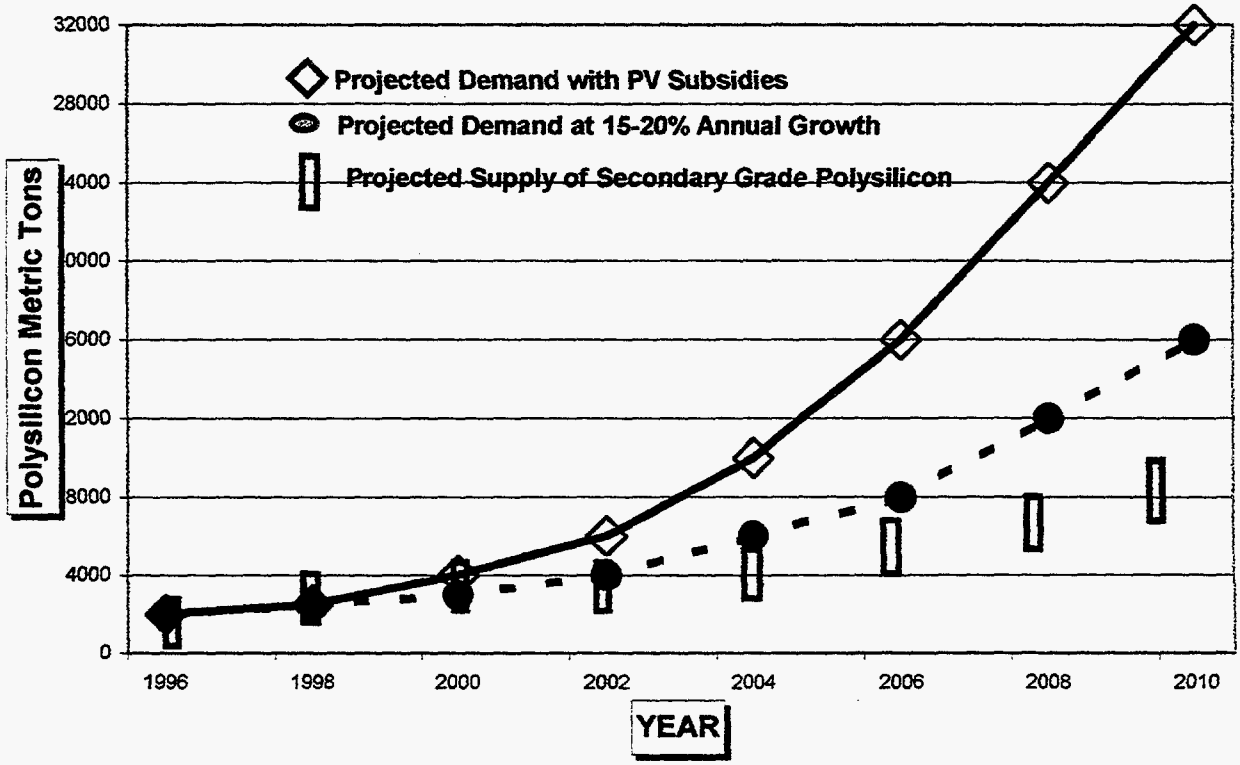


Figure 3. Forecasted PV Feedstock Demand and Secondary Polysilicon Supply in Metric Tons by Year

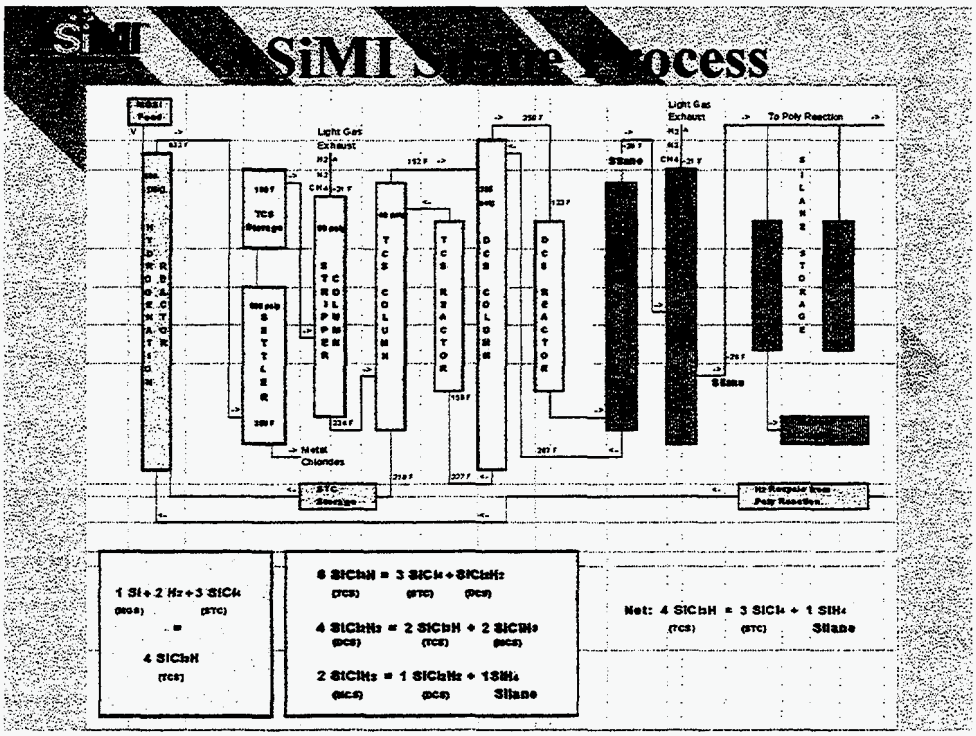


Figure 4. Flow Schematic of Advanced Silicon Materials Silane Production Process

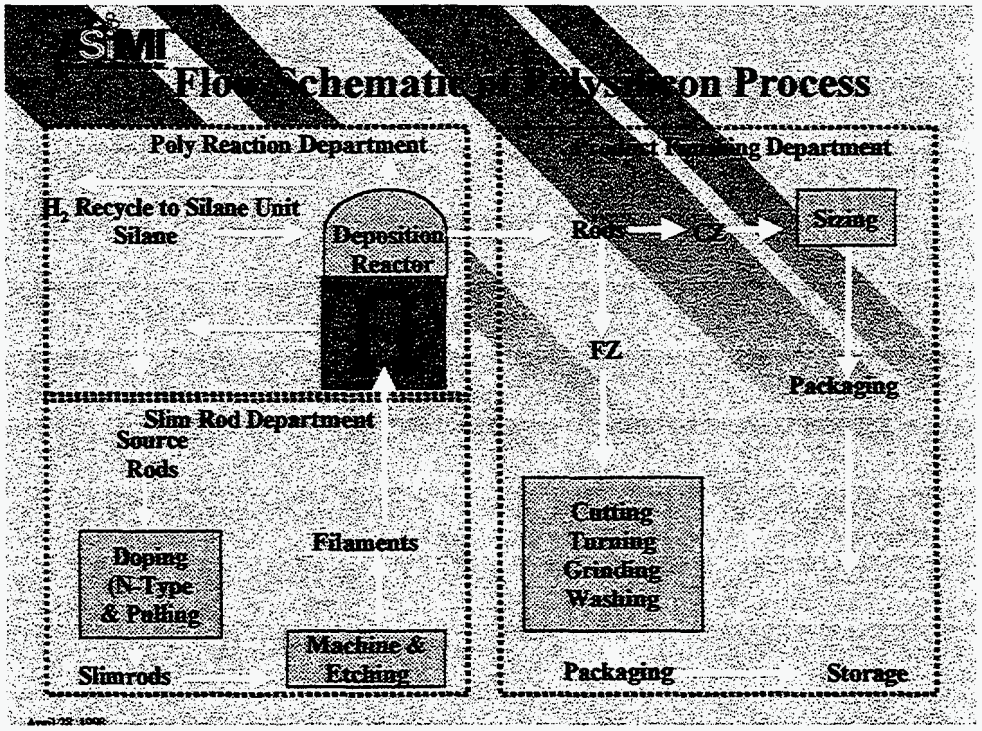


Figure 5. Flow Schematic of Advanced Silicon Materials Polysilicon Production Process

POLYSILICON PRODUCTION IN THE COMMONWEALTH OF INDEPENDENT STATES

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ABSTRACT

The main polysilicon production facility of the former Soviet Union is in Ukraine. Most silicon crystal growth facilities in Russia need to depend on imported polysilicon feedstock material. Recently, the Initiative for Proliferation Prevention program and the International Science and Technology Center have funded several projects in the nuclear successor states of the former Soviet Union to develop new sources of semiconductor-grade and solar-grade polysilicon feedstock.

I. INTRODUCTION

The silicon photovoltaic (PV) industry has been relying on rejected materials from the integrated circuit (IC) industry for the feedstock material for crystal growth. These rejected materials, over 2,000 metric tons in 1997, amount to about 10% of the semiconductor-grade polysilicon used by the IC industry. This arrangement worked well until 1995 when a shortage of polysilicon feedstock began to drive up the cost and limit the growth of the silicon PV industry. If the PV industry continues to grow at the present rate, which in recent years has been higher than the growth rate of the IC industry, and if crystalline silicon continues to be the dominant technology of the PV industry, then we must develop new sources of solar-grade polysilicon. An obvious solution is to build new factories dedicated to the production of low-cost (< US$10/kg), solar-grade polysilicon. The purity requirements for solar-grade polysilicon, according to the Solar-Grade Silicon Stakeholders Group, are the following: it is preferred that polysilicon have either B or P doping, with no compensation; resistivity at 25°C should be greater than 1 ohm-cm; oxygen and carbon should not exceed the saturation limits in the melt; and the total non-dopant impurity concentration should be less than 1 ppma [1].

Most of semiconductor-grade polysilicon is produced by the trichlorosilane ($SiHCl_3$) distillation and reduction method [2,3]. The trichlorosilane is manufactured by fluidizing a bed of fine pulverized metallurgical-grade silicon (MG-Si), which is more than 98% silicon, with hydrogen chloride in the presence of a copper-containing catalyst. The MG-Si, which costs about US$1.5/kg, is produced by the reduction of natural quartzite (silica) with coke (carbon) in an electric arc furnace. This method of polysilicon production is very energy intensive [4], and it produces large amounts of wastes, including a mix of environmentally damaging chlorinated compounds. About 80% of the initial metallurgical-grade silicon material are wasted during the process. In addition, the semiconductor-grade polysilicon material produced by this method far exceeds the purity requirement of the PV industry, and the cost (over US$50/kg, with most of it attributable to the $SiHCl_3$ processes) is several times higher than what the PV industry can afford [5]. Every watt of crystalline silicon PV module generating capacity requires roughly 20 g of polysilicon. Thus, if the cost of solar-grade polysilicon is US$20/kg, the cost of polysilicon per watt of a crystalline-silicon PV module is US$0.40. It is obvious that less complicated, less energy intensive, more efficient, and more environmentally benign methods need to be developed to meet the cost and quality requirements of the PV industry. New methods of producing solar-grade polysilicon should either be chlorine free or recycle chlorine internally to reduce cost and avoid damage to the environment.

Recently, the Initiative for Proliferation Prevention (IPP) program and the International Science and Technology Center (ISTC) have funded several projects in the nuclear successor states of the former Soviet Union to develop new sources of semiconductor-grade and solar-grade polysilicon. The IPP program is a U.S. Department of Energy (DOE) nuclear threat reduction effort. It strives to stabilize institutes, personnel, technology, and materials formerly dedicated to developing and manufacturing weapons of mass destruction in the nuclear successor states of the former Soviet Union – Russia, Ukraine, Belarus, and Kazakstan. The program addresses proliferation risks through Laboratory-to-Laboratory cooperative research and development projects in the former Soviet Union and projects with commercialization potential involving United States industrial partners [6]. The ISTC in Moscow, Russia was established by multilateral agreements as nonproliferation programs with the primary objective of providing peaceful non-weapons opportunities to weapons scientists and engineers in the Newly Independent States, particularly those with knowledge and skills in weapons of mass destruction and their delivery systems [Web site: http://www.istc.ru].

II. LOW-TEMPERATURE, CHLORINE-FREE PROCESSES FOR POLYSILICON FEEDSTOCK PRODUCTION

The National Renewable Energy Laboratory (NREL) and Sandia National Laboratories (SNL), with funding from the IPP program, has initiated a joint research program with the Intersolarcenter to study new chlorine-free methods of producing solar-grade polysilicon. So far, the most promising method developed by this project is one that uses MG-Si and absolute alcohol as the starting materials. This new process requires only 15 to 30 kWh of energy per kg of polysilicon produced vs. about 250 kWh/kg of the

trichlorosilane method. The silicon yield (polysilicon and the main by-product, silica sol) is in the 80% to 95% range vs. 6% to 20% for the trichlorosilane method. The eventual cost goal is US$10 per kg of solar-grade polysilicon.

The basic processing stages of this chlorine-free polysilicon production process are the following:

1. The reaction of metallurgical-grade silicon with alcohol proceeds at 280°C in the presence of a catalyst:

$$Si + 3\,C_2H_5OH \xrightarrow{catalyst} Si(OC_2H_5)_3H + H_2. \quad (1)$$

2. The disproportion (i.e., simultaneous oxidation and reduction) of triethoxysilane in the presence of a catalyst will lead to the production of silane and tetraethoxysilane:

$$4\,Si(OC_2H_5)_3H \xrightarrow{catalyst} SiH_4 + 3\,Si(OC_2H_5)_4. \quad (2)$$

3. Dry ethanol and such secondary products as high-purity SiO_2 or silica sol can be extracted by hydrolysis of tetraethoxysilane. The alcohol will be returned to Stage 1.

$$Si(OC_2H_5)_4 + 2\,H_2O \text{ ----- } SiO_2 + 4\,C_2H_5OH. \quad (3)$$

4. Silane is decomposed pyrolytically to pure silicon and hydrogen at a temperature of about 900°C:

$$SiH_4 \xrightarrow{850°\text{-}900°C} Si + 2\,H_2. \quad (4)$$

The purity requirements for solar-grade silicon are not as high as those for electronic applications. Thus, the silane will undergo a simplified cycle of purification, and at Stage 4 the less expensive and less energy-consuming process of a fluidized bed reactor can be used, instead of the well-known Siemens Process [2].

III. THE SILICON-OF-SIBERIA PROJECT

The Silicon-of-Siberia project is an IPP project with SNL being the technical coordinator for financing and the Mining & Metals Combine (MCC) of Krasnoyarsk, Russia being the operator of the proposed plant. Thomas Maletta of Dolphin Consulting is the project manager. The objective is to construct a 1,000 metric tons per year *semiconductor-grade* polysilicon factory in Siberia using a conventional trichlorosilane process at an estimated cost of $200M. The proposed plant design will consist of four 250-MT modules. The first module with a capacity for 250-MT of polysilicon and 20,000 MT of trichlorosilane is estimated to cost $90M.

IV. SOLAR-GRADE POLYSILICON PRODUCTION BY A PLASMA DECOMPOSITION METHOD

Kompozit Corp., Moscow has a two-year ISTC project starting May 1997 to develop a polysilicon deposition method that combines physical evaporation and plasma decomposition. The starting material for the evaporation process is high-purity quartzite from Siberia. The estimated eventual cost of solar-grade polysilicon produced is US$10/kg.

V. LOW-COST POLYSILICON PRODUCTION BY RECYCLING OF INDUSTRIAL WASTE

The Institute of Physics and Technology, Almaty, Kazakstan received funding in July 1998 from ISTC to study low-cost polysilicon production by recycling of industrial waste. Two of the co-authors of this paper, J.M. Gee and Y.S. Tsuo, are technical advisors of this project.

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STRING RIBBON—A NEW SILICON SHEET GROWTH METHOD

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ABSTRACT: String Ribbon, a method for continuous growth of silicon sheet, is described. Production furnaces are run continuously, 24 hours a day, and produce 5.6 cm wide ribbon of 300 μm thickness. A major R&D program is underway to ultimately grow ribbon at 10 cm width and at 100 μm thickness. The technical challenge of managing the thermal environment to minimize stress has been addressed using finite element modeling iterated with afterheater designs. Results on the production material and progress towards the R&D goal are reported.
Keywords: Ribbons – 1: c-Si – 2: manufacturing and processing -3

1. INTRODUCTION

A recent study by the European Commission [1] concluded that the most likely candidate to first achieve the goal of low cost solar cells at $1/watt was polycrystalline silicon and that ribbon could be significantly below that. Since 1994 Evergreen Solar has pursued the development of a silicon ribbon technology which is called String Ribbon and which should have an excellent chance of meeting this goal.

There are two common problems which all vertical ribbon technologies must overcome. One is edge stabilization and the other is minimization of the residual stress due to the high thermal gradients near the solid-liquid interface. Edge stabilization is addressed differently for each of the three currently practiced silicon ribbon technologies: EFG; dendritic web; and String Ribbon. For EFG, the edges are eliminated by growing a hollow polygon which is then laser cut into cell blanks. For dendritic web, dendrites are propagated along the ribbon edges under a supercooled melt condition. In String Ribbon, the subject of this paper, strings of a high temperature material are used and are incorporated into the grown ribbon.

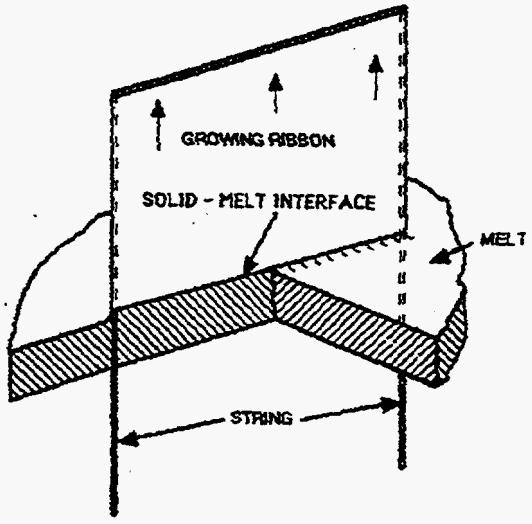

Figure 1 – String Ribbon growth process.

The thermal stress issue is challenging both from an experimental and a theoretical viewpoint. As will be seen below, considerable success in dealing with this challenge has already occurred. A combination of the basic robustness of the String Ribbon growth process and the use of finite element modeling iterated with afterheater designs has allowed Evergreen to commercialize the String Ribbon growth method and to make substantial headway towards the longer term goals of wider and thinner ribbon.

The incentive for the latter is two-fold. First, thinner and wider material can provide for as much as a three-fold increase in output per crystal growth machine. Secondly, 100 μm material reduces bulk diffusion length concerns since lifetime measurements indicate as grown diffusion lengths of about 100 μm.

2. GENERAL CONSIDERATIONS FOR STRING RIBBON GROWTH

The basic process [2] is illustrated in Figure 1. The strings are a non-conductive material which can be left in the ribbon as it is made into a solar cell. The ribbon is grown vertically and continuously from a shallow melt in a graphite crucible and crystallizes directly from the melt as a flat polycrystalline ribbon. Thus, complete segregation of impurities into the melt can readily occur. The possibility of either employing lower purity raw material and/or periodic dumping of the melt can be readily exploited in this silicon growth method.

2.1 Thermal Stress

The thermal stress problem is that, for any practical growth speeds the ribbon must endure, a thermal gradient of at least 500°/cm near the solid-liquid interface will ensue. Figure 2 shows a temperature vs. vertical distance profile. The stress is related to the second derivative, d^2T/dy^2. A lower d^2T/dy^2 gives lower stress. The second derivative can also be thought of as the curvature and the problem then is to minimize the curvature and to do this in the highest possible temperature region.

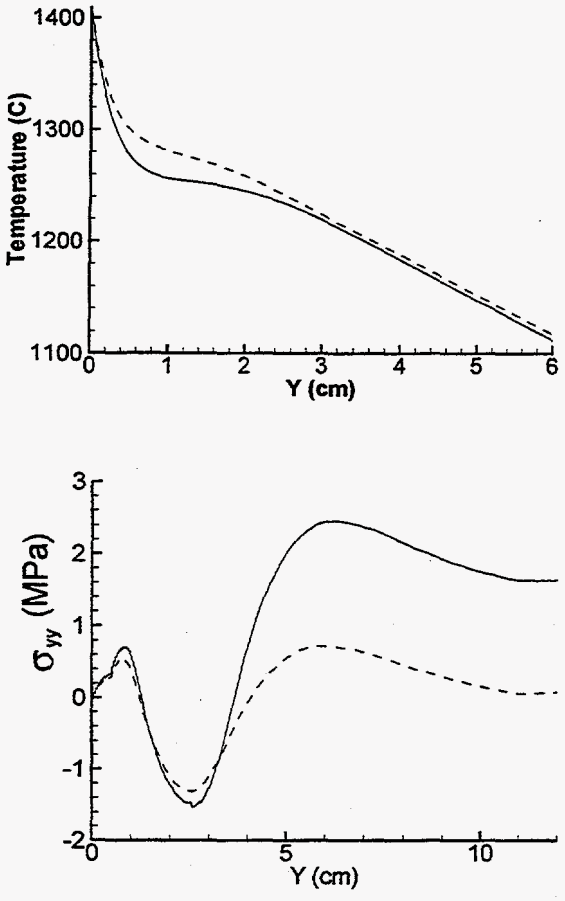

Figure 2- (top) Modeled cooling profiles, dashed line shows optimized afterheater design. (bottom) Dashed line shows lower final stress state predicted by thermo-plastic stress program.

The theoretical challenge is to model the thermal environment and from this predict an optimal cooling profile to minimize d^2T/dy^2. The two dimensional geometry of the String Ribbon process has allowed us to first explore 2-D finite element modeling and use this to iteratively design an afterheater which empirically will provide the desired modeled thermal profile. A 3-D thermal modeling effort has also been launched; this is much more involved to set up but ultimately will more closely resemble the actual situation and therefore be an even better predictor of a desired cooling profile.

In Figure 2 we also illustrated a modeled change in the thermal profile and the reduction in curvature which then ensues. Also, in conjunction with the thermal profile modeling, a thermo-plastic stress model [3,4] was used to predict the final stress state of the ribbon for various thermal profiles and indicated a very significant reduction in stress for the modeled change.

Practical manipulation of the cooling profile is done by using an afterheater. The afterheater is a structure that surrounds the ribbon as it cools after solidification; a passive afterheater simply redirects radiant heat from the crucible, an active afterheater incorporates a heat source.

The earliest application of this iterative approach provided us with a simple passive afterheater design which is now in use on our production machines. However, it soon became clear that for growth of 100 μm 10 cm ribbon, an active or tunable afterheater would be preferable

3. PRODUCTION RIBBON

The simplicity of the process has allowed Evergreen to launch into production with this material at 300 μm thickness and 5.6 cm width. Figure 3 shows some of the production crystal growth furnaces. Individual cells are 15 cm long (~ 84 cm^2). Evergreen Solar now manufactures a 30 W and a 60 W size module based on String Ribbon cells. The crystal growth machines are run continuously, 24 hours each day, seven days per week, with an in-house developed melt depth measurement coupled with automatic melt replenishment.

The production process is continually being upgraded from the point of view of automating it so that a single crystal growth operator can run a large number of the machines. The machines are easy to replicate and we have installed and started running a new machine within 48 hours of receiving it. String Ribbon is much less sensitive to variations in melt temperature compared to the other two silicon ribbon methods. An example of this is the fact that a new reel of string material can be installed without interrupting growth.

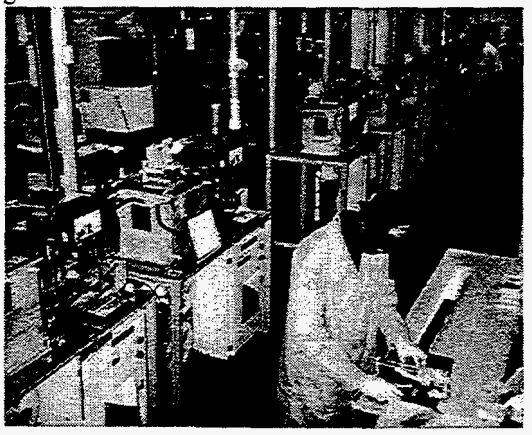

Figure 3 – Production crystal growth furnaces.

For production purposes, key indicators are yield and duty cycle. Duty cycle is the time that a machine is actually producing usable ribbon. Yield is the number of usable wafer blanks divided by the total ribbon grown. As already indicated, the production process is continuously being improved. At present, we have attained a duty cycle of almost 90% and silicon-to-wafer yields frequently exceed 90%. As a result of our automated melt height and continuous melt replenishment, thickness uniformity has improved significantly. Data for the past three months is shown in Figure 4.

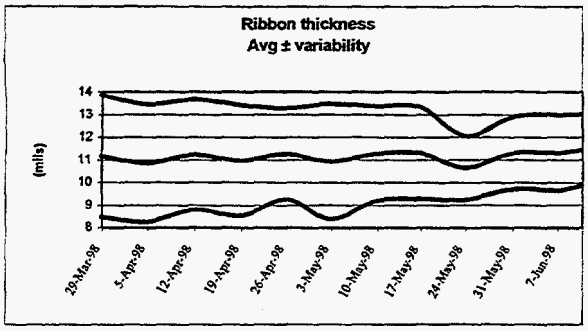

Figure 4 – Production thickness uniformity over the last 3 months.

4. R&D RIBBON PROGRAM

Initially, we have divided the R&D program into two parallel components—growth of wider ribbon (>5.6cm) and the growth of thinner ribbon of 80 – 100 μm thickness. Within the next twelve months we will unify them.

4.1. Wider Ribbon

As an initial thrust towards the growth of 10 cm ribbon, we have used a passive afterheater design suggested by the 2-D modeling work. For an intermediate goal, we chose 8 cm ribbon. The effort went quite well and we have now produced a sizeable quantity of 8 cm material, 300 μm thick. Figure 5 shows some 4 ft. long strips of this material. In the near future, we will investigate the possibility of switching our cell line to 8 cm x 15 cm cells (120 cm^2 in area).

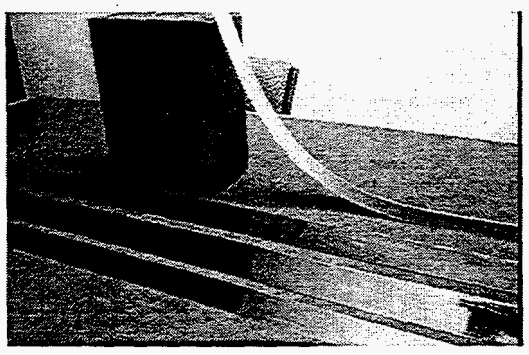

Figure 5 - (fore) lengths of 8 cm wide ribbon
(back) flexed length of 125 μm thick ribbon

4.2 Thinner Ribbon

Evergreen is aggressively pursuing the goal of eventually producing 10 cm wide ribbon at 100 μm thickness. A design for an active afterheater, based again on the 2-D thermal modeling work, has been made and is being built at the time of this writing. Initially, we will grow 80-100 μm ribbon of 5.6 cm width and then, finally, 10 cm width.

As an intermediate step, we have used an advanced prototype passive afterheater to grow material of about 125 μm thickness. This was done to test the limits of passive afterheaters and to produce some material quickly for R&D cell purposes. Further, it was important to obtain some sense of the handling issues with silicon this thin. As can be seen in Figure 6, the material is flat, but not as flat as for the 8 cm wide ribbon of 300 μm thickness. Figure 6 qualitatively compares the flatness of the three types of ribbon we have grown so far, 300 μm, 5.6 cm wide production material, 300 μm, 8 cm wide ribbon, and 125 μm, 5.6 cm wide. Reflections of the striped background show that the 8 cm and 5.6 cm wide ribbon are quite flat at 300 μm; while the 125 μm thick 5.6 cm wide ribbon is less flat. Figure 5 demonstrates the flexibility of the 125 μm thick ribbon.

Silicon at thicknesses of about 100 μm is quite flexible but it is still silicon—basically a brittle material. The ability to successfully handle and process thin ribbon such as this will depend on two factors. First and foremost, the ribbon will need to be flat. Secondly, the cell processing should entail minimal handling and mechanically benign processing steps. The stress issue is being addressed with the active afterheater described already. For the other concern, Evergreen's cell line has been deliberately designed to be very gentle mechanically and to require very few steps and very little handling. Preliminary experiments with the 125 μm material scribed into our standard size blanks of 5.6 cm x 15 cm run through our processing line indicate that this is a very tractable problem.

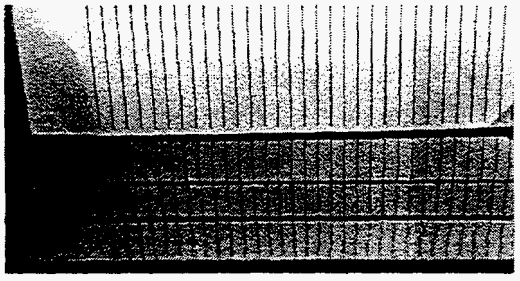

Figure 6 – Comparison of flatness of 300 μm thick 8 and 5.6 cm wide ribbon (back) and 125 μm thick 5.6 cm wide ribbon (fore).

4.3 Solar Cell Results on R&D String Ribbon

In conjunction with Professor Rohatgi's group at Georgia Tech, to date the best cell made on the 125 μm ribbon has been 15.4% using laboratory type processing. Other relevant observations are that the material shows, like many polycrystalline silicon materials, sensitivity with thermal processing such that the final lifetime can be very much higher than the starting lifetime.

5. SUMMARY

String Ribbon is now being actively pursued in production and in a research mode. Production material is 5.6 cm wide and 300 μm thick. Yields, duty cycle, and ribbon thickness control all have attained values which indicate further commercialization and expansion of this silicon ribbon technology. Research results using thermal modeling combined with iterative designs for afterheaters, both passive and active, has been very fruitful and has produced very promising results to date. Prospects for eventually growing 10 cm wide, 100 μm ribbon seem excellent.

6. ACKNOWLEDGEMENTS

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Status of EBARA Solar, Inc.

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During the past year, efforts at EBARA Solar have focused on overcoming the remaining obstacles which limit the production of single crystal dendritic web silicon ribbon. The heating method has been changed from induction heating, using a single induction coil, to resistance heating with four independent zones. Seven web furnaces are currently operating with resistance heating. With this transition, moving parts for temperature control (e.g., radiation shields and induction coil) were eliminated and flexibility in the delivery of heat to the melt was enhanced. This led to increased reproducibility in the growth process, and opened the way for hardware modifications which increased the stability of the process itself. It is now common to grow dendritic web silicon crystals, having a nominal thickness of 100 μm, at steady state widths up to 6 cm at a corresponding area rate of 10 cm^2/min. Crystals have been grown up to 37 m in length, while requiring only 440 g of silicon. During the growth of long crystals, the melt level remains constant because silicon pellets are delivered to the melt at a rate which matches the crystal growth rate (100% feeding).

Control systems leading to nearly untended growth have also been developed. These perform functions such as adjusting the temperature of the melt to the freezing point of silicon ("hold"), controlling the undercooling of the melt in order to initiate growth from the dendrite seed ("wingout"), sensing the extent of the linear wingout and executing the crystal pulling sequence upon reaching the desired size ("button"), controlling the melt temperature based on measured dendrite thickness for sustained, steady-state growth, and measuring the melt level continuously during growth. With crystal terminations associated with thermal and feeding conditions largely under control, additional work is directed toward reducing the incidence of terminations by loss of single crystal structure ("poly"). Such poly terminations are thought to be caused largely by thermal stress and the bending of the thin web crystals, and are currently being investigated in collaboration with NREL. The web growth process also requires a very clean melt, free from particles which can nucleate the growth of unwanted silicon "ice" in the undercooled melt. A key problem in this regard is the accumulation of silicon oxide particles on the growth hardware, where the source of oxygen is the dissolving quartz crucible. A method for removing oxide-laden vapor from immediately above the melt and collecting it in a controlled fashion has been demonstrated but not yet implemented.

Although cell fabrication has not been a major activity during the past year, some web cells (2.5 cm × 10.0 cm) have been made recently, primarily to evaluate the quality

of web crystals grown in the resistance furnaces. Starting web substrates are antimony-doped to 20 Ω-cm. Processes include: wet chemical cleaning of the web crystal sections to remove the deposited growth oxide, applying and oven-drying liquid phosphorus and liquid boron dopants to opposite sides, diffusing phosphorus and boron simultaneously in an RTP unit, stripping the diffusion glasses, measuring sheet resistance, cutting cell-sized pieces from the crystal sections using diamond scribing, screen printing the front aluminum contacts, alloying the aluminum with silicon in a belt furnace, screen printing and drying silver soldering pads on the aluminum bus bars, screen printing the back silver contacts, and firing the silver pads and contacts in the belt furnace. Because these cells are made for material quality evaluation, no antireflective (AR) coating is applied. Such cells have demonstrated the capability of achieving 15% efficiency, confirming the quality of web grown in the resistance furnaces. In earlier pilot-scale operations, mechanical yields in excess of 90% have been achieved with these processes, in spite of the fact that dendritic web substrates are only 100 μm thick and that handling of crystal sections and cell blanks is done manually at this time.

Dendritic web cell efficiencies up to 17.3% have been realized on lightly-doped n-type substrates. Bifacial cells with back-illuminated efficiencies nearly equal to front-illuminated efficiencies have also been made in the past. Other cell structures are currently being investigated in collaboration with the University Center of Excellence for Photovoltaics at Georgia Tech, in an attempt to exploit the thin, single crystal nature of dendritic web. In particular, the aluminum alloy p-n junction is being evaluated as a back junction for use in an interdigitated back contact (IBC) cell, shown in Figure 1. In such a cell, both positive and negative contacts are on the unilluminated side, thereby reducing shadowing losses to zero and allowing the treatment of the front surface to be dictated by concerns for passivation alone.

As a precursor to the IBC cell, a structure was fabricated by screen-printing aluminum and silver on the back and front, respectively, of n-type (20 Ω-cm) dendritic web silicon substrates. This simplified structure is shown in Figure 2. Aluminum was alloyed in an RTP unit in the presence of oxygen for additional surface passivation, while silver was fired in a radiantly-heated belt furnace. Cells up to 13.2% (4 cm^2 area) were produced (J_{sc} of 31.3 mA/cm^2, V_{oc} of 599 mV, FF of 0.706), indicating the aluminum alloy p-n junction is suitable for solar cells if placed at the back. Internal quantum efficiency was quite good, as shown in Figure 3, suggesting a base lifetime in excess of 75 μs. Contacts which are self-doping and self-aligning, such as Ag-Sb of Figure 1, are also being developed for application to both conventional and IBC web cells.

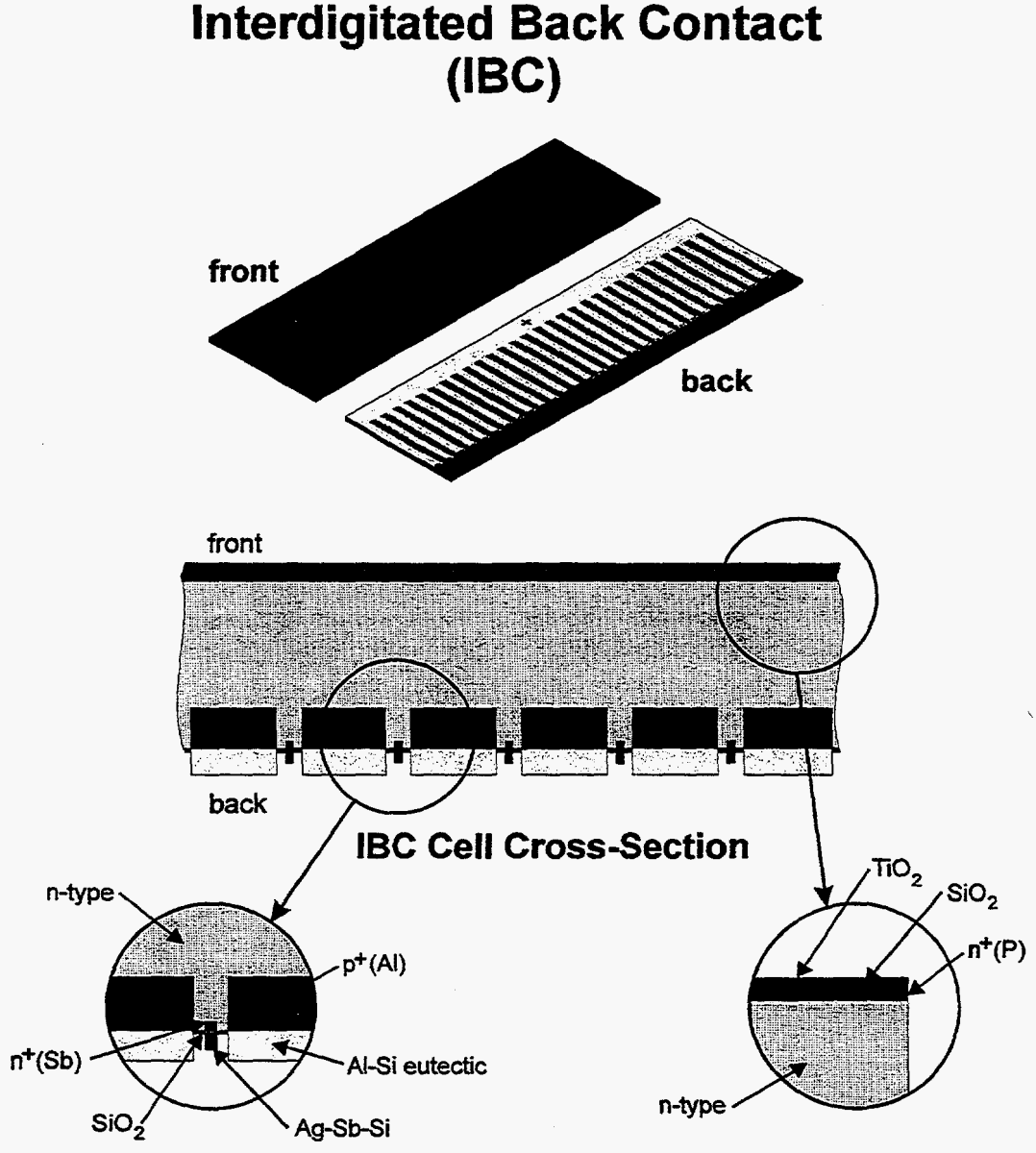

Figure 1. Target IBC cell structure with Al alloy p-n junction and self-doping Ag-Sb negative contact.

Screen-Printed Cell with Aluminum Alloy Back p-n Junction (Precursor to IBC)

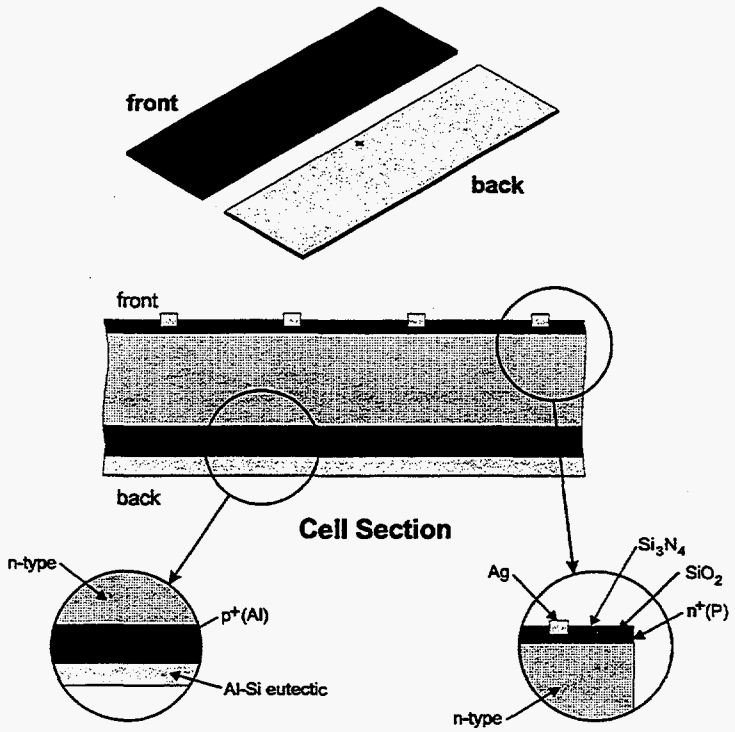

Figure 2. Intermediate cell structure to evaluate quality of Al alloy p-n junction on back.

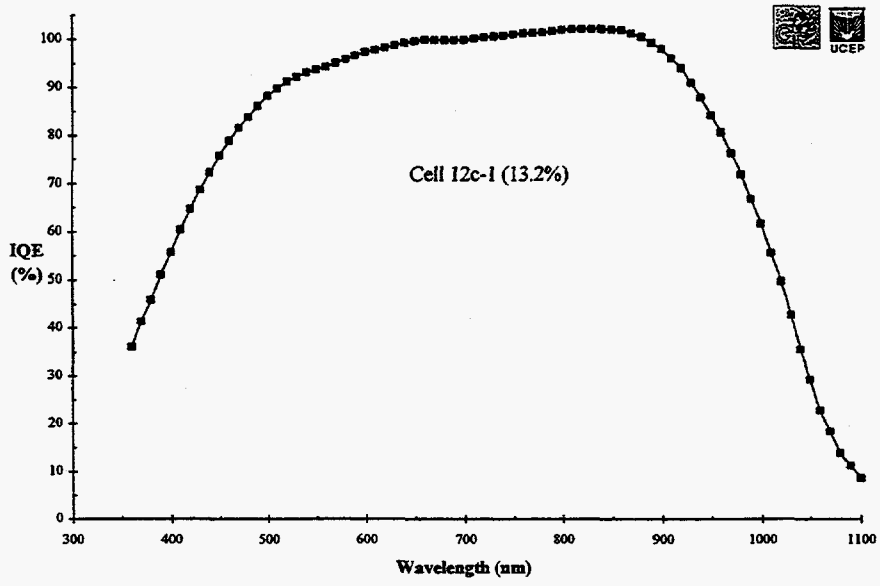

Figure 3. IQE for Screen-Printed Dendritic Web Cell with Back Aluminum Alloy Junction

Status and Issues of Crystalline Silicon Solar Materials and Devices in Japanese PV Market

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ABSRACT: Japanese activities for crystalline Si solar materials and devices have been directed to the promotion of Si feedstocks R&D using Kawasaki process and to discussion of about future directions for bulk Si devices. The quality of the Kawasaki cast crystals has greatly improved by a joint work between Japanese companies. 14%-level efficiency cells have been fabricated using good-quality cast wafers and conventional cell fabrication processes. Last year, the Japanese government subsidy program for PV houses has contributed to sell more than 8,000 systems. However, the module price tends to be saturated and is difficult to decrease furthermore. Future cost reduction will be realized by creating new module designs including building integration, static-concentrator and light-trapping structure.

1. INTRODUCTION

In recent years, crystalline silicon solar modules using bulk Si materials have become dominated more and more in photovoltaic market and played a major role for both remote and grid-connected power applications[1]. Especially, last years' market growth was remarkable by showing 43% increase in the world. However, the market growth in the coming next century might be suppressed if production technologies on low-cost silicon feedstocks, high-speed slicing and high-efficiency, low-cost solar cells and modules were not developed.

In 1993, Japanese government had decided to restructure the past Sunshine Program by taking account of an environmental issue and to restart the New Sunshine Program. In 1994, an aggressive subsidy program for private houses and public buildings was implemented by Ministry of International Trade and Industry to promote PV market exploitation[2]. In this year, more than 10,000 PV systems are expected to be installed on the roofs of private and public houses using the subsidy program.

As for R&D in the past project, steady progress had been made especially in the fundamental research and the development of new process technologies for Si feedstocks and solar devices[3]. Especially, the past 4-year government R&D project from 1992 to 1996 for crystalline Si materials and devices was successful. Primary results were the developments of equipment and technologies to produce gigantic cast ingots and also fast cell fabrication processing technologies for multicrystalline Si solar cells. 17%-efficient, large-area multicrystalline Si solar cells were fabricated with 15%-level efficient, modules fabricated using multicrystalline Si solar cells. In addition, very-high efficiency, single-crystal solar cells with a 22%-level were fabricated.

This paper describes the technological status of the Si feedstock program which has been promoted by a new association, SOGA, established in 1996. Another issues emerged are the saturation of price reduction and the cost gap between current module price and government cost forecast. Further cost reduction will be realized by developing automated mass-production technologies from Si feedstocks, wafers, cells to modules and creating new module designs including building integration, static-concentrator and light-trapping structure.

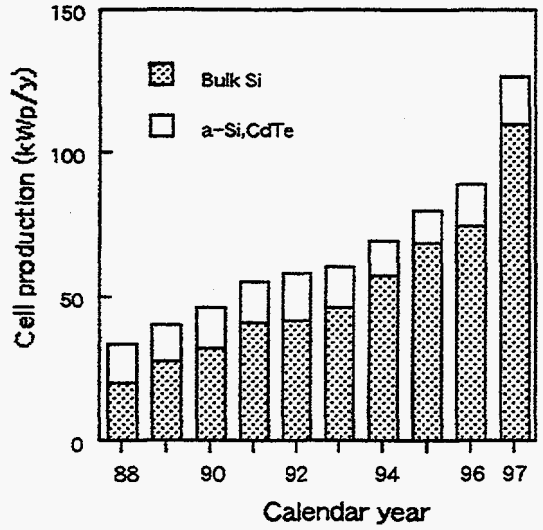

Fig. 1 Yearly production growth of bulk-Si and film-type solar cells.

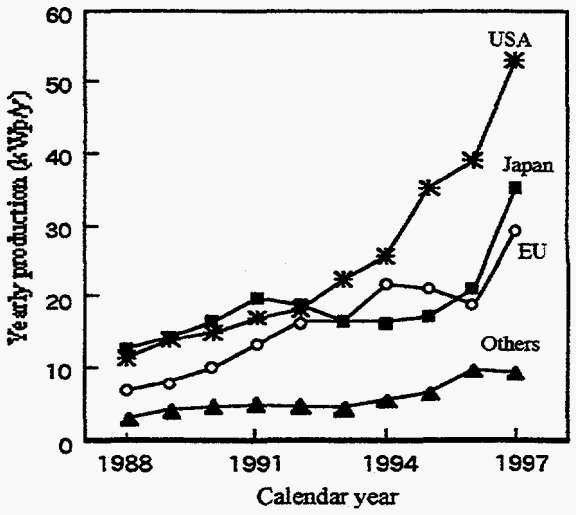

Fig. 2 Market competition between USA, EU, Japan and others from 1988 to 1997.

2. MARKET DEPLOYMENT

As already mentioned above, the recent market growth has been remarkable. Especially last year, a world-wide PV market expanded to 127 MWp, 43% increase as compared to 1996. The market size is about 4 times larger than that in 1988. As indicated in Fig. 1, the increase depends upon a great expansion of cell production using single and multicrystalline Si wafers. As the production of a-Si and CdTe, film-type solar cells has been almost constant in the past ten years, crystalline silicon solar cells and modules using bulk Si materials will become dominated more and more in a future photovoltaic market for both remote and grid-connected power applications.

The rapid growth of cell production occurred both in USA., EU and Japan, as shown in Fig. 2. In 1988, about ten years ago, production shares of USA and Japan were almost the same. However, Japanese share declined from 1991 because of economical depression and lower yen price, whereas productions in USA and EU grew steadily. Since 1994, Japanese production tended to recover from the depression and to increase rapidly. Last year, 65% increase was attained as compared with the previous year in Japan. This remarkable increase is mainly due to the initiation of government subsidy program for private PV houses. As indicated in Fig. 3, the number of PV houses in 1997 surpassed 8,000 corresponding to 30 MWp and is expected to be more than 10,000 due to the fixed budget increment in FY 1998.

However, PV system price did not decrease expectedly. As shown in Fig. 3, the total price of a 3 KWp system in 1994 was 6 million yen (40 k$ using an exchange rate of 140 yen/$) and users had to pay 2 million yen due to the 2 thirds subsidy. In 1997, the total price of the 3 KWp system was 3.4 million yens and the users had to pay almost

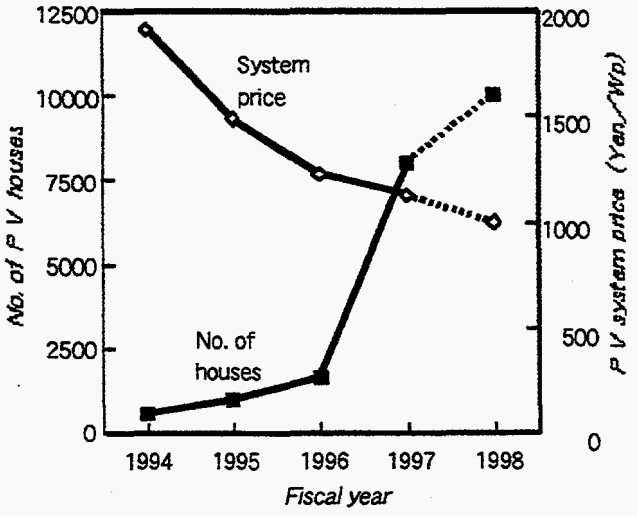

Fig. 3 Yearly variation of number and system prices of PV houses under government support.

the same 2 million yens as the subsidy went down one third. The current price of 1,130 yen (8.1 $) / Wp is consisting of 690 yen (5$) /Wp for modules, 315 yen (2.3$) /Wp for balance of systems and 120 yen (0.9 $) /Wp for installation. Further price reduction is considered to be difficult by the conventional, highly-reliable superstrate module design.

3. R&D STATUS

(1) Silicon Feedstocks

In the past until 1992, a low-cost process of silicon feedstock by carbothermic reduction of high-purity silica had been investigated. However, the process was not selected for a recent urgent need of Si feedstocks and cast ingots. Instead, refining of metallurgical-grade Si materials has been conducted. In the Kawasaki process in Fig. 4, phosphorus impurity was firstly removed from metallurgical-grade Si feedstocks by evacuation and then boron impurity using a plasma oxidation. Boron content could be reduced by mixing water vapor in an argon plasma to a 0.1 ppm level. Metallic impurities were reduced to a ppb level by twice resolidification of the refined MG-Si. Table 1 shows recent results of cell efficiencies using cast wafers fabricated from the Kawasaki SOG-Si feedstocks[5]. Cell efficiencies of around 14% were obtained by a conventional cell fabrication process which is almost the same level in the use of a semiconductor-grade Si feedstock. This year, a pilot-scale setup with a capacity of 100 kg will be constructed by the government support.

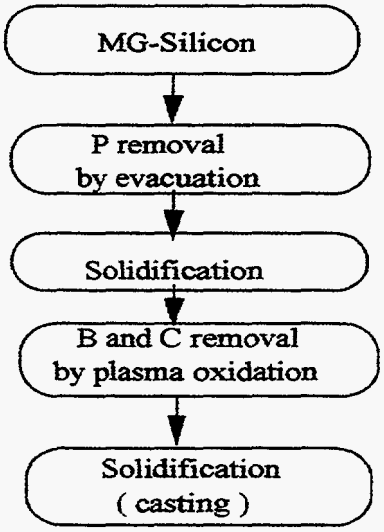

Fig.4 Production flow of Si feedstocks refined from metallurgical-grade silicon source[5].

Table 1 Quality of Kawasaki SOG-Si materials and cell efficiencies using cast wafers from the SOG-Si

SOG-cast	Mean lifetime (μs)	Mean cell efficiency (%)	
		Process A	Process B
KS-971	1.8	11.4	12.4
KS-972	3.1	12.5	13.3
KS-981	10~12	12.5	14.5
KS-98E *	20~30	13.4	14.2

* Cast wafers using semiconductor-grade source

(2) Casting and wafering processes

In the past from FY 1985 to 1996, quality improvement of conventional, electromagnetic and drip-controlled cast ingots had been conducted persistently by investigating the effects of solidification conditions on the crystal quality and also on the cell characteristics. Especially, a cold-crucible casting process with a magnetic field was selected owing to its inherently inexpensive nature. The temperature gradient during ingot solidification was found to affect the ingot quality substantially. Cell efficiency using the electromagnetic casting (EMC) ingot was a little smaller than that using conventionally cast substrates. However, cell efficiency of about 16% was reported to obtain by annihilation of active defects through hydrogen passivation. In 1992, 25 cm square ingot was firstly fabricated by the EMC technology and an ingot with 1.6 m in length was grown. In 1996, a production-level EMC furnace was constructed to grow a record 500 kg ingot with 35 cm square and 2.2 m in length at a solidification

rate of 2.0 mm/min. Another casting process had been proposed by dripping molten Si on crystallized ingot, so-called drip-controlled method (DCM). The DCM process was applied to develop a continuous production technology of a 170 kg ingot with a size of 43 cm square and 40 cm in height. Using 26 DCM cast substrates, an average cell efficiency of 16.6% and a maximum efficiency of 17.1% were realized for 225 cm^2 area substrates.

Currently, the EMC process requires the development of continuous and automated production technologies including initial heating-up of a molten zone and in-situ cutting of the ingot. The former is discussed on the use of plasma torch and the latter is the application feasibility of a laser cutting to get a smaller ingot for slicing and something like that. Another issue is to develop a fast slicing and smaller kerf loss by a sophisticated multiwire saw technology. The technology target of the fast slicing technologies is to achieve 115,000 slices/month/setup with 250-μm thick, 15-cm square wafers from smaller 40cm-square ingots. Another challenge is to develop technologies of a simultaneous slicing of 4 ingots for cost reduction. This year, another issues will be taken into account ranging from separation, cleaning, investigation and packing of many sliced wafers.

4. PRICE ANALYSIS AND COST FORECAST OF SOLAR MODULES

As already mentioned in Fig. 3, one of the current issues is the saturation of module prices although production quantity expanded rapidly due to the government subsidy policy for PV houses. The current price is consisting of module, balance of system (BOS) and installation. The BOS includes inverters, circuits, connections, wiring and etc. As indicated in Fig. 5, the prices of the three components for the small PV systems tended to decrease year by year by a government guidance. To compare the three components in more detail, the percentage of the three components were calculated. As shown in Fig. 6, the price percentage of the solar modules tended to increase, while the percent of the BOS tended to decrease and the installation almost kept constant.

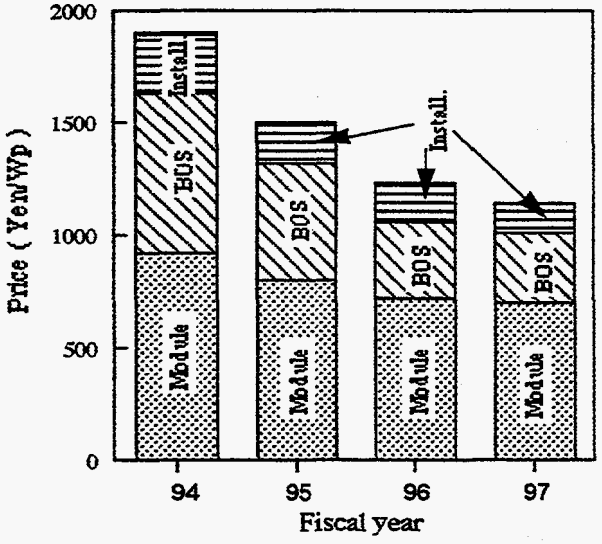

Fig. 5 Yearly variation of PV system price from 1994 to 1997.

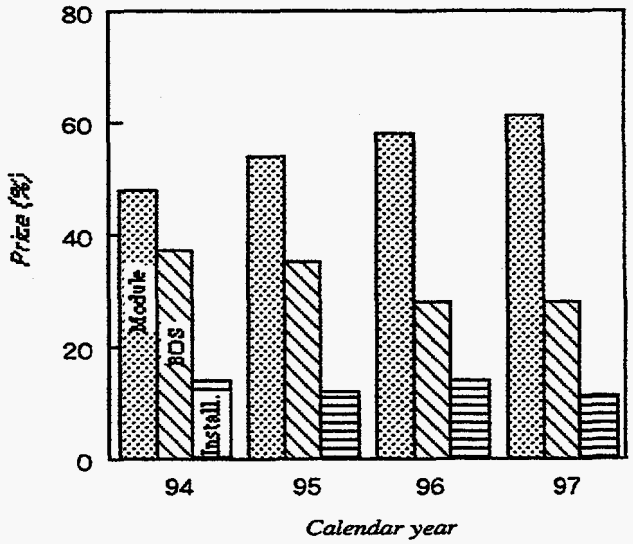

Fig. 6 Price allocation of module, balance of system and installation

As expected, cost reduction of solar modules is key factor for future cost reduction of the PV systems. Fig. 7 shows yearly reduction of the government module price, so-called NEDO price, and also government cost forecast under an assumed production of 100 MWp/year. The trend of the NEDO price is a saturated to be about 600 yen (4.3$)/Wp which is the same as the price trend of the small systems in Fig.3. One of the peculiar point in Fig. 7 is the big cost gap between the current price and

cost forecast of 200 yen/Wp. The allocation of the current prices is about 30% for the each components as indicated in Fig. 8. In the cost calculation, all the components would be reduced by automated, mass production of 100 MWp/y for cells and modules and 500 MWp/y for Si materials. Especially. the allocation of cell production was expected to reduce drastically.

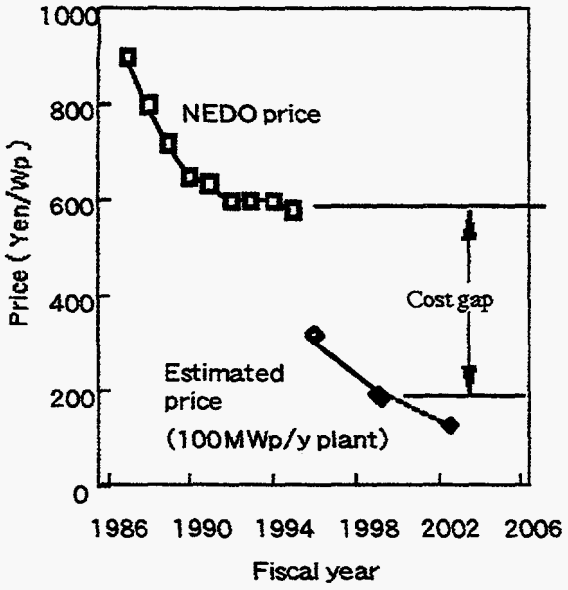

Fig. 7 Yearly reduction of NEDO price and estimated production cost.

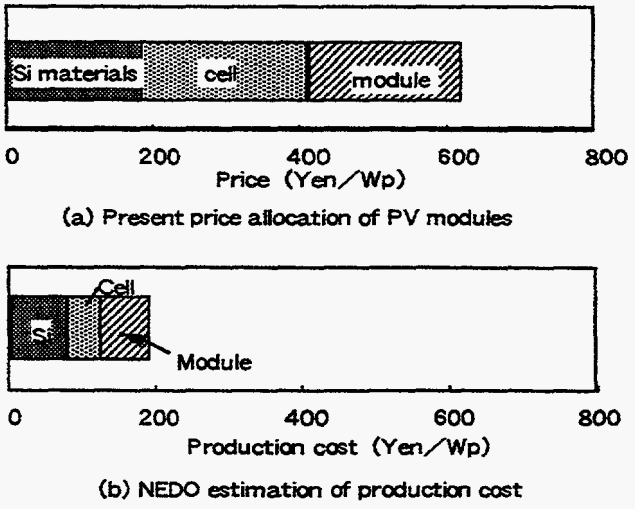

Fig. 8 Cost allocations of current module price and calculated NEDO production cost.

5. CONCLUSIONS

In the current government project, the feasibility of further cost reduction is pursued through various thin-film cell approaches. The government cost target is 140 yen (1 $) /Wp to meet the current price of electricity generated by a gigantic power plant. This is too ambitious and challenging. It is worried about that no one can reach the government target. The most important thing is not to achieve the ambitious cost target, but to create new ideas to reduce the module price to half or one third of the current price. Further cost reduction would be realized by promoting module-oriented research including building integration, static-concentrator and light-trapping structure in addition to automated, mass-production of Si materials , cell and modules.

ACKNOWLEDGMENTS

The author is obliged to Dr. F. Aratani, General Manager of SOG-Si Technology Research Association (SOGA), Mr. S. Wakamatsu, Director General of the Photovoltaic Power Generation Technology Research Association (PVTEC) and Mr. Konno, Director General of the Solar Energy Division of the New Energy and Industrial Technology Department Organization (NEDO) .

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BEHAVIOUR AND INFLUENCE OF DEFECTS IN "PHOTOVOLTAIC" SILICON WAFERS

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Silicon wafers used for photovoltaics could be divided in several classes according to the type of solar cells :

- cells for high concentration ($\approx$ 100 suns)
- cells for weak concentration (< 30 suns)
- cells for AM1.5 illumination
- thin film solar cells

Although the raw wafers are generally of high electrical quality, the processing steps needed to make solar cells induce or activate defects and impurities. However, defects or impurities could be present in the raw materials, especially in multicrystalline silicon. These defects can be electrically active, i.e. recombining for minority carriers in the raw materials, they can be also initially neutral and then activated by unavoidable thermal treatments (they could be called sleeping defects). In this paper, we try to show how these defects and the impurities can limit or degrade the minority carrier lifetime and so, the conversion efficiency in the different types of solar cells.

For concentration solar cells made with FZ silicon wafers, problems come from the high doping levels which induce first aggregation of boron or self-interstitials and then Auger recombinations for boron concentrations higher than 10^{17} cm^{-3}. These aggregates are weakly recombining in the raw material but they can trap impurities and once decorated, they become more active.

In Cz wafers, the main problem is due to oxygen, which the concentration is frequently in the 10^{18} cm^{-3} range. Even during the phosphorus diffusion, nucleation centers are created when the wafers are heated at temperatures higher than 700°C. These nucleation centers are converted in precipitates during annealings at temperatures closed to 900°C (those used to oxydized the wafer surfaces). These precipitates induce in turn dislocation networks which can trap impurities and degrade the lifetime. External gettering techniques like phosphorus diffusion or aluminium-silicon alloying are unable to restore the initial properties. Although the precipitates could be shrinked or dissolved by self-interstitial injection, the lifetime is not significantly increased because the dislocation networks cannot be removed and trap strongly impurities, i.e. an external gettering is developped. Even when the oxygen concentration is below the solubility limit, oxygen atoms can interact with boron, especially in highly doped p type wafers, and oxygen-boron pairs degrade the lifetime of minority carriers.

In multicrystalline wafers, it is well known that extended crystallographic defects and metallic impurities, which frequently interact, are the main source of recombination centers. The main defects are decorated dislocations and dislocation tangles. In conventionally casted materials, external gettering techniques could be applied successfully provided the interstitial oxygen concentration is lower than 6.10^{17} cm^{-3}. Such techniques give rise to better results than those obtained with hydrogen.

In electromagnetically casted wafers, there is generally a high density of extended defects and metallic impurities which are initially neutral at room temperature (they can be detected by LBIC scan maps at low temperature) but become active after any kind of annealing at temperature higher than 600°C. Consequently, electromagnetically casted wafers must be processed at the lowest temperatures and can be improved by hydrogenation only. Conversely, conventionally casted silicon wafers can be treated at high temperatures, i.e. they can be submitted to gettering treatments to be improved.

Thin film cells can be prepared using Liquid Phase Epitaxy (LPE) or CVD deposition techniques on solar grade silicon substrates, i.e. more or less pure multicrystalline silicon wafers. It was found that crystalline defects of the substrate are transfered to the layer. However, for LPE deposition, the layer is purer than the substrate and the diffusion length of minority carriers are higher in the layer, due to a gettering of metallic atoms by the liquid solvant.

Defects could also have some beneficial effects, especially when they are voluntary introduced and localized in the wafers. This is the case for backside dammages due to ion implantation, and particularly to He^+ implantation followed by annealings which create nanocavities. These cavities induces a segregation gettering of impurities which can improve the wafers.

Endly, it was recently shown that p-n junctions made with dislocation-containing wafers behaves as light emitting diodes (LED) in the infrared, thus the photovoltaic structure could be converted in infrared LED and optoelectronic devices.

FEEDSTOCK EVALUATION FOR CZOCHRALSKI GROWN SILICON SOLAR CELLS

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ABSTRACT: A key factor for profitable mass production of conventional mono-crystalline silicon cells is the continuous supply of electronically and economically acceptable feedstock materials. The material presently available on the market can be divided into three major categories: virgin poly, remelt and potscrap. In this work the electrical properties of ingots grown from these materials and their impact on the performance of solar cells are investigated. The materials significantly differ with respect to the response of the diffusion length to solar cell processing steps. Ingots from potscrap show the lowest diffusion length as well as the smallest improvement after solar processing steps. A significant contribution to the improvement of diffusion length after P-diffusion can be attributed to the annihilation of thermal donors which decrease the diffusion length and partially compensate the as-grown material. The correlation between diffusion length L and short circuit current of solar cells processed from these materials is better when L is measured after P-diffusion and oxidation than in the as grown state.

1. INTRODUCTION

Conventional mono-crystalline silicon cell technology still contributes to about 55% to the annual output of the world's photovoltaic industry (1997: 110MW). The continuous supply of electronically and economically acceptable feedstock materials for the crystal growth is a key factor for profitable mass production. From the presently available three categories of materials, i.e. virgin poly, remelt and potscrap, the latter two are waste products of the silicon electronics industry: remelt comes from tops and tails and rejected ingots whereas potscrap is the residual melt frozen in the quartz crucibles. In this work the electrical properties of ingots grown from these starting materials and their impact on the performance of solar cells are investigated

2. MATERIALS AND PROCESSES

Test ingots (136mm diameter) were grown in production line Czochralski (Cz) crystal growers from defined feedstocks based on typical charges of these different materials. By using the identical digital crystal grower and growth parameters special care was taken to achieve comparable crystal quality. Wafers were cut from the ingots' tops and bottom. The electronic quality was investigated in terms of minority carrier diffusion length maps measured by the Elymat [1] technique, resistivity maps (4 point probe) and the oxygen impurity content (FT-IR). Adjacent wafers were characterized (A) as grown, (B) after standard P-diffusion and (C) after P-diffusion plus oxidation and (D) after a furnace (=TD) anneal of 650°C (2h in nitrogen). All wafers (A) to (D) were KOH damage- etched (25µm of material removed on each side). For the Elymat measurements a 6µm thick layer including the emitter and oxide layers is removed from each wafer (B) and (C) prior to the Elymat measurements. Simple 300µm thick n^+p test cells without back surface field, using

screen printing contacts, random pyramid surface texturization and TiO_x antireflection coating, were processed from these wafers keeping track of ingot position. The cells were characterized by I-V characteristics under a calibrated AM 1.5 illumination.

3. RESULTS

3.1 Wafer Characterization

Figure 1 shows the diffusion length and resistivity maps of a damage etched and a P-diffused wafer from virgin poly feedstock (ingot top). <L> and <ρ> stand for the laterally averaged values of diffusion length and resistivity, respectively. The resistivity map of the as-grown wafer reveals a clear ring structure with the lowest ρ values in the center and the outer perimeter. The corresponding diffusion length map appears to be inverted with a similar ring structure and the highest L-values in the center and the outer perimeter. After P-diffusion the laterally averaged ρ-value is decreased and the ring structure is slightly weaker. In the diffusion length map the ring structure has almost completely disappeared and the laterally averaged value is significantly increased. Figure 2 shows the bulk resistivity for each material for the top and the bottom of the ingots and before and after P-diffusion. There is a significant decrease of resistivity from top to bottom. Moreover, the bulk resistivity is significantly reduced by P-diffusion (note that the emitter was removed for the measurement). The differences between materials are less significant. Figure 3 presents the concentration of interstitial oxygen impurities [O_i] measured by FT-IR. [O_i] varies little between the materials, but decreases significantly from top to bottom of each ingot, too.

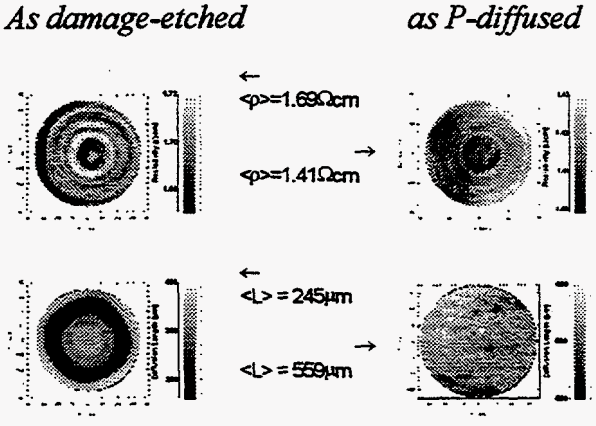

Figure 1: Wafer maps (virgin poly feedstock, ingot top) of resistivity ρ (above) and diffusion length L (below)

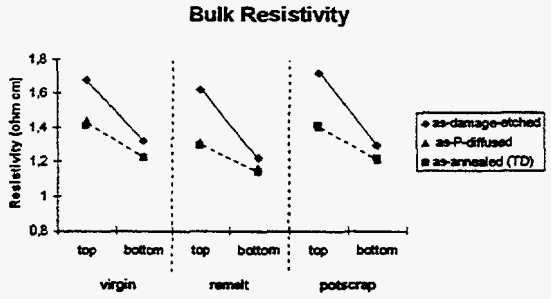

Figure 2: Laterally averaged bulk resistivity of top and bottom wafers from different feedstock materials after damage etch, P-diffusion and thermal donor (TD) anneal, respectively.

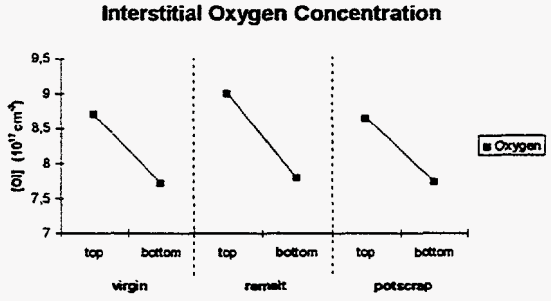

Figure 3: Interstitial oxygen concentration of top and bottom wafers from different feedstock materials

The similar variation of oxygen content and resistivity from top to bottom, the anti-correlation between diffusion length and resistivity maps and the decrease of resistivity after thermal treatment (here P-diffusion) indicate the presence of thermal donors which partially compensate the material and decrease the minority carrier lifetime and diffusion length. Thermal donors are well known oxygen related defect complexes which form at temperatures between 300°C and 500°C [2]. In order to prove this hypothesis both diffusion length and resistivity mappings were done before and after a typical thermal donor anneal (650°C, 2h) which is known to destroy these thermal donors [3]. The bulk resistivity decreases after the TD anneal for all wafers, see Figure 2. The new value is always equal to the resistivity measured after P-diffusion. We therefore can conclude: for both thermal treatments compensating donors which were introduced during growth are destroyed. As the concentration of thermal donors is known to increase (super-linear) with the initial oxygen concentration [2] a correlation between measured interstitial oxygen concentration and resistivity is indeed expected. In addition to that it is well established that the thermal history of the ingot during Cz growth favors the formation of thermal donors at the seed end (ingot top) [3]. The observed changes of resistivity due to the TD anneal indicate a high concentration of thermal donors at the ingot tops causing compensation ratios in the order of 25%. The relative resistivity variation from top to bottom decreases from 27% for the as-grown ingots to 13% after thermal treatment (average of ingot tops). The remaining axial gradient is usually attributed to the segregation behavior of boron [3].

Figure 4 shows the diffusion length of top and bottom wafers from the three different materials after damage etch, after P-diffusion and after TD anneal. The diffusion length increases after TD anneal for all wafers except potscrap-bottom. The diffusion length averaged over all materials are 259 µm (damage etched), 402µm (P-diffusion) and 340µm (TD anneal). Figure 5 shows the relative increment of diffusion length with respect to the as-damage-etched value for both annealed and P-diffused wafers. The response to P-diffusion varies from 120% for virgin-top to -5% for potscrap bottom. Both the increments and the absolute values of the diffusion length are smaller after TD than after P-diffusion.

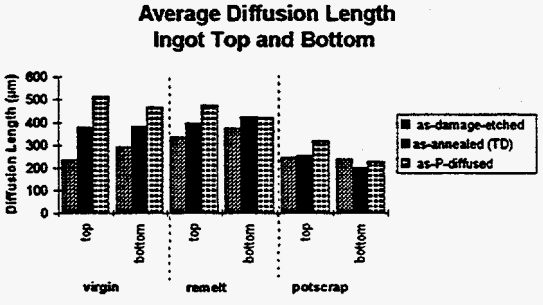

Figure 4: Laterally averaged diffusion length of top and bottom wafers from different feedstock materials after damage etch, P-diffusion and thermal donor (TD) anneal , respectively

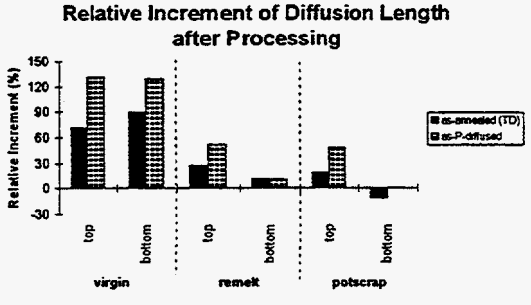

Figure 5: Increment of diffusion length relative to the as-damage-etched state after P-diffusion and TD anneal, respectively.

An increase of minority carrier lifetime or diffusion length after annihilation of thermal donors is expected as they are deep enough in the energy gap to act as recombination centers [2]. A significant contribution to the improvement of the materials after P-diffusion evidently is the annihilation of thermal donors. The surplus improvement of P -diffusion relative to TD anneal is most likely due to the well known gettering of metallic contaminants.

3.2 Correlation with Solar Cell Performance

Figure 6 shows the short circuit currents of cells fabricated from wafers of the three different feedstock materials (ingot averages) plotted against the average diffusion length L measured on as-damaged etched and on as P-diffused and oxidized wafers, respectively. The solid line presents a one dimensional model calculation with the solar cell modeling program PC1D for the simple 300μm n^+p cell structure. For this cell type only a variation of ΔJsc <1 mA (2.5%) is expected for a diffusion length range between 200μm and 500μm. The data points fall close to the simulated curve. Figure 7 shows the data on an enlarged scale. Included are lines fitted by linear regression and the correlation coefficients. The wafers measured closest to the completed solar cell process, i.e., after P-diffusion and oxidation, show the best correlation with the short circuit currents. The inferior correlation of the as-grown diffusion length with cell short circuit currents can be attributed, as shown above, to the changes of the materials upon thermal processes like TD annihilation or impurity gettering.

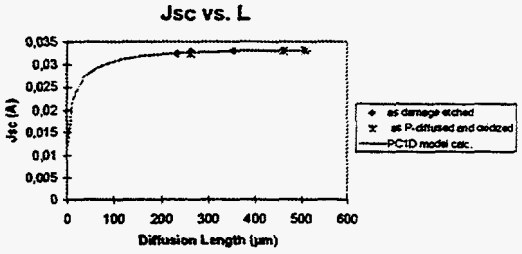

Figure 6: Short circuit currents Jsc (ingot averages) vs. diffusion length L measured as damage etched and after P-diffusion + oxidation; solid line shows a model calculation by PC1D

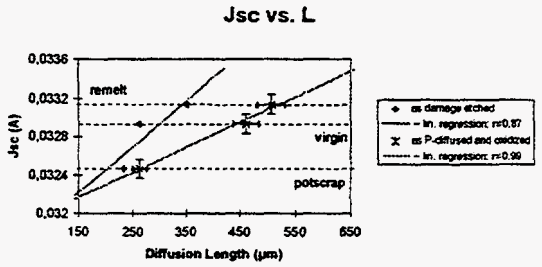

Figure 7: Jsc vs. L (ingot averages) measured as damage-etched and after P-diffusion + oxidation and corresponding regression lines.

4. CONCLUSION

Wafers and cells from ingots Cz-grown from virgin poly, remelt and potscrap feedstocks were investigated. It was shown that different materials vary with respect to their response to cell processing steps: ingots from potscrap show the smallest improvement of diffusion length. The correlation of resistivity, oxygen and diffusion length measurements revealed that thermal donors in the as-grown ingots decrease the diffusion length and partially compensate the p-type background doping. A reliable prediction of solar cell performance from electrical parameters requires thermal processing steps prior to characterization. The slightly (2%) lower currents of cells from potscrap feedstock could be attributed, in agreement with the PC1D calculations, to the lower bulk diffusion length after processing.

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[2] see for example: J. Michel and L.C. Kimerling, *Electrical Properties of Oxygen in Silicon*, in Semiconductors and Semimetals, Vol. **42** (1994) 251

[3] see for example: W. Zulehner and D. Huber *Czrochralski Grown Silicon*, in Crystals Vol **8**, Springer Verlag Berlin Heidelberg 1982, p. 3

PHYSICS OF IMPURITY GETTERING IN PV SILICON

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ABSTRACT

We review recent advances in the understanding of a variety of processes and mechanisms of gettering metallic impurities away from the device active regions to the created gettering regions. Particularly emphasized is the process of gettering metallic species in precipitated form, as they limit the solar cell performances and are difficult to be gettered.

I. INTRODUCTION

Gettering of metallic contaminants away from the device active regions already is an essential part of the integrated circuit (IC) manufacturing technology using Czochralski (CZ) Si wafers,[1,2] and is experiencing an increasing importance in Si solar cell fabrication for improving cell efficiency.[3-13] Gettering is needed because Si is an indirect bandgap semiconductor, with its lifetime component due to band-band activities on the order of 1 s and its normal lifetimes of much smaller than 1 ms are due to electrically active impurities (metals) and defects. Such impurity and defect electrical activities are responsible for the desirable fast action of switching devices, but also for the detrimental result of device/circuit failures due to excessively large pn junction leakage current and extremely short storage capacitor charge holding times. Point defects must be present to their thermal equilibrium concentrations. The presence of impurities is, however, an extraneous factor which can be controlled by cleaning and by gettering.

Gettering consists of: (i) the creation of suitable gettering sites; and (ii) the gettering processes of contaminants. Requirements on both issues for successful gettering differ between those used for the monolithic IC devices and bulk devices such as solar cell. For ICs, intrinsic gettering (IG) utilizing oxygen precipitates and associated defects in the CZ Si wafer bulk as gettering sites is used.[1,2] There is no profound need for improving the starting substrate quality, but during processing it is necessary to getter metal atoms introduced into Si. Since IC devices are monolithic, metal atoms can be gettered to the wafer bulk IG sites. In the last 20 years, extensive efforts have been devoted to studies of IG site creations.[1,2] For solar cells, IG is unsuitable because of the bulk location of IG sites. Only extrinsic gettering (EG) schemes with sites at wafer surface regions can be used. Also, a variety of Si substrates are used to produce solar cells: single crystal float-zone (FZ) and low oxygen content CZ wafers are used for high efficiency cells fabricated in clean facilities, while commercial solar cells are produced using low cost CZ wafers and large grain multicrystalline ribbons and wafers. The multicrystalline Si materials contain grain boundaries, dislocations, metal precipitates as well as dissolved metals. Moreover, commercial solar cell production facilities are not clean and would hence further contaminate the cells. Clearly, gettering is essential for improving the starting Si substrate quality as well as for guarding against contamination during processing.

A fair amount of effort has been recently devoted to identify the physics and to model the metal gettering processes, including metal dissolution from the precipitates (for multicrystalline solar Si), diffusion of metal atoms to, and their stabilization at the gettering sites.[14,15] The terms IG and EG are by the nature of gettering sites. Classification of gettering may also be according to the gettered metal stabilization mechanisms at the gettering sites: *relaxation* gettering and *segregation* gettering.[14,15] In relaxation gettering the impurity concentration in the gettering and gettered regions are the same at the gettering temperature. However, because of easy precipitate nucleation at the getter-

ing sites, during cooling impurities in the gettered region diffuse rapidly to the gettering region to precipitate out. Gettering of Cu[16] and Fe[17] by IG are examples of relaxation gettering. In segregation gettering, the impurities have already diffused to and stabilized in the gettering region at the gettering temperature, because of the segregation effect, i.e., the higher metal solubility in the gettering region than in the gettered region. Gettering by P indiffusion[18] and by the use of an Al-Si liquid layer[13] are model cases of segregation gettering.

II. PHYSICS OF GETTERING PROCESSES

II.1. Gettering Methods and Mechanisms

Recently a large effort has been devoted to physically and numerically model the impurity gettering processes without using empirical or fuzzy factors. The modeled gettering schemes include IG via the relaxation mechanism (for IC), and the EG methods of using P indiffusion and Al-Si liquid layers, via the segregation mechanism (for solar cells). The modeled impurities include Fe and Au. Fe is a common contaminant, while gettering of Au involves participation of also native point defects. Gettering by IG schemes for IC applications will not be discussed here, so that we can emphasize aspects relevant to solar cell applications.

An Al layer on the Si wafer surface provides a gettering effect because of *chemical* segregation. The solubility of other metals in Al is very high, reaching 1 at% in solid Al. Above the eutectic temperature of 577°C for which a liquid Al-Si alloy forms, the solubility of a typical metal can exceed 10 at%, or $5x10^{21}cm^{-3}$. Since the metal solubility limit in Si does not exceed ~10^{17} cm^{-3}, the segregation coefficient of the metal between the Al-Si liquid and Si is >10^4, reaching 10^{10} for many metals. This provides a tremendously large driving force for metal atoms to segregate into the Al-Si liquid layer. This gettering method should be highly effective for interstitial metal species because of their large diffusivities in Si and the large segregation coefficient. Solar cell efficiencies can be improved by the use of Al for a variety of reasons,[3-13] with gettering being one prominent contributor.[13]

Indiffusion of P into the surface of a Si wafer getters metallic impurities for two reasons. First, for metal atoms possessing a deep acceptor level, e.g., M^- or M^{2-}, a high concentration of P provides an *electronic* segregation gettering action because in the P diffused region the electron concentration is high which gives rise to a higher M^- or M^{2-} solubility than in the gettered region. Second, the gettering process of substitutional-interstitial metal species (s-i species, e.g., Au), which diffuse via the kick-out mechanism

$$M_s + I \Leftrightarrow M_i \qquad (1)$$

involving the consumption of the Si self-interstitial I, is enhanced by P-indiffusion because the process injects I to alleviate the I undersaturation in the gettered region created by the leaving of M_s atoms.

II.2. Fundamental Equations

The modeling effort has led to a number of physically correct equations for applications to the relevant gettering processes. Because of the involvement of the segregation processes, which occurs simultaneously with impurity diffusion, a diffusion-segregation equation is developed.[19,20] This equation reads

$$\partial C/\partial t = \partial\left[D\left(\partial C/\partial x - (C/m)(\partial m/\partial x)\right)\right]/\partial x\,, \qquad (2)$$

where m is the segregation coefficient of the gettered impurity species, with its value taken to be 1 in Si and in the Al-Si liquid to be the ratio of the metal solubilities in the Al-Si liquid and in Si. Alternatively, one can also use the empirical computational flux criterion,[21]

$$F_s = h\,(C_1 - C_2/m_2)\,, \qquad (3)$$

where F_s is the flux at the Si and Al-Si liquid interface, C_1 is the impurity concentration at the last computational grid point at the Si side of the interface, C_2 is the impurity concentration at the first computational grid point at the Al-Si liquid side of the interface, m_2 is the impurity segregation coefficient which is the impurity segregation coefficient in the Al-Si liquid relative to Si, and h is the *mass transport* coefficient. It has been recently shown[22] that $h=D^{eff}/\lambda$, where D^{eff} is an effective diffusivity due to the impurity jump frequency from the Al-Si liquid back into Si at the interface, and λ is the atom jump distance.

To treat the precipitation problem, a set of three coupled equations has been developed. For simplicity, the precipitates are assumed to be spherical in shape. These equations are

$$\partial C/\partial t = \partial\,[D(\partial C/\partial x - (C/m)\,(\partial m/\partial x))]/\partial x + 4\pi r\rho D\left(C^* - C\right), \qquad (4)$$

$$C^* = C^{eq} \exp\left(2\Omega\sigma/rk_BT\right), \qquad (5)$$

$$dr/dt = -\,\Omega D\left(C^* - C\right)/r\,. \qquad (6)$$

In Eqs. (4)-(6) C is the (metal) impurity atom concentration in the matrix, C^* is the impurity dynamic equilibrium concentration at the interface of Si and the precipitate with radius r, C^{eq} is the thermal equilibrium concentration of the impurity, ρ is the precipitate density, Ω is the volume of one impurity atom in the precipitate, σ is the precipitate-matrix interfacial energy density, and k_B is Boltzmann's constant. It is noted that Eqs. (4)-(6) apply to the precipitate growth as well dissolution processes.

To relate the influence of impurity concentrations on lifetime before and after gettering, the well known lifetime equations for dissolved impurities are used, and that for a precipitate of radius r is treated assuming diffusion limited carrier capturing process. For details of these aspects see the contribution of Pleckhanov et al. [23]

III. MODELING RESULTS

As examples of a large variety of numerical modeling results, we present that of gettering of precipitated Fe, and that of gettering Au.

III.1. Gettering of Precipitated Fe

The case of gettering precipitated Fe is of particular interest, because multicrystalline solar Si contain regions with high densities of dislocations and metal silicide precipitates, for which the minority carrier diffusion lengths are extremely low and cannot be improved by a normal gettering treatment using the Al-Si liquid layer.[24] We will show that the reason is that precipitate dissolution is involved which requires more extensive treatment.

Figure 1 shows the calculated results of gettering Fe in Si wafers 200 μm in thickness by a 2 μm thick Al-Si liquid layer at the wafer backsurface (at the 200 μm position). In general, Fe is assumed to have been introduced at a higher temperature to its solubility throughout the wafers and followed by two kinds of processes prior to gettering at different temperatures: (i) quenched; and (ii) annealed at a temperature lower than the Fe introduction temperature so that Fe exists in Si as dissolved atoms and in precipitates at the gettering temperature.

For the case shown in Fig. 1, Fe was assumed to have been introduced at 900°C to its solubility of ~4.3×10^{13} cm^{-3} and then precipitated out to steady state at 700°C to the density of $\rho=10^{11}$ cm^{-3}. It is seen from Fig. 1 that the attainable Fe concentration is substantially below its solubility at the gettering temperature. This is the result of the large Fe segregation coefficient between the Al-Si liquid and Si. In steady state, impurity distribution is dependent upon the segregation coefficient but not its actual concentration. On the other hand, the gettering process is extremely slow, resulting in: (i) it takes more than 60 h for the gettering process to reach the steady state Fe concentration of ~1×10^4 cm^{-3}, Fig. 1(b), instead of ~2.7 h for the case of having only dissolved Fe in Si, Fig. 1(a); (ii) to reduce the Fe concentration everywhere in the Si wafer to below 99% of the 700°C Fe solubility value of ~10^{11} cm^{-3}, it has taken already ~59 h, with precipitates located at the wafer frontside still not totally dissolved (not shown); (iii) for shorter times, the dissolved Fe concentrations in the Si wafer (and precipitate size, not shown) are highly non-uniform: they decrease monotonically from the frontside to the backside of the wafer. As ρ decreases, the needed gettering time is increased. For example, it takes ~260 h for the $\rho=10^{10}$ cm^{-3} case to reach the steady state. The primary cause for the low gettering rate is that the Fe precipitate dissolution rate is very low at the low gettering temperature, as it is limited by the Fe solubility value at that temperature.

Gettering at higher temperatures can speed up the gettering rate tremendously, but at two expenses. First, the eventually attainable Fe concentration is higher than that for a lower temperature gettering process, because the Fe solubility is higher at a higher temperature. Second, if quenched after gettering, there exists a characteristic time period for which the Si wafer lifetime will be degraded, and lifetime improvement is attained only for longer gettering times. The reason for the later phenomenon is also that the Fe solubility is higher at a temperature higher than the precipitation temperature. These aspects are discussed in detail in the contribution of Plekhanov et al.[23] They suggested a variable temperature gettering scheme for achieving both a high gettering rate and a high eventual gettering efficiency, see Fig. 2 and reference 23.

III.2. Gettering of Au

The case of gettering Au is of interest, because of the involvement of *I* and the existence of a synergistic effect when P-indiffusion and Al-Si liquid gettering schemes are simultaneously used.

To model P indiffusion gettering of Au, Gafiteanu et al.[22,25] wrote a set of 5 partial differential equations to account for the diffusion/change of P, *I*, *V*, Au_s, and Au_i, with the equation for Au_i in the diffusion-segregation form of Eq. (2). For obtaining numerical solutions, a set of known physical constants is used and first finely adjusted by obtaining fits to the gettered Au and the P indiffusion profiles of Sveinbjösson et al.[18] To model gettering Au by an Al-Si liquid layer, a similar set of equations is used. To model the combined use of P indiffusion and Al-Si liquid layer gettering, it was only necessary to combine the two cases and to adjust some boundary conditions. All simulation results are obtained with initial conditions corresponding to those of Sveinbjösson et al.,[18] because this is the only set of quantitative data available in the literature. Simulation results of gettering Au by the three methods, Fig. 3, show that the combined method is the fastest while the Al-Si liquid layer method is the slowest, and the combined method is also most stable while the P indiffusion method is most unstable. The physical reasons for these features are: (i) P indiffusion injects *I* to alleviate Au_i generation/migration induced *I* undersaturation in the Si matrix to provide a faster Au_s gettering rate than that of using an Al-Si layer which does not actively influence *I* concentration; (ii) in long gettering time cases the P indiffusion gettering is unstable because of the finite P source material (spread-on) used in experiments[18] and in the calculations. The combined method is superior because of the elimination of the shortcomings of both methods, and hence the *synergistic* effect. Note, another outstanding feature shown in Fig. is that, in either P indiffusion or Al-Si liquid layer gettering, for which the gettering sites are located on only one wafer surface, both wafer surface regions are gettered much more effectively than the wafer middle region. This *surface proximity* effect, instead of a *getterer proximity* effect, results from the *I* undersaturation induced by Au outdiffusion, and the facts that Au_i is fast moving and that both surfaces are perfect

Tan et al. 1987

I sources which alleviate the *I* undersaturation in the surface regions. We have obtained experimental evidences for the surface proximity effect using an Al-Si liquid layer to getter Au, Fig. 4.

IV. CONCLUSIONS

We conclude by mentioning that the major physical aspects for modeling gettering processes in solar cell processing have become available. It is desirable to develop a gettering simulation program, which requires further efforts. One aspect, which is in principle important, is that the precipitate nucleation process has not yet been treated up to now. A practical aspect we will shortly treat involves a distribution of metal precipitates of different sizes.

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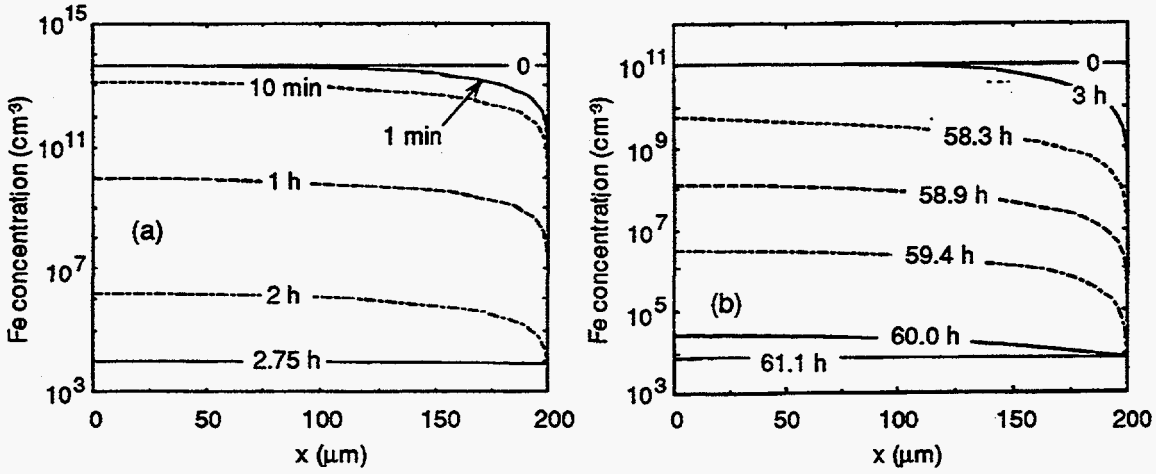

Fig. 1. Calculated Fe concentrations by gettering at 700°C using an Al-Si liquid layer placed at the wafer backsurface (the 200 μm position). Fe is assumed to have been introduced at 900°C to the solubility of ~4.3×10^{13} cm^{-3}. (a) That quenched to 700°C, i.e., with all Fe in solution, for gettering. (b) That annealed at 700°C prior to gettering to allow Fe to precipitate out to completion with $\rho = 10^{11}$ cm^{-3}.

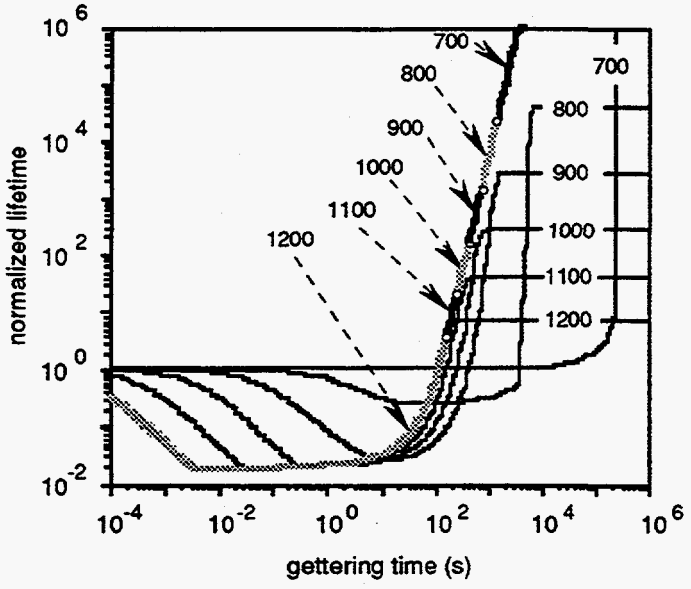

Fig. 2. Normalized carrier lifetime as a function of gettering times for the process carried out at different gettering temperatures. Fe precipitates are present in the Si wafers under conditions mentioned in Fig. 1.

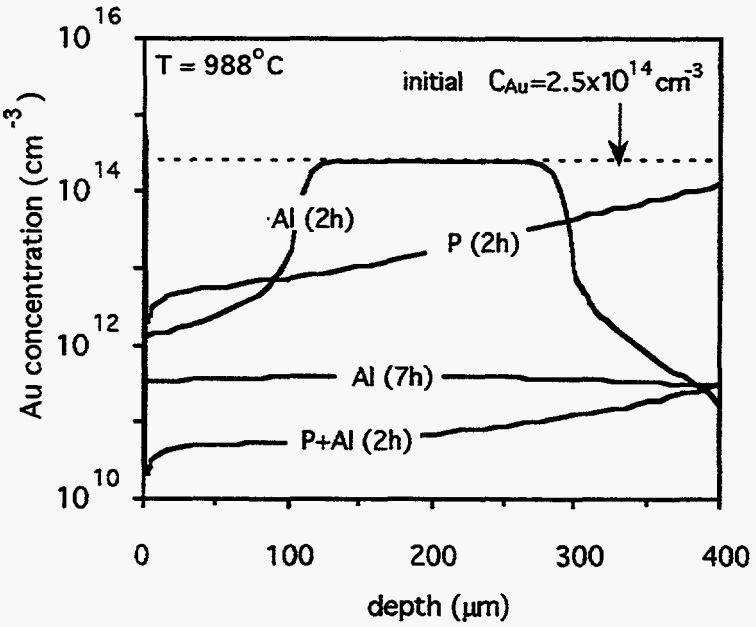

Fig. 3. simulated results of gettering Au from a 400 μm thick Si wafer, using P-indiffusion, the Al-Si liquid layer, and the combination of the two methods. Notice the surface proximity effect and the synergistic effect of the P+Al gettering case.

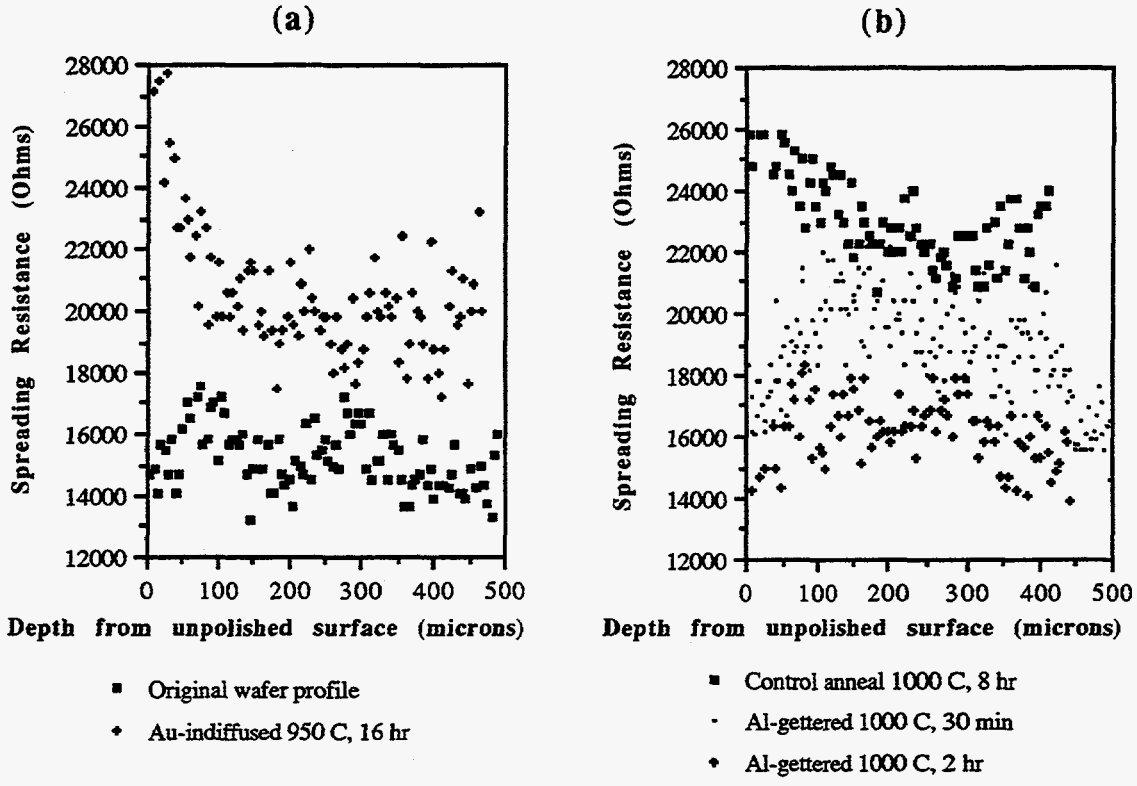

Fig. 4. Spreading resistance depth profiles of Si samples (a) from original wafer and after Au indiffusion at 950 C for 16 hr, (b) control annealed at 1000°C for 8 hr and after Al gettering at 1000°C for 30 min and for 2 hr respectively. Almost all profiles were measured from the unpolished wafer surface (at 0 micron depth). For the 30 min Al gettering, two samples were taken from adjacent locations and profiles measured from both surfaces (i.e., from 0 microns and 500 microns). The profile shown above is a composite of the two. For Au indiffusion as well as Al gettering, the metal films were on the left side of the profiles shown, i.e., on the unpolished wafer side.

Lifetime studies of multicrystalline silicon

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Abstract: The application of photoconductance measurements to investigate the electronic properties of multicrystalline silicon is illustrated with selected experiments, ranging from process control to fundamental research. Carrier trapping effects are discussed, and a technique based on controlled cross-contamination of hyper-pure silicon wafers with multicrystalline wafers is used to separately study the effect of metallic impurities. The variability of the effective lifetime with injection level is explained in terms of the Shockley-Read-Hall recombination model. Finally, the implications of effective lifetime on device voltage are pointed out.

1. INTRODUCTION

In spite of its extensive, and increasing, use in the photovoltaics industry, multicrystalline silicon (mc-Si) is still a relatively poorly understood material, even after twenty years of research [1]. Inherently, it is a complex semiconductor system where the crystalline lattice is interrupted at the grain boundaries and the volume is frequently populated by foreign atoms, micro-defects and dislocations. It is fundamentally non-homogeneous, with changing properties across the surface of a wafer and within the volume of an ingot. The growth conditions can have a strong effect on its quality and there can be significant differences between ingots grown with the same technique. Furthermore, several different methods are currently used to grow the ingots; we should, properly speaking, say that there are several multicrystalline silicon materials.

The characterisation of the electronic properties of mc-Si by means, for example, of lifetime testing, is complicated, owing to its non-homogeneity and to the co-existence of several different recombination mechanisms. Yet, lifetime measurements are the most useful tool available to study the physical limitations of mc-Si and overcome them. It is particularly important to study the possible changes induced by processing [2], a task that is facilitated by the use of simple, contactless measurement techniques. It has recently been realised that the lifetime of mc-Si can be nearly as high as that of single crystal silicon [3,4], that high temperature processing is not necessarily harmful to mc-Si [5,6], that the surfaces can be well passivated [7] and that high efficiency solar cell designs can be implemented in mc-Si wafers [5]. These advancements have led to conversion efficiencies over 18% [5,6,8] and open-circuit voltages over 650 mV [9]; the 20% efficiency mark has practically been reached [10]. These impressive achievements in the laboratory do not mean, however, that we have come to the end of the journey. Besides prime quality material and ultimate performance, research should be directed towards the mid and low quality mc-Si commonly used for mass production of mc-Si solar cells.

The measurement principles and the data analysis the quasi-steady-state photoconductance method (QSSPC) used preferentially in this study for lifetime testing are quite straightforward [11, 12]. Its application to different single crystal and multicrystalline silicon (mc-Si) wafers with different

dopant densities, contamination levels and crystallographic quality is described here. The advantages of the QSSPC technique over the classical transient PCD method to characterise non-homogeneous materials are first illustrated with a simple experiment. The QSSPC method is then used to monitor the effect of a phosphorus gettering process. The variability of the *effective* minority-carrier lifetime with excess carrier density concentration is explored in some detail. Controlled cross-contamination of FZ wafers is used to separately study the effect of metal impurities on carrier recombination mechanisms. This technique combined with gettering, which leaves crystallographic defects as the primary cause of recombination, and the systematic application of lifetime testing lead to a better understanding of multicrystalline silicon.

2. AVERAGE LIFETIME OF NON HOMOGENEOUS MATERIALS

Agreement between the transient and steady sate methods is not to be expected in all cases. On the contrary, we have found that the transient PCD method frequently overestimates the lifetime in non homogeneous materials, in particular, mc-Si. To demonstrate this, we prepared a 1 Ωcm FZ silicon wafer with passivated phosphorus diffusions on both sides and dipped half of it in HF to strip the passivating oxide. We measured the effective lifetime on both halves of the wafer and obtained 280 μs for the passivated side and 6.5 μs for the de-passivated side. The sample was then centred on the inductive coil of the photoconductance instrument, which is about 2 cm in diameter and the lifetime was measured sequentially using the transient PCD and the QSSPC techniques. The PCD lifetime was almost identical to that of the best half of the sample, about 280 μs. The QSSPC lifetime was significantly lower, 165 μs, very close to the average of the lifetimes of the good and bad regions of the sample. (The small discrepancy with this average, (280+6.5)/2=143 μs, can be explained by the 14% error of our QSSPC set up when trying to measure lifetimes as high as 280 μs).

Clearly, the transient technique can have a tendency to emphasise the highest lifetime present in the sample since the contribution from low-lifetime areas to the photoconductance vanishes quickly and is no longer present in the region of the decay curve typically used to determine the lifetime. The experiment described above confirms the theoretical expectation [13] that a steady state measurement should give an area-weighted average of the different lifetimes present in a non-homogeneous material. This is particularly relevant for multicrystalline silicon, where the QSSPC method gives a more realistic representation of its quality. Table I compares the QSSPC and transient PCD measurements of one single crystal FZ wafer and two multicrystalline silicon wafers (gettered). The QSSPC method can be expected to over-estimate the lifetime by about 10% for lifetimes in the range of 200 μs, which is actually observed in the FZ sample. Despite this tendency to over-predict the lifetime, the QSSPC method gives lower, more realistic, lifetimes for the mc-Si wafers.

Substrate	*QSSPC measurement,* τ_{eff}*(μs)*	*PCD measurement,* τ_{eff}*(μs)*
FZ (1 Ωcm)	180	170
mc-Si (1.5 Ωcm)	190	260
mc-Si (1.5 Ωcm)	120	220

Table I. Comparison between transient PCD and quasi-steady-state photoconductance (QSSPC) measurements of single crystalline and multicrystalline silicon wafers. From [13].

3. DEPENDENCE OF THE EFFECTIVE LIFETIME ON EXCESS CARRIER DENSITY

In the quasi-steady-state technique it is easy to sweep through a range of light intensities by means, for example, of a xenon-bulb flash and take hundreds of data points within a flash duration of about 7 ms. If the decay rate of the light is 2.3 ms, the discrepancy between this quasi-steady-state measurement and a true steady-state one is less than 10% for effective lifetimes lower than 200 μs. This facilitates the study of the injection dependence of the effective lifetime. The data contain much more information that just a single lifetime value; studying the dependence of τ_{eff} with carrier density can give insight into the nature of different recombination mechanisms.

3.1 A phosphorus gettering experiment

Phosphorus gettering is a well-known process to improve the electronic quality of mc-Si wafers. Measurements of the lifetime before and after the gettering treatment are essential to asses its efficacy and to optimise the process. Several mc-Si and CZ wafers were cleaned and subjected to a light $POCl_3$ diffusion at 840 °C, "in-situ" oxide passivation at 900 °C and forming gas anneal 400 °C; the sheet resistance of the n-type diffusion was 460 Ω. The effective lifetime was measured using the quasi-steady-state (QSSPC) method. The wafers were then etched to eliminate the previous lightly diffused regions and subjected to a phosphorus gettering treatment at 900 °C for three hours. Subsequently, the heavy phosphorus diffusion was removed (about 10-15 μm of silicon were etched) and a new light diffusion was performed in the same conditions as the initial one.

Fig. 1 shows the inverse of the measured effective minority carrier lifetime as a function of the excess carrier density for one CZ and two mc-Si wafers. These graphs visualise the overall recombination rate at a given carrier density. The beneficial effect of the gettering treatment on the mc-Si wafers is remarkable, although it is not identical for all wafers. A 0.2 Ωcm wafer (not shown) remained essentially unchanged. Samples M1 and M2 have almost the same resistivity, 1.5 Ωcm, although they come from different ingots; notably, the resistivity of M1 was obtained with a compensation factor of 1.5. The lifetime of M2 increased with gettering a factor of 10, to about 200 μs, while that of M1 doubled, to about 50 μs.

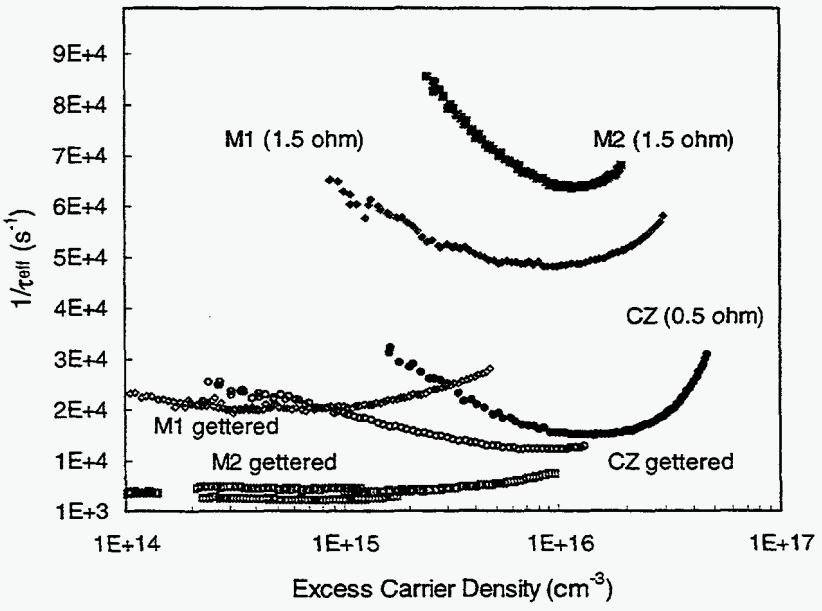

Figure 1. Pre- and post-gettering measurements of one CZ and two multicrystalline silicon wafers.

It is also interesting to note that the shape of the curves changes with gettering. In particular, the variability of τ_{eff} with injection

level becomes much weaker. This indicates that the initial strong variability of τ_{eff} at low injection levels is very likely a fingerprint of the metallic impurities present in the wafers. The efficacy of the gettering treatment seems to be highest for wafers that had a stronger variation of the lifetime at low injection levels before gettering. In the following sections we investigate the variability of the lifetime in more detail.

3.2 The Shockley-Read-Hall recombination mechanism

The variability of τ_{eff} at low injection shown in Fig. 1 for the pre-gettered wafers can be explained by the classical treatment of bulk recombination developed by Shockley, Read and Hall [14]. The expression for the bulk minority carrier lifetime, simplified to the case of a p-type region and recombination centres located in the middle of the energy gap, is

$$\tau_{(SRH)} = \tau_{no} + \tau_{po}\frac{\Delta n}{\Delta n + N_A} \qquad (1)$$

According to Eq.1, $\tau_{(SRH)}$ would increase with injection level from τ_{no} to $\tau_{no}+\tau_{po}$. If the electron and hole capture cross sections were identical, this could represent a doubling of $\tau_{(SRH)}$. Larger changes are actually possible if, for example $\tau_{po}>>\tau_{no}$. At very high light intensities, the effective lifetime is affected by recombination at the phosphorus diffusions used to passivate the surfaces of these wafers. This produces, together with the Auger recombination mechanism, the upward trend in the $1/\tau$ vs. Δn curves shown in Fig. 1. The overall variability of the effective lifetime can be described with the following expression:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{(SRH)}} + \frac{J_o}{qn_i^2 W}\left(N_A + \Delta n\right) \qquad (2)$$

Fitting the experimental data with Eq. 1 and 2 it is possible to determine the fundamental electron and hole lifetimes. The results corresponding to the curves in Fig. 1 are given in Table I.

	Max. τ_{eff} (μs)	τ_{no} (μs)	τ_{po} (μs)
M1 (mc-Si)	20	16	30
M2 (mc-Si)	15	7.5	25
CZ (pre-getter)	62	15	250
CZ (post-getter)	75	45	400

Table I. Fundamental electron and hole lifetimes for the multicrystalline and CZ wafers of Fig. 1.

4. LIFETIME MEASUREMENT OF MULTICRYSTALLINE SILICON

4.1 Lifetime map of a mc-Si ingot

Measuring the lifetime of wafers from different regions of a multicrystalline silicon ingot is an interesting exercise. A diversity of situations with different degrees of contamination and crystallographic quality naturally happen in a typical ingot growth process. In this experiment [15] we used wafers provided by Eurosolare Spa. The wafers came from two different ingots grown by directional solidification. A light $POCl_3$ diffusion at 840°C for 25 minutes followed by thin oxide

layer growth at 900°C for 30 minutes and FGA at 400°C was used to minimise recombination at the surfaces. The effective lifetimes of several 0.9 Ωcm wafers from ingot #6, measured with the QSSPC technique, are shown in Fig.2. Wafers from the central part of the ingot showed a significantly better electronic quality than wafers from the top and bottom regions. Without the additional information provided by the cross-contamination experiment described below, it is impossible to determine the physical origin of the low lifetimes measured for some of the wafers; at this stage both crystallographic defects and metallic impurities are possible (and likely) reasons.

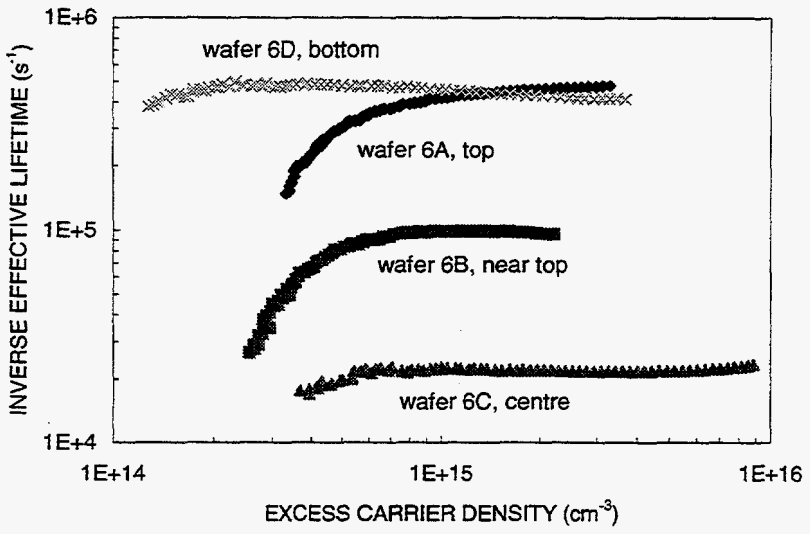

Figure 2. Experimental measurement of the effective lifetime of wafers from different regions of a cast multicrystalline silicon ingot (ingot #6).

4.2 Carrier trapping effects

Although the most immediate way of summarising the measurements shown in Fig. 2 is to report a single lifetime value corresponding to the range where τ_{eff} is reasonably constant, the data show an apparent increase of τ_{eff} as the light intensity and the carrier injection level decrease. Because of this, a direct measurement of the lifetime at the normal operating conditions of a solar cell (below 1 sun) is practically impossible. An advantage of the QSSPC set up is that it facilitates the measurement at high light intensities, where the effect saturates, or is swamped, and a realistic lifetime can be observed. Obviously, extrapolating the lifetime measured at high light intensities to predict the performance at one sun can be inaccurate, but it is better than having no information at all or believing in an anomalously high lifetime.

The behaviour of the effective lifetime of many mc-Si wafers at low intensities can be explained by a carrier trapping effect consisting of the temporary retention of electrons in relatively shallow energy levels in the band gap. We have adapted a previous theoretical model to the practical situation of a QSSPC measurement [16]. The model is based on the simultaneous presence of deep traps, primarily responsible for carrier recombination, and shallow traps that produce a distortion in the measured photoconductance while contributing negligibly to carrier recombination. In essence, the shallow traps reduce the number of free electrons available for recombination and conduction processes. The external illumination generates electrons and holes in equal numbers; many electrons are trapped and do not contribute to the photoconductance, although the holes do. The number of free electrons is thus reduced and the overall recombination rate is lower. The effect is more noticeable at relatively low illumination levels, when the fraction of trapped electrons is significant.

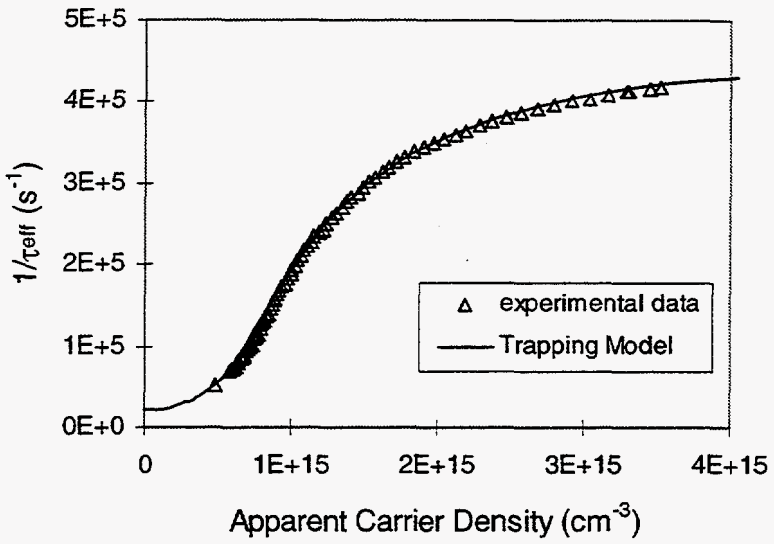

Figure 3. Photoconductance measurement of multicrystalline Si wafer 8A, from the bottom of ingot #8 showing trapping. The continuous line is a fit using the trapping theoretical model.

The trapping model explains the experimental dependence of the effective lifetime on injection level very well and allows the trap density to be determined. As an example, Fig.3 shows the model fitted to a mc-Si wafer from ingot #8. Preliminary evidence suggests that this "trapping" effect might be related to crystallographic defects in the material. Metallic impurities produce the opposite type of behaviour, as we shall see later. Ingot #8, which was suspected to be defective due to problems during the growth process, proved to be of inferior quality and showed much more pronounced trapping. Wafers from the top of ingot #6 also showed more pronounced trapping than wafers form the central region (see Fig. 2), and this is probably correlated to the higher dislocation density measured in them.

5. RECOMBINATION DUE TO METALLIC IMPURITIES

Cross-contamination between mc-Si and ultra-pure FZ wafers can be used to detect the presence of metallic impurities in the mc-Si wafers [17]. The cross-contamination occurs when high purity float zone wafers are placed very close to the mc-Si samples during a high temperature step: a proportion of the mobile impurities present in the multicrystalline wafers effuse out of them and is absorbed by the adjacent float zone wafers. The process is very much like phosphorus (or boron) doping using solid sources; in this case the mc-Si wafers are the dopant sources and the dopant species are transition metals.

Several controlled cross-contamination experiments consisting of a light $POCl_3$ diffusion at 840°C for 25 minutes followed by thin oxide layer growth at 900°C for 30 minutes, were performed on wafers from various regions of two commercial cast mc-Si ingots. The lifetime of the control wafers was directly correlated to the lifetime of the adjacent mc-Si wafers and the corresponding ingot region, as can be seen in Table II. Considering that the typical lifetime of a clean 1 Ωcm FZ wafer processed in an identical way is of the order of 400 μs, the results indicate that the concentration of mobile impurities is low in the central region (control wafer lifetime 330 μs), while it is high at the bottom of the ingot (most likely due to contamination from the crucible), and also at the top (caused by transition metal segregation during ingot growth) [15]. Subsequent SIMS measurements identified the presence of Fe and Cr both in the mc-Si wafers and in the cross-contaminated FZ wafers.

In an elegant way, the cross-contamination technique transfers the metallic impurities to a crystallographically perfect medium where their effect on carrier recombination can be studied without the combined influence of grain boundaries, dislocations and other defects present in the

mc-Si wafers. In fact, trapping effects make it impossible to explore the low carrier density range in many mc-Si wafers, particularly those from the defective ingot #8. Figs. 4 and 5 show the results of intentional cross-contamination experiments that used 1 Ωcm FZ wafers as controls, a resistivity that is quite common for commercial solar cells. It is reasonable to think that, for a given level of contamination, the lifetimes of the 1 Ωcm FZ wafers are an upper bound of those achievable with mc-Si wafers of the same resistivity. Nevertheless, the concentration of metals in the FZ wafers is lower than that of the source mc-Si wafers and, very likely, it is higher near the surfaces than in the volume of the wafers.

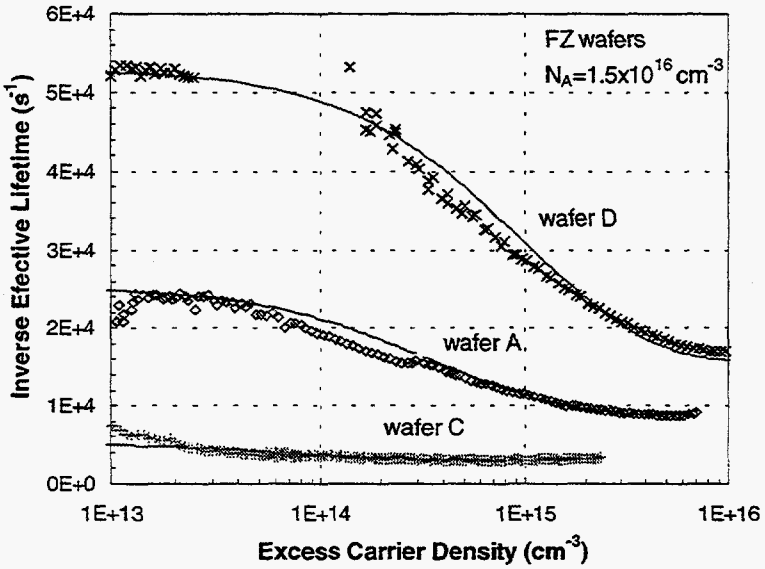

Figure 4. Inverse effective lifetime as a function of carrier density for three float-zone 1 Ωcm silicon wafers having different degrees of contamination from top (wafer FZ8D), centre (wafer FZ8C) and bottom (wafer FZ8A) regions of multicrystalline silicon ingot #8. The continuous lines are theoretical fittings using the S-R-H recombination model.

The experimental lifetimes shown in Figs.4 and 5 for FZ control wafers corresponding to the central and end regions of ingot #8 (crystallographically defective) and ingot #6 (standard quality), respectively, show a dependence with carrier density that can be modelled with a single S-R-H recombination level. The data can be fitted with Eqs. 1 and 2 using the fundamental τ_{no} and τ_{po} given in Table II. The ratio between τ_{no} and τ_{po} is not the same for all the wafers, indicating that the recombination centres are probably different.

	Max. τ_{eff} of control FZ (μs)	τ_{no} (μs)	τ_{po} (μs)	*Contamination source*	*Max. τ_{eff} of mc-Si source wafer (μs)*
FZ 8A	110	50	2000	bottom, ingot #8	1.9
FZ 8D	60	21	300	top, ingot #8	1.2
FZ 8C	330	400	10^5	Centre, ingot #8	4
FZ 6A	45	30	250	Top, ingot #6	2.3
FZ 6B	100	50	1500	Near top, ingot #6	10

Table II. Recombination parameters of 1 Ωcm FZ wafers cross-contaminated by mc-Si wafers from different regions of two multicrystalline silicon ingots.

To complete the experiment, the mc-Si wafers (and also some cross-contaminated FZ wafers) were subjected to a $POCl_3$ gettering treatment followed by silicon etch and an additional light diffusion to passivate the surfaces. The FZ controls recovered the high lifetimes typical of the uncontaminated state. The gettered mc-Si wafers did not produce cross-contamination, indicating that the 3h, 900 °C gettering was sufficient to extract the majority of the mobile metal atoms. Most of the mc-Si wafers that had been identified as containing a high density of mobile impurities by the previous cross-contamination experiment improved markedly with phosphorus gettering. Nevertheless, wafers from the top region of both ingots had a very high density of dislocations (>10^6 cm^{-2}) and did not improve with gettering [5]. The final lifetimes of the gettered mc-Si wafers can be considered to be a measure of their crystallographic quality. This quality proved poorest at the top of the ingots. To predict the response to gettering the cross contamination experiment needs to be complemented with a measurement of the dislocation density.

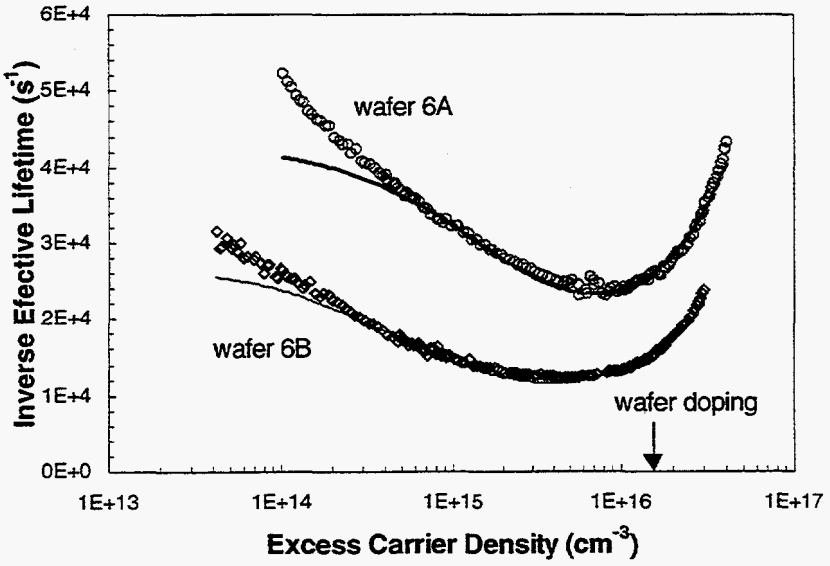

Figure 5. Experimental (open markers) variation of the effective lifetime with excess carrier density for two 1 Ωcm FZ wafers contaminated with mc-Si wafers from top (wafer FZ6A) and near top (wafer FZ6B) regions of ingot #6. The continuous lines are the corresponding S-R-H fits.

6. DEVICE IMPLICATIONS OF METALLIC CONTAMINATION

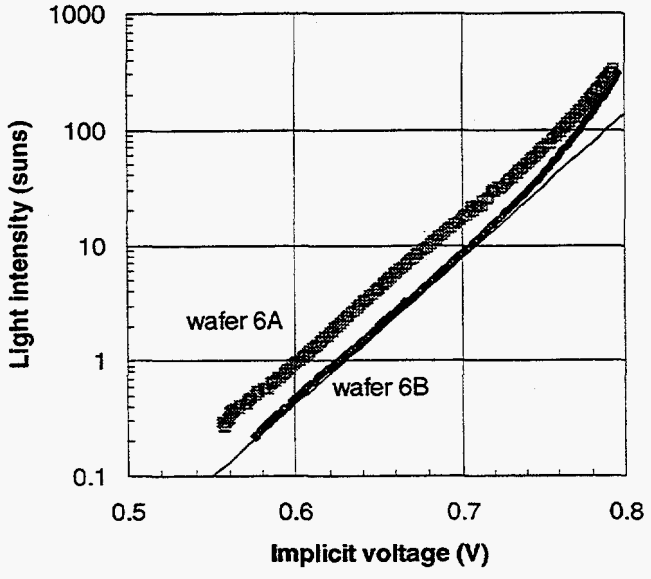

Figure 6. Implicit voltage vs. light intensity of two FZ wafers (FZ 6A and FZ 6B) with phosphorus diffusions on both sides and different degrees of metallic contamination.

As shown in the previous sections, the detailed analysis of the photoconductance data can be quite complex. A much more straightforward way of presenting them is to use the well-known language of device voltage [18]. This is shown in Fig. 6 for two 1 Ωcm FZ silicon wafers having phosphorus diffusions on both sides. These particular wafers were intentionally

cross-contaminated with the mc-Si wafers from ingot #6 (their corresponding effective lifetimes are shown in Fig.5) and exhibit a relatively high recombination rate, higher than standard 1 Ωcm FZ material. The implicit open-circuit voltages at one-sun illumination are 600 mV and 625 mV for wafers F6A and F6B, respectively. The straight line in Fig. 6 is a single-exponential fit to the implicit I_{sc}-V_{oc} characteristics with a $J_o \approx 1.3 \times 10^{-8}$ Acm^{-2} and an ideality factor of 1.35. The ideality factor decreases to nearly 1 only at very high light intensities. This relatively high ideality factor can be expected to have a detrimental effect on the fill factor of a solar cell fabricated with this wafer. Interestingly, the origin of high ideality factor and low fill factor can be traced to the presence of metallic impurities in the material.

7. CONCLUSIONS

The experimental fact is that carrier recombination in a semiconductor is complex and can not, in general, be accurately described by a constant lifetime value except within a restricted range of carrier densities. The *effective* minority-carrier lifetime can be affected by several physical mechanisms simultaneously that can have different dependencies on carrier injection level. The analysis of the injection dependence of the effective lifetime provides insight into these mechanisms.

The specific dependence of the effective lifetime on injection level can be quite different for multicrystalline silicon wafers. Frequently, it *increases* with injection level at very low carrier density levels, goes through a maximum and then decreases at high injection levels. The most likely physical reason for the measured dependence at low injection levels is that the bulk minority carrier lifetime *increases* due to the nature of the SRH recombination mechanism in the volume of a semiconductor. The strong change of τ_{bulk} observed in many samples can be explained with a high asymmetry in the electron and hole fundamental lifetimes. We have found evidence that, at least in some cases, the magnitude of SRH recombination is related to the concentration of metallic impurities in the material. Translated to the language of device voltage, the injection-dependence of the effective lifetime can produce increased ideality factors in the current-voltage characteristics and reduced fill factors and output voltages.

There are, nevertheless, cases where the apparent effective lifetime increases monotonically as the injection level is decreased. This behaviour, frequent in multicrystalline silicon, can be explained in terms of carrier trapping effects. The origin of these traps is still uncertain, with preliminary evidence indicating that they might be related to the crystallographic quality of the material, including the grain size and the dislocation density. If such correlation can be confirmed, measurements of the trapping effect might be very useful to diagnose the crystallographic quality of multicrystalline silicon.

Aknowledgement

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MINORITY CARRIER LIFETIME AND SPV INVESTIGATIONS IN PV

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Both the microwave photoconductive decay (μ-PCD) and the surface photovoltage (SPV) are fast, non-contact, non-destructive techniques for monitoring carrier lifetime in silicon material. They are also capable of performing high resolution mapping of whole samples this way offering a practical tool for the identification of the source of a given contaminant. Even if these techniques are meant to measure practically the same material characteristics (carrier lifetime or diffusion length), both methods have their own advantages when applied in the field of photovoltaics.

A special realization of the μ-PCD technique is when frequency tuning is used to optimize the microwave signal to the given sample. This approach offers considerable flexibility this way making possible measurements of a variety of samples. Contamination pattern recognition or even the identification of contaminants could be performed either in the starting material like silicon ingots and blocks or in the final products i.e. solar cell or panel. A variety of measurement examples are provided to demonstrate the above capabilities of the μ-PCD technique.

Nevertheless, the result obtained from the μ-PCD investigation is a lifetime at high carrier injection level. On the other hand, the parameter that has a closer relationship to a solar cell operation is the diffusion length which is measured by the SPV technique. Therefore, this latter method has its own role in process monitoring in photovoltaic industry. Measuring results based on SPV investigations are provided, and furthermore compared to μ-PCD data.

Present Status of the Surface Photovoltage Method (SPV) for Measuring Minority Carrier Diffusion Length and Related Parameters

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Abstract:

We present an overview of the physics and practical issues related to surface photovoltage measurements of the minority carrier diffusion length and its application to monitoring recombination center defects in silicon. A tutorial description is given of the role of pertinent processes like injection, recombination and trapping. The evolution of the SPV method is presented followed by a description of the most recent refinements addressing the measurement of long diffusion lengths in silicon wafers with emphasis on accuracy, measuring speed, tool-to-tool reproducibility and, practically the most important question of monitoring iron concentration.

Texturization technologies of multicrystalline silicon

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Abstract

In recent years multicrystalline silicon solar cell technology has gained an increasing PV market penetration. This is caused by its excellent cost reduction potential with relatively short economy-of-scale energy amortization periods compared to monocrystalline silicon. Most of the newly installed crystalline silicon solar cell production lines all over the world are relying on conventionally cast or ribbon multi Si substrates. An important prerequisite is however the achievement of high solar cell efficiencies. A major contributor to the gap between the performance of the best single crystalline solar cells and those prepared from multicrystalline material is the general inability to texture the latter using the standard anisotropic wet chemical etching approach. This is so because only a fraction of the grains of multi Si are close to the (100) orientation required. This complete lack of simple and cost effective texturing techniques for multicrystalline silicon has stimulated their design and development over the past years.
The present work tries to provide an overview of the techniques available and their respective state-of-the-art. In the first part the physical background of the effect of texturization within a solar cell such as the reduced light reflection, an enhanced electrical charge carrier generation probability and the better light trapping of weakly absorbed long wavelength photons will be discussed based on two dimensional device simulations. In a subsequent section the texturization technologies currently investigated will be summarized such as isotropic, anisotropic as well as electro-chemical etching methods, dry plasma etching approaches, laser texturing and different mechanical structuring methods such as fast rotating texturing tools, wire saw texturization, and diamond scribing. Particular emphasis has been put on the latest results at the University of Konstanz concerning the development of a fast mechanical texturing technique. It is based on cylinder-like tools micro-mechanically profiled and coated with an nickel/diamond abrasive layer which are mounted on a high frequency spindle of a silicon dicing machine. Macroscopic V-groove-like surface textures with typical structure dimensions in the range of 50 to 100µm as well as microscopical textures with profile depths below 10µm can be obtained in multicrystalline silicon with a high throughput (one wafer per second) and at a low cost (smaller 5 US cent per wafer). An efficiency gain larger than 5% relative after cell encapsulation could be accomplished in an industrial manufacturing environment. This review will close with a comparison of the presented texturization technologies focusing on their effectivity in solar cell efficiency enhancement and their industrial up-scaleability. The full review paper can be obtained at the workshop.

Advances in Solar Cell Metallization in the Manufacturing of High Efficiency Silicon Solar Cells

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Abstract:

Future growth in the PV market will come from lower cost product. However it is the total installed cost which is important and not the factory gate module price. This requirement points to high efficiency solar cells as the preferred PV technology. Laboratory methods of delivering high efficiency solar cells are well known and rely on non cost effective technologies but do indicate the direction manufacturing should take. The ability of screen printing and plating technologies to manufacture cost competitive solar cells will be discussed. The advantages of the laser grooved buried grid solar cell are described together with the potential for further improvement.

Introduction

While the photovoltaic market has been growing strongly in recent years, the fact remains that PV generated electricity is only cost competitive in small stand alone systems of less than 2 kWp. Various financial subsidies, from governments or electricity users, have been given around the world to develop an on grid-market for systems of 1 kWp to megawatts. A truly sustainable market will only develop when PV generated electricity costs are comparable to conventionally generated costs, given a realistic premium for PV for low environmental impact. PV electricity costs are determined the total installed system price which is typically twice the factory gate module price, for crystalline silicon modules. However when comparing silicon solar cell modules with other technologies, the possibility exists that lower efficiency modules might have lower factory gate process but higher installed cost. The installed cost involve shipment to the site, structures and installation. These will be higher when lower efficiency modules are used to give a certain sized installation. It can be shown for Germany where labour costs are high that reducing the module cost by half but doubling the installation time will result in a higher total installed cost. By the reverse argument if higher efficiency modules than conventional silicon technology are produced for similar $/Wp costs then the whole installation cost is reduced in proportion to the increased efficiency.

Once the system is installed the cost of electricity from the array is determined by the actual kWhr generated over the life of the array in the particular location. It is increasingly recognised that the measurement of module power at STC is not necessarily a good guide to the actual kWhr's that a PV array will give under real operating conditions and indeed quite a range of performance has been observed in the kWhr/kWp for different PV module technologies. If it were assumed that all the PV technologies gave the same installed cost per Wp, then the technology delivering the highest kWhr/kWp value would give the lowest electricity cost. While the factors which control kWhr/kWp are complex it is clear that the diode quality in the cell is an important parameter in determining low light level efficiency of modules which is a strong contribution to high kWhr/kWp generation. Of necessity high efficiency solar cells will have good diode characteristics.

Thus it can be seen that a promising route to achieving the successful implementation of PV at the Gigawatt level is the development of cost effective technologies for high efficiency silicon solar cells. This paper discusses potential routes to large scale manufacture of high efficiency silicon solar cells. High efficiency is taken as above 16% for the purpose of this paper.

Concepts for High Efficiency Silicon Solar Cells

An efficiency of over 24% has been independently verified for the PERC structure developed by Green [1]. Other workers have obtained efficiencies over 22% [2,3]. These approaches have in common the use of high quality FZ wafers, good surface passivation, localised BSF's and excellent anti-reflection properties through inverted pyramids and double layer ARC. The metallisation evaporated Ti/Pd/Ag defined by photolithographic lift off techniques. These techniques do not yield cost competitive solar cells but they do show the potential which can be achieved and provide the road map for attaining high efficiency. the principal features are :-

(1) Good antireflection properties
(2) Surface passivation
(3) Fine grid lines (low surface shading)
(4) Lightly doped emitters
(5) Back surface field
(6) High bulk lifetime

The challenge is to find a cost effective way to deliver all these attributes within one solar cell structure. Historically the PV industry has tackled this task by evolving from the evaporated contact space solar cell. The evolution has been via some kind of electro-plated contact to screen printed contact which remains the dominant technology in world-wide production. The achievements and limitations of the screen printing process will be discussed before going on to look at the latest promising solar cell technology.

Screen Printed Solar Cells

The advantages of screen printing are that it gives a short and simple manufacturing process which is readily automated and makes use of the infrastructure of the major hybrid circuit manufacturing industry. A relatively low cost manufacturing process has resulted but efficiencies have been limited to below 15% in high volume manufacturing on commercial grade CZ wafers. The disadvantages of the process are grid lines have a minimum width of about 120 μm due to limitations in screen construction and paste rheology. In addition the emitter has to be highly doped to allow Ohmic contact with the silver screen printing paste. This high doping causes high recombination within the emitter and so the short wavelength energy in the solar spectrum is lost.

Intensive research has been carried out at IMEC and other institutes to overcome these disadvantages. Fine line printing of grid has lead to lines as thin as 70 μm being produced in a pilot line facility but in industrial production this is limited to around 100 μm. The disadvantages of the highly doped emitter have been overcome by using selective emitters where the area under the contact is more heavily doped than the rest of the surface. A range of techniques have been developed to produce this structure including, masking the contact and etching back the emitter, double diffusion, printing the dopant paste alone and autodoping the surface. All these techniques can be made to work but a high degree of precision in the printing is required. Good surface passivation can be obtained from deposition a PECVD silicon nitride which can be fired through by the metallisation during hydrogen into the silicon surface and enhancing the passivation. The screen printing process lends itself easily to producing back surface fields by printing aluminium on the rear surface. The higher than normal firing temperature to fire through the front contact is ideal for good BSF formation without balling of the aluminium in the rear contact and cells can be successfully co-fired. Combining these techniques has given cells of over 17% efficiency in monocrystalline cells and 16% in multicrystalline cells.

It can be seen that within the limits of the bulk lifetime of the material the route map to high efficiency has been followed closely.

Plated Contact Solar Cells

A hybrid approach which uses photolithography to define the front contact and screen printing the rear contract has been tried by Siemens Solar [4]. A front passivating oxide was used on the front surface and a grid line pattern opened by photolithography. A silver contact was then deposited on the front side by a rapid electroless plating of silver after an initial film of electroless nickel had been deposited. A rear surface BSF was formed by screen printing and firing aluminium paste. Cells with efficiencies up to 16.5% were produced. A pilot stage run produced an average efficiency of 16% and 14% efficient

modules were made. Although a 112 kWp installation was successfully made in SE Germany, the technology has not been further commercialised.

Laser Grooved Buried Grid Solar Cells

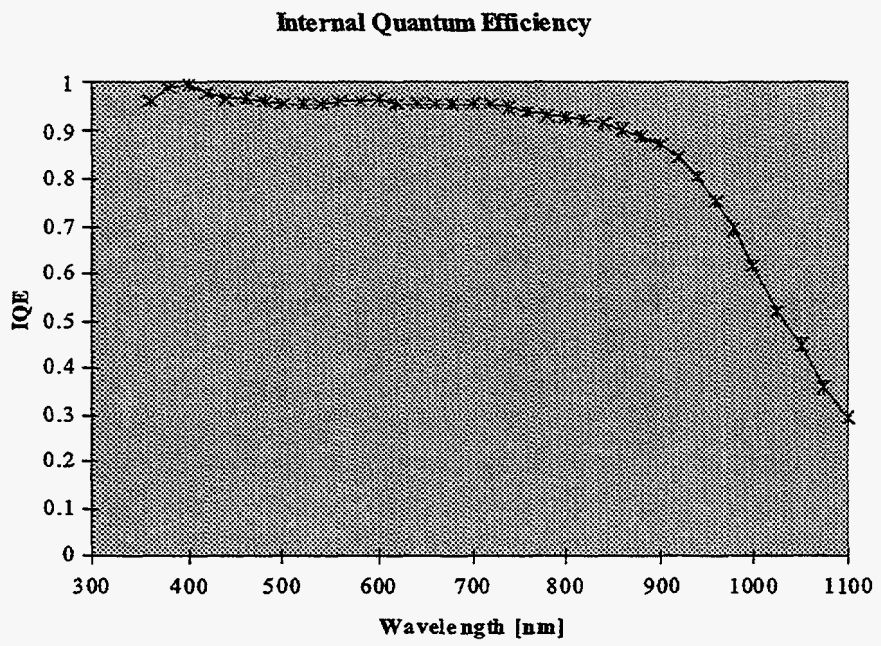

Figure 1. Internal Quantum efficiency of a 16.9% CZ LGBG Cell.

An alternative to screen printing is the LGBG cell in which the road map for high efficiency can be followed in a robust industrial process. The sequence of operations to produce the cell are well known. [4],[5]. The key features of the process are the laser grooving to produce fine grid lines of around 30 μm width and the selective emitter structure produced by a double diffusion. In the industrial process LPCVD silicon nitride is preferred to the oxide passivation of the research laboratory. This layer also acts as a diffusion mask in the two stage diffusion process and also acts as a plating mask for the electroless deposition of the metal contacts. A BSF is produced from evaporated aluminium. The nitride layer gives reasonable passivation with surface recombination velocities of <1000 cm/s. It can be seen from the spectral response (fig1) that the LGBG cell has very good short wavelength response. Using solar grade CZ wafers efficiencies of 16.5 to 17% (125 x125 mm p-square cells) are regularly achieved in high volume production and yields above 90%. Module costs per watt on similar throughputs are lower for the LGBG process than for screen printing in BP Solar's experience. The BP Solar España factory has recently been debottlenecked to 10 MWp throughput and is the largest solar cell factory in Europe.

As mentioned in the introduction the actual energy produced by a system is more important than the efficiency at STC. As has been reported elsewhere [6], the good diode properties of the LGBG cell, its excellent blue response and high efficiency down to low light levels combine to make the cell particularly effective over the annual climatic cycle and gives it some of the highest kWhr/kWp figures recorded as shown in table 1.

Table 1. kWh/kWp field performance of BP585 modules

kWh/kWp	*Location*	*Array Size*	*Year*
914	Baden-Rütihof	2.7 kWp	1996
900	Aachen	4.8 kWp	1995/6
1080	Feldis, CH	4.1 kWp	1995/6
1000	Canobbio, CH	3 modules	typical

The LGBG process is also very flexible and can be used to produce products very different to the standard flat plat module. Cells of over 20% at 18x have been demonstrated [7] and recent results show that this efficiency cab be expected at up to 40x. The most obvious example is the ease with which concentrator cells can be produced on the same line as one sun cells with little modification of the cell process. A 500 kWp concentrating system (40x) is currently being assembled in the Canary Islands to demonstrate the low cost potential of parabolic trough concentrators using LGBG cells [8].

The cells are also effective at low concentration. A novel module structure incorporating miniature CPC (Compound Parabolic collector) which gives up to 3x concentration without tracking for a wide acceptance angle. The structure of the CPC requires cells only a few mm wide if the CPC depth is to be kept to around 10 mm which is typical for PV modules in building applications. Cells approaching 17% efficiency at 3x have been made in high volume. This development opens the way to high efficiency modules using as little as one third the silicon of conventional designs.

The technology can also be adapted to use thicker than optimum ARC in a range of colours. This is important in increasing the size of the PV market by making solar cells more visually appealing to architects.

Conclusions

High efficiency solar cells are of critical importance in achieving a widespread deployment of photovoltaic technology. The way in which the metallisation is applied is critical to cost effectiveness in high volume manufacture of the solar cell. Screen printing technology continues to show the capability for further improvement. LGBG cell technology has now come of age in high volume production and shows an adaptability in high and low level concentration.

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Selective-Emitter Solar Cells - from Laboratory to Production Processes

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1. Introduction.

The typical efficiency of commercially produced crystalline silicon solar cells lies in the range of 13 - 16 %. Generally accepted future efficiency goals for the industrial solar cells are 18-20 % on monocrystalline and 16-18% on multicrystalline silicon. Pathways on how to achieve the efficiency objectives can be found in laboratory cell processing.
Although it is well known how to manufacture the high efficiency laboratory cells, direct transfer of these processes to production lines will create processing bottlenecks. Industrial processing techniques and materials are selected for the maximal cost reduction while maintaining a relatively good efficiency. Industrial solar cells are fabricated in large volumes mainly on large area ($\geq$100 cm^2) Czochralski monocrystalline or multicrystalline silicon substrates. The production processes and equipment should fulfil the throughput requirements of 1000 wafers per hour. These are the main reasons why only surface texturing , aluminium BSF and, to limited extent, surface passivation, have been applied in the solar cell production lines.
Currently a lot of effort is being spent in the development of the industrial type selective emitter processes. Until now, the only high volume production process employing the selective emitter structure is the Laser Grooved Buried Grid process developed by the University of New South Wales.
Lately, new diffusion and passivation techniques, combined with an improved screen printing metallization have lead to the development of a wide range of the industrial type selective emitters. This paper presents evolution of the IMEC selective emitter solar cells from laboratory to high throughput production type processes.

2. Optimization of silicon solar cell emitters for maximum cell efficiency.

The emitter region in silicon solar cells has been the subject of large number of experimental and theoretical studies[1-5]. These studies deal mainly with the emitter saturation current, surface recombination velocity and emitter quantum efficiency. Theoretical models, independently developed by many researchers, were able to calculate the conversion efficiency of thin and thick emitter silicon solar cells taking into account the surface recombination velocity, the Fermi carrier degeneracy, band-gap narrowing and Auger recombination. These studies lead to the conclusion that non-passivated emitters have better performance when the surface impurity is high ($N_s > 10^{20}$ cm^{-3}) while the well passivated emitter can benefit from the low surface recombination velocity if the surface doping concentration is low ($N_s \approx 10^{19}$ cm^{-3}).
King and co-workers [4] reported measurements of the saturation current density of transparent emitters, from which they determined the surface recombination velocity for oxide passivated surfaces as a function of surface phosphorus concentration. Using these data they generated contour plots of emitter saturation current density and emitter quantum efficiency. In combination with emitter sheet resistance contours this information can be used to design the cell optimal emitter profile.
However, the independent optimization of the emitter profile does not necessarily lead to an optimum cell conversion efficiency. The influence of several factors, such as the emitter sheet resistance, contact resistance and geometrical aspects, strongly affecting the fill factor, must be considered jointly.

An emitter optimization study for cells with evaporated and screen printed contacts taking into account all mentioned above factors has been presented by Demesmaeker[6]. We present here the results obtained for large cells with screen printed contacts.

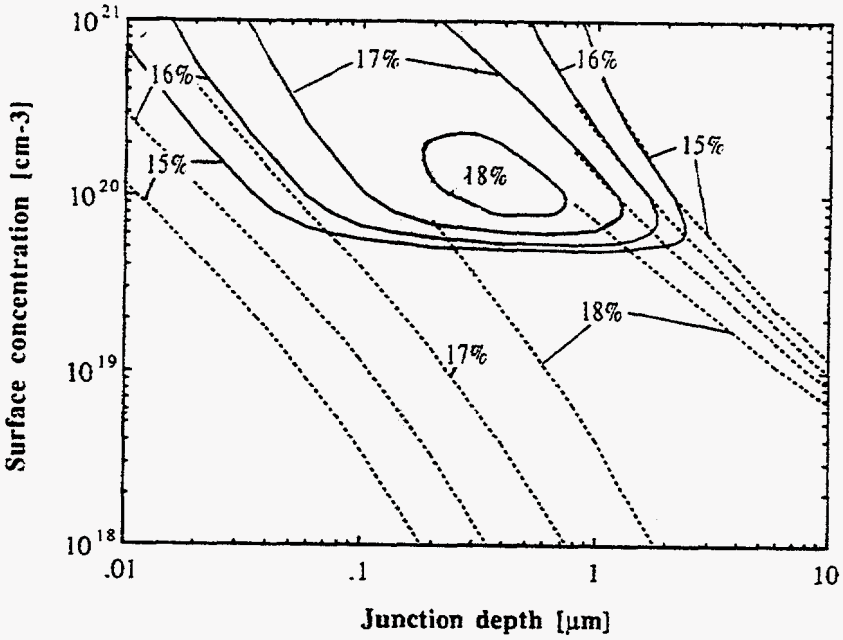

Fig.1 Contours of constant efficiency for 100 cm^2 cells with a Gaussian emitter profile and screen-printed Ag contacts taking into account resistive and geometrical factors. Solid lines: homogeneous emitter, dotted lines: selective emitter.

Unlike evaporated contacts, screen printed contact show a point-contact nature. Contact resistivities measured for screen printed silver contacts strongly depends on phosphorus surface concentration and range from 10^{-3} to 10^{-2} Ωcm^2. This is a factor of 1000 higher than the values reported for evaporated contacts.

Contours of constant optimum efficiency have been generated for 200 μm thick, 100cm^2 cells with a base doping concentration of $10^{16}cm^{-3}$ as shown in Figure 1. The measured dependence of the contact resistance and surface recombination velocity of passivating oxide on the surface concentration has been taken into account. The calculation has been performed for both uniform and selective emitters. For the latter a 1μm deep Gaussian profile with a surface concentration of $10^{21}cm^{-3}$ was assumed under the fingers.

From the results shown in Figure1 it can be concluded that for the cells with a non-selective emitter the phosphorus surface concentration should be at least $10^{20}cm^{-3}$. Due to the high contact resistivity , the fill factor decreases drastically for lower surface concentrations. Moreover, given the characteristics of screen printed metal contacts, the junction depth should be at least 0.3 -0.4 μm so as to avoid shunting of the emitter. These constraints leave only a small region in the surface–concentration/junction depth plane where near–to-maximum cell efficiency can be obtained. Small deviations from the optimum emitter profile result in a drastic changes in cell efficiency.

For cells with a selective emitter, the best efficiency is not much higher, but less sensitive to small variations in emitter surface concentration or junction depth. This lower sensitivity for deviation from the optimum processing condition can be considered as the main advantage of using a selective emitter structure for industrial cells with screen printed contacts.

The following chapter will give a critical review of the selective emitter processes developed in IMEC with screen printed metallization.

3. Selective emitter process with screen printed metallization.

3.1. Single diffusion and etch-back selective emitter process.

The first version of the etch-back selective emitter applied to solar cells with screen printed metallization had enormous difficulties with alignment of the front side metal grid with the highly doped emitter regions. Any misalignment resulted in shunting through the shallow junction between the fingers. The solution was found by reversing the order of the etch-back and metallization processes[7]. The version of this process applied to silicon multicrystalline cells is presented in Fig.2.

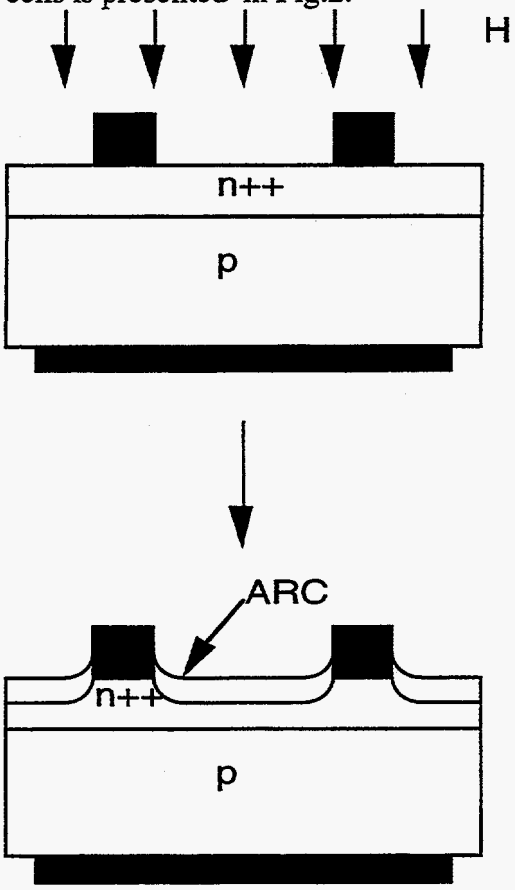

Fig. 2 Single diffusion and etch-back selective emitter including hydrogen passivation

First the heavy P-diffusion is carried out to form of a deep n++ emitter with sheet resistance typically between 10-16 Ω/sq. Parameters of the diffusion process (time and temperature) were adjusted to provide effective impurity gettering. Next the front and back contacts were screen printed and fired. After that the wafers received hydrogen plasma passivation treatment at 350°C for one hour from the emitter side. Subsequently the front and back metallization was protected by acid resistant screen printing paste. This is followed by etching-back of the emitter in an HF-HNO_3 solution to sheet resistance of 80-100 Ω/sq. Finally an antireflection coating was deposited over the whole front surface. The advantages of this process are numerous. First , the critical alignment of the silver grid with the highly doped n++ regions is avoided and replaced by an easy alignment of the protective paste to the silver fingers. Secondly, only one phosphorus diffusion step is required for forming the selectively doped emitter.

At the same time this heavy n^{++} diffusion step replaces the separate gettering step. The near-surface emitter layer damaged by hydrogen plasma is removed along with the emitter etch-back. Large area multicrystalline cells fabricated using this particular selective emitter had a short circuit current increased by 1.5 mA/cm^2 and open circuit voltage up to 9 mV higher in comparison to homogeneous emitter of 40Ω/sq.

This process has also several disadvantages. The etch-back process is carried-out in a diluted CP4 type solution. In order to have reproducible results the etch-back process was carried out wafer by wafer. Putting more wafers lead to an uncontrolled exothermic reaction. Monitoring of the sheet resistance of etched emitters can not be done in-situ. Wafers had to be taken few times out of the solution for emitter sheet resistance measurements. Prolonged hydrogen plasma treatment resulted in the peeling of screen printed contacts.
Another important weak point of this process is absence of the front surface passivation.

3.2 Double diffusion selective emitter.

The selective emitter process with two diffusion steps developed in IMEC is presented in Figure 3. This process solves the main problems of all emitter etch back processes described in the section above.
Compared to standard solar cell processes for homogeneous emitters, there are only two additional processing steps required, one printing step and one diffusion step. The removal of the deeply diffused region happens during the texturization process. In the following, the optimisation of single processing steps are described in detail.
As a first step, the saw damage is removed by etching the as-cut wafers in a concentrated solution of NaOH. The minimized cleaning prior to the diffusion consists of only a short dip in a diluted hot HCl solution. This guarantes perfect neutralisation of sodium and dissolves metallic contaminants.

Saw Damage Etching
Cleaning
Deep Diffusion $POCl_3$, (16 Ω/sq.)
Masking Paste Printing
Texturization and Selective Junction Etching
Paste Removal
Shallow Diffusion $POCl_3$ (80-100 Ω/sq.)
PECVD SiNx Deposition
Screen Printed Metallization

Fig. 3 Two diffusion and selective texturization selective emitter process.

A deep n^{++}-emitter is diffused inside a quartz tube furnace, using liquid $POCl_3$ as a doping source. The obtained sheet resistivities are in the range of 10 to 16 Ω/sq.
Thorough investigations have been undertaken on the next processing steps: selective texturing, PECVD nitride deposition and screen printed metallization.

3.2.1 Texture etch-back.

In the proposed process the texturing solution should be able not only to texture wafer surfaces but also at the same time remove completely the deep junction. We developed the new texturing composition fulfilling this task both for mono and multicrystalline wafers[8]. Figure 4 shows the SEM picture of one of the selectively texture monocrystalline wafers directly after the removing of the masking layer. After texturing, a shallow emitter optimized for a high blue response is diffused from gas phase in open tube furnace to sheet resistance of around 80 - 100 Ω/sq.

3.2.2 Passivation from firing-through PECVD SiNx ARC layers.

As already mentioned in chapter 2 surface passivation is a crucial point for shallow transparent emitters. The IMEC surface and bulk passivation process is based on the use of a hydrogen rich direct plasma deposited silicon nitride layer. This nitride layer acts not

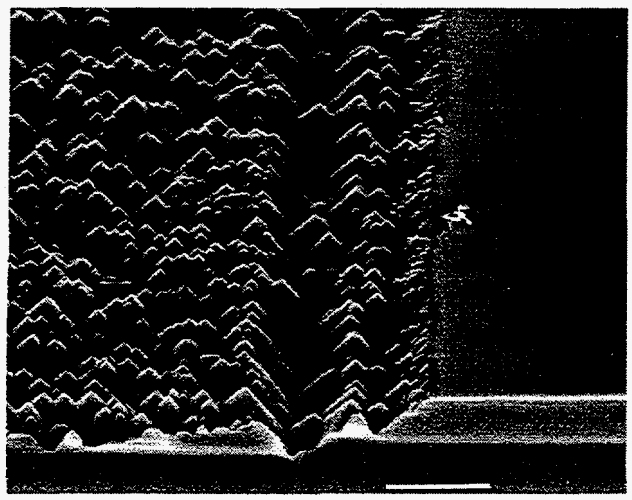

Fig.4 SEM picture of a selectively textured mono-c wafer

only as an anti-reflection coating but also serves as the source of atomic hydrogen. According to the processing sequence shown in Figure 3 the front metallization is screen printed on the top of PECVD SiNx layer and fired later together with a back contact in an IR furnace[9].

Since the front contacts are fired through the SiN_x-layer, it will be referred to as the firing-through process. The main benefits are :

- solderable contacts : contacts are directly solderable after firing, any masking or brushing off of ARC layer is not needed
- surface and bulk passivation : a thermal treatment after the deposition of silicon nitride can release hydrogen from the Si-H and N-H bonds into the cell, passivating the silicon surface and the bulk. The surface damage which is a consequence of the nitride deposition in a direct PECVD-system is annealed so that a good surface passivation is obtained.
- creation of BSF : since front (Ag) and back contact (Al) are fired together at elevated temperature, this will result in the formation of an Al-BSF on the back surface of the cell.
- the oxidation step can be removed from the process since a good surface passivation is obtained by performing the thermal treatment of the silicon nitride.

It is clear that during one step (the firing of the contacts) multiple actions take place at once. This is known as co-processing which greatly simplifies the generic process. Depending on the starting quality of the material and its response to hydrogen passivation, the firing-through nitride process brings an efficiency improvement of 0.5 % absolute (high quality material) to 2.5% absolute (more defected material, EMC, etc.)

The best results obtained with this selective emitter process are listed Table 1.

Table 1 : Best selective emitter cell results (100 cm^2, 1 Ωcm, DLARC) (* as independently confirmed by Fraunhofer ISE)

Wafer type/ texturing	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eff. (%)
Multicrystalline/Al kaline textured	34.5	624	75.9	16.3*
Multicrystalline/ Mech. text.	35.5	612	75.7	16.5*
Monocrystalline / Alkaline textured	35.6	619	78.3	17.3

3.3 Selective emitter in one diffusion step without etching or masking.

This approach does not need any additional processing step, masking or etching step as compared to uniform emitter processes[9,10]. The principle of this process is shown in Figure 4. A phosphorus paste is selectively applied to the front surface of the Si substrate by screen printing. The printed pattern is similar to the metallization pattern that has to be printed at the end of the cell processing sequence, including some tolerance in width for alignment. The phosphorus paste is subsequently dried and the substrate heated to temperatures typically above 900 ° C. Phosphorus diffuses strongly into the Si substrate where the source material was printed directly to the surface. At those areas deeply doped regions with a high phosphorus surface concentration are formed during the diffusion step. At the other surface areas phosphorus diffuses at much lower rates into the Si surface because it is only transported indirectly by out-diffusion from the source material in the gas atmosphere to those regions. Both differently doped regions are created in this simple processing sequence automatically during the same diffusion step without additional masking or etching.

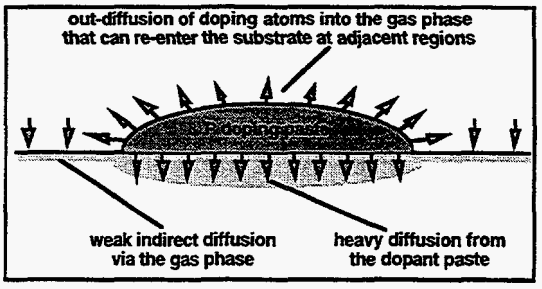

Fig. 5 Illustration of the selective diffusion principle

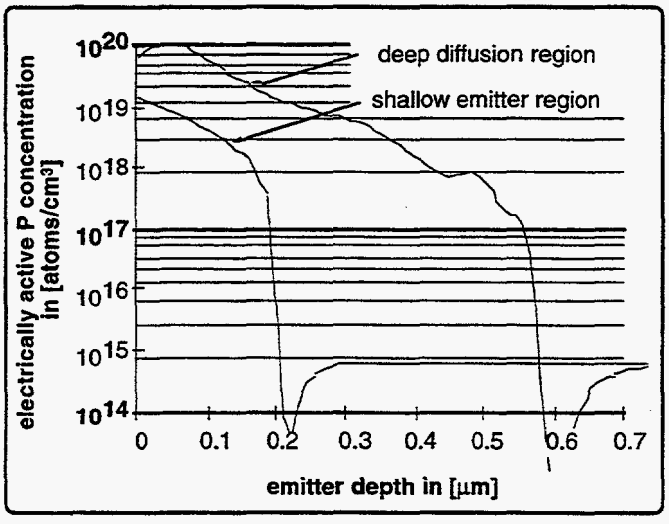

Fig. 6 SRP depth profiles of the electrically active P concentration on the place of highest and lowest emitter resistance

The spreading resistance depth profiles shown in Figure 6 prove that the proposed simple method is able to produce a selective emitter in only one diffusion step. The deeply diffused regions with a high surface concentration are present at those areas onto which screen printed metallization is applied later in the processing sequence. At the same time the shallow emitter regions with a low surface concentration are formed elsewhere.
A shallow and weakly doped emitter asks for good passivation of the front surface and the front contact grid has to be perfectly align on the invisible highly doped areas. The first problem is solved by applying a PECVD SiNx ARC layer in combination with a firing-through process described above. The printer equipped with digital camera takes care of printing of the front grid exactly on the top of highly doped areas.
The best cell results obtained so far were achieved using a processing sequence comprising alkaline saw damage removal and texturization, the selective diffusion step from P paste, a very short thermal oxidation (800° C, 1 min.), a PECVD SiN_x deposition (single ARC) and a screen printed metallization sequence in which front and rear contacts are fired at the same time. This sequence has proven to result in good passivation of front and rear surface (in situ Al back surface field formation during metallization firing). The best cell result is listed below in Table 2.
The same process applied to high resistivity Cz wafers resulted in short circuit current of 38

mA/cm^2, a surprisingly high current for a simple screen printing cell process. The IQE curves shown in Figure 7 explains this large current increase by the excellent cell blue response.

Table 2: Best solar cell result on 10 x 10 cm^2 Cz Si

firing through oxide & Si nitride	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eff. (%)
0.5-2 Ohm cm Cz Si	36.9	628	78	18.0

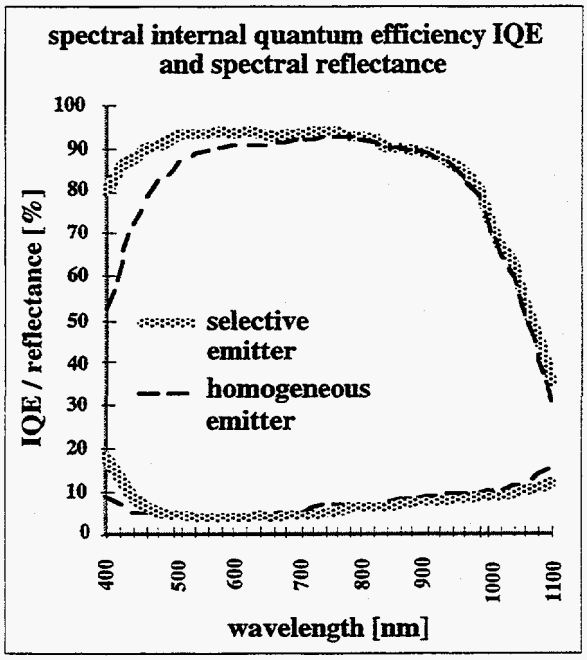

Figure 7 : Improved spectral response of screen printed selective emitter solar cells

Lack of tan impuritiy gettering step, present in the previous selective emitter processes, makes this process mainly suitable for good quality substrates which do not require extensive P-gettering. However, the same process applied to large area multicrystalline wafers produced cells with the efficiencies above 16 %.

The only obstacle in the implementation of this selective emitter process into solar cell production lines is the reproducibilty problem of the cell fill factor. After hundreds of printing cycles the screens might be mechanically deformed and the alignment of the diffusion pattern with the metallization pattern becomes problematic leading to large variation in the cell fill factors. The latest development in the stencil screens gives hope that the durable screens without deformation after few thousands of the printing cycles will be soon commercially available[11].

4. Summary.

It has been proved long time ago by the theory and laboratory work that the selective emitters in combination with good surface passivation can significantly improve the cell efficiency. The Laser Grooved Buried Contact cell is an example of transferring the selective emitter concept into production lines. This paper describes the evolution of the selective emitter process in combination with screen printed contacts. The introduction of screen printers with optical alignment, good surface passivation by means of PECVD SiNx layers and development of advanced pastes able to provide a low contact resistance even when fired through passivating layers, triggered-off the significant progress in the commercially promising selective emitter processes based on screen printed metallization. The most promising seems to be the selective emitter process based on the auto-doping from selectively printed P-paste. In combination with a good surface and bulk passivation process by means of the firing-through PECVD SiNx , the efficiency in the range of 18% on Cz-Si and above 16% on multi-Si large area wafers have been obtained. The basic advantage of this selective emitter process is that the processing sequence requires no any additional processing step with reference to a homogeneous emitter process.

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PECVD DEPOSITION OF SILICON NITRIDE: FUNDAMENTALS AND PROSPECTS FOR INDUSTRIAL APPLICATION

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Abstract: The plasma-enhanced chemical vapor deposition (PECVD) of silicon nitride (SiN_x) is of enormous interest for the silicon photovoltaic (PV) community as it offers the possibility to fabricate a surface and bulk passivating antireflection coating at low temperature. In this paper, the fundamentals of the PECVD technology and the resulting SiN_x films and Si-SiN_x interfaces are discussed. Furthermore, the prospects of the PECVD method for application in the PV industry are evaluated.

1. INTRODUCTION

One of the most important manufacturing steps of Si solar cells is the cost-effective fabrication of an antireflection (AR) coating. Ideally, this coating should not only reduce optical losses but simultaneously provide a reasonable degree of surface passivation and, in the case of multicrystalline (mc) Si material, a hydrogen passivation of bulk defects and/or grain boundaries. During the last decade it has become increasingly clear that the most promising candidate for the achievement of these vastly differing tasks is *silicon nitride* generated at low temperature (300 - 450 °C) by means of the PECVD technique [1 - 8]. These plasma silicon nitride films (a-SiN_x:H, abbreviated 'SiN_x') act as a *surface (and bulk) passivating AR coating*, a unique combination that is not met by the standard coatings* on Si solar cells.

2. FUNDAMENTALS OF THE PECVD DEPOSITION OF SILICON NITRIDE

2.1 Direct PECVD

Chemical, mechanical, electrical and optical properties of silicon nitride films strongly depend on the preparation method and the particular processing parameters. *Stoichiometric* amorphous silicon nitride (a-Si_3N_4) films can be made by direct nitration of silicon, nitrogen ion implantation into silicon, or sputtering of silicon in a nitrogen-containing ambient [9]. However, because these methods are either limited to very thin (< 10 nm) films or produce a strongly damaged silicon/silicon nitride interface, the most common preparation method is to grow amorphous silicon nitride films from the gas phase by means of *chemical vapor deposition* (CVD). In general these methods use hydrogen-containing reactants, resulting in *non-stoichiometric* silicon nitride films with up to 40 atomic % of hydrogen. The three basic CVD processes are the reaction of silane and ammonia at atmospheric pressure and temperatures in the 700 - 1000 °C range (APCVD), the reaction of dichlorosilane and ammonia at reduced pressure (~ 0.1 mbar) and temperatures around 750 °C (LPCVD), and the plasma-enhanced reaction of silane and ammonia (and, optionally, nitrogen) mixtures at reduced pressure (~ 1 mbar) and temperatures below 500 °C (PECVD). Especially the PECVD method [10] is of great interest for the semiconductor industry because it allows the fabrication of silicon nitride at *low* temperature. This is an important advantage for many applications, considering problems such as carrier lifetime degradation, throughput, or degradation of metal contact schemes.

The standard PECVD deposition method for SiN_x is characterized by the use of the *direct* plasma excitation approach in so-called direct-plasma reactors (sometimes also called parallel-plate reactors), where the processing gases are excited by an electromagnetic field and where the wafers are located *within* the plasma.

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* Thermal SiO_2 or TiO_x fabricated by atmospheric pressure CVD. Both of these materials don't contain the required hydrogen for the bulk passivation effect in mc silicon wafers. Furthermore, the refractive index of SiO_2 (1.46) is too small for optimal AR performance, while TiO_x provides no electronic surface passivation.

The electromagnetic field has a frequency of either 13.56 MHz ('high-frequency' method) or in the 10 - 500 kHz range ('low-frequency' method). Fig. 1(a) shows a cross-sectional view of such a direct-plasma reactor. Typical processing parameters for the case of a laboratory-type (i.e. single-wafer) reactor with a table diameter of ~ 20 cm are a plasma power of 100 mW/cm^2, a total gas flow of 50 sccm, and a SiH_4/NH_3 flow ratio of 10 - 50 %. In order to enhance the throughput, the industry uses so-called *batch reactors* [see Fig. 2(b)] instead of single-wafer reactors. These machines feature an array („boat") of disc-like metal plates (∅ ~ 20 cm, spacing ~ 2 cm), enabling the simultaneous processing of more than hundred Si wafers. Several direct-plasma batch reactors are presently in use in the silicon PV industry.

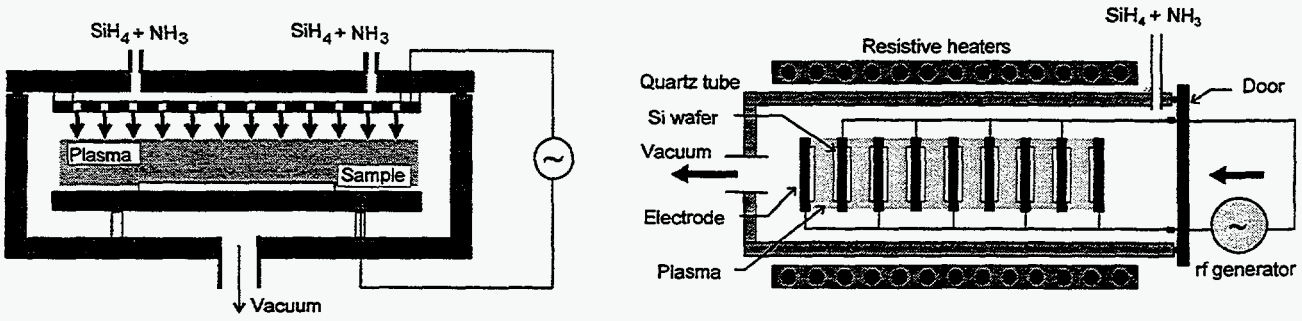

Fig. 1 (a) The standard PECVD SiN_x deposition in a laboratory-type direct-plasma reactor. Note that *both* processing gases (SiH_4 and NH_3) are excited by the electromagnetic field and that the wafer is located *within* the plasma excitation volume. (b) Direct-plasma *batch* reactor for the simultaneous PECVD deposition of SiN_x onto many silicon wafers.

The plasma excitation frequency has a strong impact on the electronic properties of the resulting Si-SiN_x interfaces. The reason is that below the so-called *plasma frequency* (~ 4 MHz) ions are able to follow the plasma excitation frequency and therefore produce a strong surface bombardment. Due to the resulting surface damage, SiN_x films fabricated with *low-frequency* direct PECVD only provide an intermediate-quality surface passivation on Si surfaces [8]. Furthermore, the surface passivation is not stable against the UV photons of sunlight [8]. Fortunately, this problem can be largely eliminated as for plasma excitation frequencies *above* 4 MHz the acceleration periods are too short for the ions to absorb a significant amount of energy. Hence, SiN_x films prepared by direct PECVD at high frequency (13.56 MHz) provide a much better surface passivation and a much better UV stability than SiN_x films prepared at low frequency (10 - 500 kHz) [11].

However, in spite of the industrial success that the direct-plasma batch method has already achieved, this method has a number of major drawbacks and technical limitations with regard to the *low-cost* mass production of SiN_x coatings on Si solar cells. These problems include [12]:

- In order to achieve a satisfactory throughput, industrial batch reactors use several 'boats' at a time: one being loaded with wafers, one being processed in the tube, one cooling down in a parking position, and another one being unloaded. This requires a complicated (and hence expensive) boat handling system.
- The loading of the fragile Si wafers into the boats is rather slow and complicated because (i) many different positions have to be served and (ii) the spacing between the plate electrodes is very narrow (~ 2 cm). This requires several complicated (and hence expensive) wafer handling systems (robots). The costs of the wafer and boat handling systems may exceed 50 % of the costs of the total PECVD system.
- In direct-plasma systems not only the Si wafers but also the walls of the quartz tube are covered with SiN_x (*non-directional* film deposition). After a relatively small number of depositions the SiN_x must be removed from the quartz tube. This removal is a rather slow process involving expensive and environmentally hazardous etching gases (CFCs).
- Due to the large thermal mass of the boats, there is a significant time period (~ 15 min) which has to elapse until the temperature required for the SiN_x deposition has stabilized across the entire boat. As the SiN_x

deposition lasts only ~ 5 min, this delay reduces the energy efficiency and the throughput of batch systems.

- In direct-plasma reactors there must be good electrical contact between the wafers and the electrodes. This point becomes increasingly difficult with evolving ribbon-grown Si wafers featuring corrugated surfaces.
- Upscaling to very large wafers (> 200 cm^2) is difficult because a homogeneous gas distribution must be ensured across the entire wafer surface and across the entire boat. In particular the uniformity of the SiN_x film properties across the entire boat represents a challenge because, depending on the degree of electrical contact between wafers and electrodes, the local power coupled into the plasma is not uniform.

For all these reasons, it is not surprising that the costs of the SiN_x deposition onto Si wafers with today's industrial direct-plasma batch reactors are relatively high (~ 0.15 US-$/$W_p$ [12]). Although the throughput is satisfactory, the above-mentioned technical problems indicate that this technique (i) does not offer sufficient room for the required cost reductions in PV applications and (ii) is not well suited for the processing of evolving photovoltaic Si materials (e.g., ribbon-grown wafers or very-large-area wafers). A very promising alternative with regard to these problems is the so-called *remote* (or *downstream*) PECVD method.

2.2 Remote PECVD

In the *direct-plasma* technique, both processing gases (SiH_4 and NH_3) are excited by the rf field and the wafer is located *within* the plasma (see Fig. 1). This reactor design leads to a *non-directional* film deposition which causes the above-mentioned problems with the parasitic SiN_x deposition onto the walls of the vacuum chamber. As can be seen from Fig. 2(a), the situation is very different in the *remote-plasma* technique. Here, the excitation of the plasma occurs *outside* the vacuum chamber and the excited species (note that only NH_3 is excited while SiH_4 is injected downstream) are directed onto the wafer by means of a narrow quartz tube. The resulting *directional* SiN_x deposition, in combination with the plasma excitation by microwaves instead of an rf field, greatly improves the speed and the economy of the deposition process while at the same time allowing the deposition of SiN_x films with virtually no surface damage of the samples. Considering the long list of technical problems and limitations of direct PECVD (see Section 2.1), it is worthwhile to investigate the advantages of remote PECVD over direct PECVD with regard to the economic mass production of SiN_x coatings on Si solar cells. These include [12]:

- With innovative plasma sources, very high plasma densities and a directional film deposition can be obtained. The resulting very high film growth rates (up to several hundred Å/s !) lead to very short processing times, which make it possible to use a fast *in-line reactor* as opposed to conventional batch reactors.
- Compared to batch systems, wafer handling in in-line systems is much easier, strongly reducing the costs of the entire system.
- No electrical contact between the wafer and the wafer holder is required in remote PECVD, allowing the use of wafers with arbitrary shape and surface roughness. This is an important point for evolving Si materials such as ribbon-grown wafers.
- Due to the simple wafer handling system and the fact that no electrical contact between wafer and wafer holder is required, the thickness of the Si wafers can be reduced to below 200 µm without sacrifices in the production yield. As the Si wafer presently causes 60 - 80 % of the total costs of the solar cell, a significant reduction (~ 15 %) of the cell costs becomes feasible.
- An upscaling to very large wafers (> 200 cm^2) can easily be realized.
- Due to the directional nature of remote PECVD, the parasitic SiN_x deposition onto the walls of the vacuum chamber is strongly reduced.
- Most industrial PECVD batch systems use *low-frequency* excitation due to technical difficulties in obtaining uniform SiN_x film properties across the entire boat with *high-frequency* excitation. Because of the uniformity problems of high-frequency direct-plasma SiN_x films and the passivation quality and UV stability problems of low-frequency direct-plasma SiN_x films, remote PECVD is the preferred option.

For all the reasons mentioned above, research is presently on the way at ISFH to evaluate if the present expensive SiN_x process based on direct-plasma batch PECVD systems can be replaced by a low-tech remote-plasma

in-line approach enabling the fast and economic SiN_x deposition onto moving Si wafers [12]. Preliminary studies at ISFH point towards an innovative in-line remote PECVD machine which is well suited for mass production and which is applicable to Si materials of arbitrary shape, surface roughness, and thickness. Fig. 2(b) shows a possible lay-out [12] of such an in-line machine which is expected to be able to process ~ 600 Si wafers per hour and to reduce the costs of the SiN_x deposition process by ~ 50%.

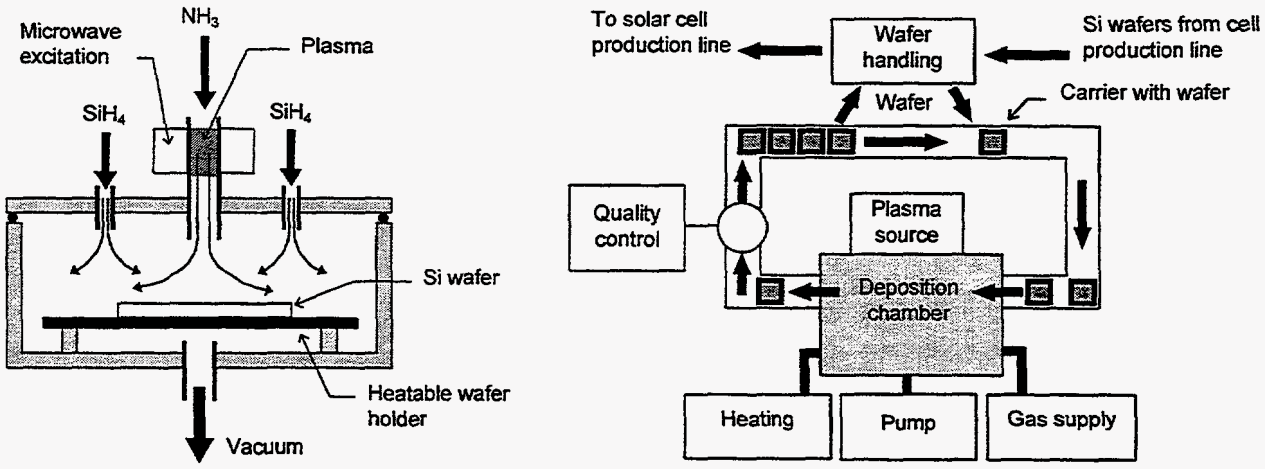

Fig. 2 (a) Laboratory-type *remote* PECVD system for the low-temperature deposition of SiN_x onto single Si wafers. Note that only ammonia is excited by microwaves and that the wafer is located *outside* the plasma excitation volume. (b) Possible lay-out of an *in-line* remote PECVD machine for the low-cost mass production of SiN_x coatings on Si solar cells.

3. FUNDAMENTAL PROPERTIES OF SiN_x FILMS AND Si-SiN_x INTERFACES

3.1 SiN_x films

Crystalline Si_3N_4 occurs in 2 forms, α and ß, containing 14 and 28 atoms per unit cell [13]. The bonding in both forms is predominantly covalent, with silicon being tetrahedrally coordinated by nitrogen atoms and nitrogen being threefold coordinated in a near-planar configuration. *Amorphous* silicon nitride prepared by CVD at high temperature (~ 1000 °C) in a large NH_3 excess can be considered as a reference material because it is essentially stoichiometric and contains very little hydrogen. The electronic structure of *stoichiometric* amorphous silicon nitride (a-Si_3N_4) and the most important defects in this material have been calculated [14]. The bandgap is predicted to be ~ 5.3 eV. Defects in a chemically ordered network such as Si_3N_4 can be defined as the Si—Si and N—N like-atom bonds and the Si and N dangling bonds. Vacancies are not expected. The calculations indicate that the main defects in a-Si_3N_4 are the *Si and N dangling bonds*. The dangling bond of a trivalent Si site (≡Si•) is calculated to form a localized, roughly sp^3 hybridized state near midgap, about 3.1 eV above E_v [13]. This state is singly occupied for a neutral site and hence paramagnetic. The N dangling bond defect (=N•) forms a highly localized $p\pi$ level just above E_v. This state is also singly occupied for a neutral site. Another paramagnetic defect center consists of a N dangling bond which is, via a N—N bond, bonded to another N atom. The Si—Si bond is predicted to form a σ state close to E_v and a σ* state close to E_c .

By means of ESR experiments it has been confirmed that the Si dangling bond is the dominant defect both in stoichiometric amorphous silicon nitride and in silicon-rich hydrogenated amorphous silicon nitride (SiN_x) with $x < 1.1$ [15 - 20]. The total Si dangling bond density was found to be quite high compared to that in a-Si:H. These experiments furthermore showed that the Si atoms with a nonpaired electron are predominantly back-bonded to three N atoms in stoichiometric and N-rich SiN_x films [21]. In the literature, this specific Si

dangling bond defect $N_3{\equiv}Si\bullet$ is termed the *K center* [21]. The K center was found to be most stable in its charged diamagnetic configurations (K^+, K^-). In Si-rich SiN_x films, in addition to the K center, Si dangling bond defects with three other back bond configurations ($Si_3{\equiv}Si\bullet$, $Si_2N{\equiv}Si\bullet$, $SiN_2{\equiv}Si\bullet$) have been identified with ESR measurements [22].

With increasing Si content both the valence band and the conduction band of SiN_x move towards midgap, decreasing the bandgap. This trend continues until the bandgap of hydrogenated amorphous Si (~ 1.7 eV) is approached. Experiments as well as calculations indicate that the energy level of the Si dangling bond defect remains near midgap, regardless of the N/Si ratio. Hence, the Si dangling bond defect is the fundamental 'deep' defect in amorphous silicon nitride. The N dangling bond produces an energy level just above E_v in N-rich SiN_x films, which disappears into the valence band in Si-rich films. There is a clear difference between the behaviour of Si-rich and N-rich SiN_x films. The dividing composition appears to be $x = 1.1$ (not 1.33 !), the percolation threshold for Si—Si bonds in a SiN_x network [14]:

- In Si-rich films, only the Si dangling bond is found and its density is controlled by equilibrium with weak Si—Si bonds, which form the band edge states ('tail states'). As mentioned above, in addition to the K center, there are other Si dangling bond defects exhibiting 1 - 3 Si back bonds.
- In N-rich films, both Si and N dangling bonds exist. The dominant Si dangling bond defect is the K center.

Of major importance for MNOS memory devices are specific defects in the bulk of the SiN_x films whose charge state can be controlled by means of an electric field or UV illumination. Fujita and Sasaki [15] and Krick *et al.* [16, 17] demonstrated with ESR measurements that the K center is the defect responsible for the charge storage mechanism. This conclusion was found to apply to stoichiometric, Si-rich, as well as N-rich SiN_x, regardless of the fabrication method of the SiN_x film. A key property of the K center is the fact that UV illumination is required to render it ESR active (i.e., paramagnetic). It has been suggested that this behavior is possibly due to a negative correlation energy of the K center [19, 20]. In this model, the charged diamagnetic states (K^+, K^-) are more stable than the paramagnetic neutral state (K^0). Hence, the positively and negatively charged diamagnetic Si dangling bond defects K^+ and K^- are traps for electrons and holes, respectively. During UV illumination ($h\nu > 3.5$ eV), the charged K^+ and K^- centers are converted into metastable neutral K^0 centers which can be detected by ESR.

3.2 Si-SiN_x interfaces

Fig. 3 shows the simplified energy band diagram of the Si-SiN_x interface [23]. Between the Si wafer and the bulk of the SiN_x film there exists a very thin oxynitride film. This SiN_xO_y film is due to the specific experimental conditions of PECVD: in the time period between the loading of the Si wafers into the deposition chamber and the start of the SiN_x deposition (i.e., the ignition of the plasma), a thin SiO_x film (< 2 nm) grows on the Si surface. During the SiN_x deposition, this SiO_x film is converted into an oxynitride film. The existence of a thin interfacial oxynitride film at Si-SiN_x interfaces is experimentally well confirmed [24]. Hence, the actual interfacial region on Si wafers covered by a PECVD SiN_x film is rather similar to the one found at the thermally grown Si-SiO_2 interface. At the latter interface, the interface states are caused by *Si dangling bond defects* in the thin, nonstoichiometric interfacial suboxide layer. Due to the presence of N and O atoms, the interface states at Si-SiN_x interfaces are Si dangling bond defects back bonded with Si, N, and/or O atoms.

Key parameters of semiconductor-insulator interfaces are the interface state density D_{it}, the trapped charge Q_{it} within the interface states, and the insulator charge Q_f. At thermally grown Si-SiO_2 interfaces the positive oxide charge is due to the Si dangling bond defect with 3 oxygen back bonds („P_{ox}" defect) [25]. This defect also exists at the Si-SiN_x interface and causes, together with the P_{ox}-like defects $O_2N{\equiv}Si\bullet$ and $ON_2{\equiv}Si\bullet$, a similar fixed positive insulator charge (~ $1{\times}10^{11}$ cm^{-2}) as at the thermal Si-SiO_2 interface. However, as shown in Ref. 23, there is another contribution to the positive insulator charge which is *not* constant but depends strongly on the electron and hole concentration at the Si surface. This variable positive insulator charge is due to the K^+ center shown in Fig. 3.

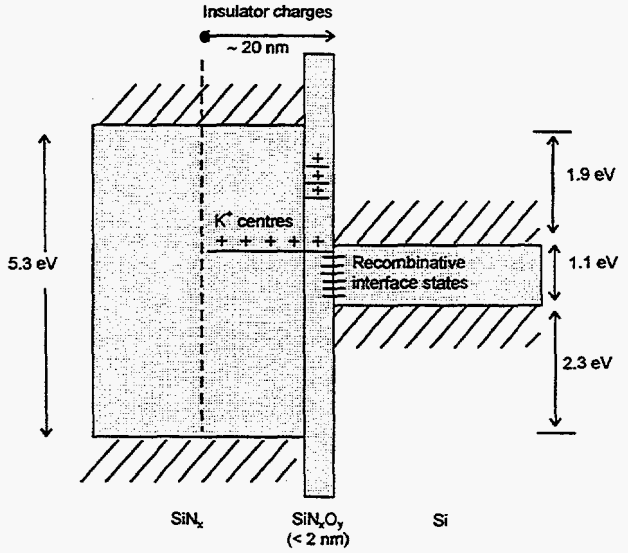

Fig. 3 Simplified energy band diagram of the Si-SiN_x interface (band bending not shown). Note that the positive insulator charge Q_f consists of two components, namely a constant contribution from the P_{ox}-like defects in the interfacial SiN_xO_y film and an operating condition dependent contribution from the charged K^+ centers within an ~ 20 nm wide section of the SiN_x film.

4. OPTICAL AND ELECTRONIC PERFORMANCE OF SiN_x FILMS

With regard to Si solar cell applications, the low-temperature deposited remote-plasma and high-frequency direct-plasma SiN_x films optimized at ISFH possess several important properties. These include (i) good surface passivation on phosphorus-diffused emitters [8, 26], (ii) outstanding surface passivation on low-resistivity Si wafers [8, 27], (iii) an excellent reduction of reflection losses [28], (iv) a very effective hydrogen passivation of bulk defects and grain boundaries in mc silicon after a post-deposition anneal [29], and (v) the compatibility with simple screen-printing methods for the fabrication of the cell electrodes [30, 31].

For each PECVD technique, the wafer temperature during the SiN_x deposition was found to have a very strong impact on the effective carrier lifetime τ_{eff} of the samples. Interestingly, regardless of the deposition method, the optimum deposition temperature is in the range 350 - 450 °C. For the investigation of the impact of the remaining most important deposition parameters (pressure, gas mixture, gas flow and plasma power), we used *design-of-experiments* methods, performing central composite experiments (see Ref. 32 for details on the optimisation of remote-plasma SiN_x films on non-diffused *p*-Si wafers). As a most remarkable result for SiN_x films deposited by high-frequency (HF) direct PECVD or remote PECVD, the impact of all deposition parameters on the refractive index n is very similar to the impact on τ_{eff} ! This can be seen from Fig. 4, which shows a plot of τ_{eff} of SiN_x passivated *p*-type Si wafers versus the refractive index of the SiN_x films [11]. For HF direct and remote SiN_x films τ_{eff} increases up to an refractive index of about 2.3, while for the SiN_x films with higher refractive index τ_{eff} saturates at an excellent value of about 1000 µs. As shown in Ref. 27, these τ_{eff} values correspond to record-low surface recombination velocities of 4 cm/s on 1.5-Ωcm *p*-silicon. Technologically, a very important finding is the fact that the observed correlation between τ_{eff} and n is about the same for the two distinctly different deposition techniques. Although we do need different deposition parameters in the two reactors to achieve a refractive index of ~ 2.3, the resulting surface passivation is identical. This allows a fast and easy control of the passivation quality simply by measuring the refractive index of the SiN_x films. The optimal refractive index above 2.3 indicates that *Si-rich* SiN_x films ($x \leq 0.7$) are required for an excellent passivation of *p*-silicon surfaces. For SiN_x films deposited by LF direct PECVD, this strong correlation does not exist. Independent of the refractive index, the LF SiN_x films provide a relatively poor effective lifetime (see Fig. 4). The most likely reason for this behaviour is the ion bombardment during the initial stage of the SiN_x deposition. This damages the surface of the Si wafer (i.e., increases D_{it}) and therefore the passivation quality becomes dominated by this damage.

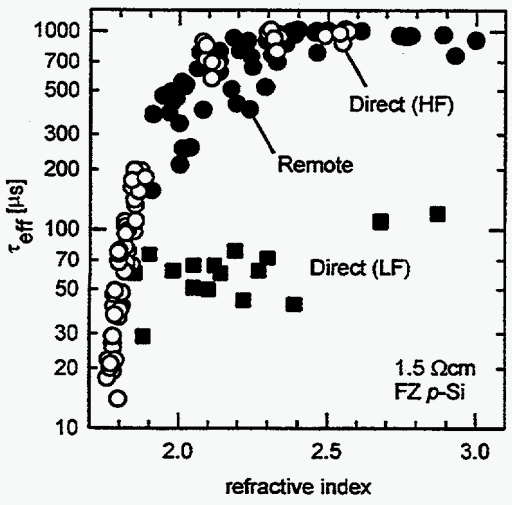

Fig. 4 Measured effective carrier lifetime of SiN_x-passivated planar 1.5-Ωcm FZ *p*-Si wafers as a function of the refractive index of SiN_x films prepared by LF direct PECVD, HF direct PECVD, and remote PECVD. The deposition temperature of all SiN_x films was about 375 °C.

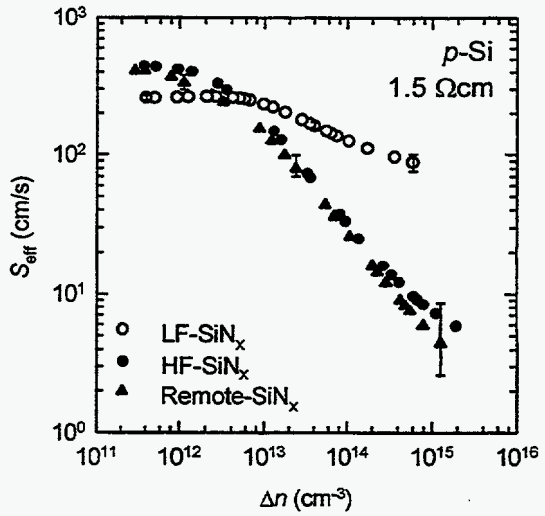

Fig. 5 Measured $S_{eff}(\Delta n)$ dependence at the surfaces of 1.5-Ωcm FZ *p*-Si wafers passivated with SiN_x films fabricated with low-frequency (100 kHz) direct PECVD, high-frequency (13.56 MHz) direct PECVD, and remote PECVD. All SiN_x films have a refractive index of ~ 2.3.

Significant information on the properties of Si-SiN_x interfaces can be obtained by measuring and simulating the injection level dependence of the effective surface recombination velocity S_{eff} of SiN_x passivated Si wafers [23, 33]. As an example, Fig. 5 shows the $S_{eff}(\Delta n)$ dependence measured at the SiN_x-passivated surfaces of three 1.5-Ωcm FZ *p*-Si wafers. The SiN_x films were fabricated with 3 different PECVD methods: low-frequency (100 kHz) direct PECVD, high-frequency (13.56 MHz) direct PECVD, and remote PECVD. All SiN_x films have a refractive index of ~ 2.3. The LF-SiN_x passivated wafer received a forming gas anneal (500 °C, 15 min) prior to the lifetime measurements in order to improve S_{eff}. It can be seen that at low injection levels all three types of SiN_x film provide about the same degree of surface passivation. With increasing injection level S_{eff} improves for all three SiN_x films, however, the improvement is much less pronounced for the LF SiN_x film. With DLTS measurements we detected three different types of defects (labeled A, B, and C) at Si-SiN_x interfaces fabricated with low-frequency direct PECVD [34]. These three defects exhibit strongly differing electron and hole capture cross section [34]. Based on the results of these DLTS measurements, we performed a theoretical analysis of the measured $S_{eff}(\Delta n)$ dependence at LF-SiN_x passivated Si surfaces. This analysis showed that defect C clearly dominates the recombination rate at such interfaces. As remote-plasma and high-frequency direct plasma SiN_x films provide a much better surface passivation at injection levels > 10^{13} cm^{-3}, we conclude that defect C is effectively suppressed at such interfaces. Hence, we suggest that defect C is caused by the ion bombardment occurring in low-frequency direct PECVD, while the 'fundamental' defects at Si-SiN_x interfaces are Si dangling bond defects as in the case of thermally grown Si-SiO_2 interfaces. It should be noted that the main reason why SiN_x films made by low-frequency direct PECVD provide a poorer surface passivation than SiN_x films made by high-frequency direct PECVD or remote PECVD are differences in the capture cross sections of the dominant defects and *not* differences in the interface state density or the positive insulator charge.

Acknowledgments

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PECVD Silicon Nitride: commercially compatible process for solar cell fabrication

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Silicon Nitride (SiNx) has a variety of applications in the electronics industry for passivation layer in IC devices, diffusion barrier and as a gate dielectric in an amorphous silicon thin film transistor (TFT) for use in active matrix liquid crystal displays (AMLCD).

In this paper, we provide a brief review of the PECVD (plasma enhanced chemical vapor deposition) technique for the deposition of SiNx layers, especially as a gate dielectric layer in a TFT which requires that the films be primarily N-rich as this leads to a dielectric with a low interface state density (in the range of 10^{10}10-10^{11} $cm^{-2}eV^{-1}$) and a high breakdown electric field strength (>5MV/cm). Its use as an antireflection coating (ARC) and as a passivation layer, has shown that there can be a significant enhancement of the conversion efficiency in multi-crystalline solar cells; in this application, in contrast to its application in the TFT structure, Si rich a-SiNx films are perhaps more ideally suited.

SiNx layers for TFT applications, as is the case in amorphous silicon technology, are routinely produced in large-scale PECVD systems. We discuss a simpler design, which would be more useful for high throughput wafer processing for ARC application.

The cost of production is an issue in the solar cell technology. For the SiNx layer step, the cost would be dictated by the gas utilization rate and by the deposition rate. A technique that we consider uses a pulsed PECVD technique as this can increase the deposition rate and is amenable for implementation for mass production.

RECENT PROGRESS IN RAPID THERMAL PROCESSING OF SILICON PHOTOVOLTAIC DEVICES

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1. Introduction

Rapid thermal processing (RTP), based upon radiatively heating silicon by incoherent optical illumination, holds the promise for revolutionizing the way solar cells are fabricated. Over the last few years RTP has emerged as a promising technology for greatly enhancing the rate of all high temperature steps utilized in solar cell fabrication. Unlike resistive furnaces, RTP utilizes tungsten-halogen lamps to heat silicon by direct radiation. Fig. 1 shows that many groups [1,2,3,4,5,6] have been successful in implementing RTP to achieve high-efficiency cells. This paper will highlight the recent progress in optimizing RTP for silicon PV not only for faster processing but also for superior device performance. Specifically, we will show how RTP has been applied for rapid and improved emitter diffusion, BSF formation, and effective front and back dielectric surface passivation. Integration of these steps so far has produced > 19%-efficient RTP cells using photolithography. Finally, we will discuss the transition to high throughput, continuous beltline RTP integrated with screen-printing and PECVD to establish a commercially viable process.

2. Rapid Emitter Diffusion and BSF Formation

In contrast to resistive furnaces, RTP utilizes tungsten-halogen and in some cases UV lamps to heat silicon by direct radiation. This differs fundamentally from conventional furnace processing (CFP) in two ways. First, the spectrum of electromagnetic energy impinging the wafers contains higher energy (shorter wavelength) photons in RTP. This is because the tungsten filament temperature in the lamps are brought to 2,000-3000°C resulting in the emission of a considerable amount of energy in the visible (and some UV) spectrum as dictated by Planck's radiation law (see Fig. 2). Furnaces heat a large thermal mass (wafers, gases, quartz tubing, etc.) to an equilibrium processing temperature (only 800-1,000°C) therefore resulting in only low energy far IR photons. Second, RTP systems are capable of heating and cooling wafers extremely rapidly, on the order of 100°C/s. As will be shown, these attributes enhance not only the kinetics of semiconductor processes but also the final performance of PV devices.

2.1 Enhanced Phosphorus Diffusion by RTP

Several researchers have observed the enhanced diffusion capabilities of RTP. Researchers at CNRS [7] showed several comparisons between RTP and CFP, which clearly indicate much greater diffusion of P in Si by RTP. Fig. 4 shows the evolution of sheet resistance vs. temperature for 25 sec RTP diffusions and 15 min CFP diffusions. Despite the more than 30 times greater diffusion time for CFP, RTP gave more diffusion than CFP for temperatures below 950°C. Singh's RTP diffusion studies showed a considerable difference in the rate of P diffusion in Si with and without light [8]. For example, the experimental setup in Fig. 5 illustrates that high-energy visible photons are incident on the P-glass/Si interface only for the front irradiation case, whereas only the weakly absorbed IR light that transmits through the calibration and sample wafers is available for back irradiation. Fig. 6 shows that about a factor of 3 times lower sheet resistance results from the front irradiation case. He explains the enhanced diffusion is due to photophysical effects that significantly lower the activation energy for semiconductor processes thus lowering the temperature and time required.

Our own experiments show a significant enhancement by RTP diffusion compared with CFP diffusion. Fig. 3 shows the resulting SIMS profiles of diffusions done under identical temperature, time, and phosphorus source conditions in the conventional furnace and an RTP system. The thermal cycle involved 880°C for 10 min diffusion using a phosphorus spin-on source with a concentration of 10^{20} cm^{-3} from Emulsitone, Co. The RTP sample gave a much lower sheet resistance of 28 Ω/□ compared with 100 Ω/□ for the CFP sample. The CFP temperature had to be increased to 930°C (for 10 min.), to achieve a comparable sheet resistance to that of the RTP diffusion (34 Ω/□). In addition to shorter processing time, RTP allows simultaneous front and back junction formation or BSF and front oxidation without cross-contamination due to cold-wall processing.

2.2 Rapid and Improved Aluminum Alloyed BSF by RTP of Screen-Printed Aluminum

Simultaneously with the emitter diffusion or with the growth of a passivating RTO, an Al BSF can be formed rapidly and effectively. This not only allows the entire cell structure to be formed in seconds or minutes, but also results in better performance. We have found that the faster ramp rate possible only in RTP results in uniform melting of Al and the formation of a more uniform Al-Si alloy, or p^+ BSF. This is clearly shown in the SEM pictures shown in Fig. 10. The furnace-alloyed Al BSF took about 1-2 hours with a 5°C/min ramp, while the RTP-alloyed BSF was formed in just 2 min with a heating rate of 1200°C/min. RTP-alloying results in a significantly more effective BSF that reduces the spatially-averaged effective back surface recombination velocity (S_{back}). This is important because although deep Al BSF profiles are well documented in the past [9], only recently, has it been shown to result in S_{back} values as low as 200 cm/s on a device [10]. A slow ramp rate results in local wetting and produces a nonuniform BSF that may have regions where there is virtually no BSF (Fig. 10) therefore increasing the spatially-averaged S_{back}. Long-wavelength analysis of the IQE of 2 Ω-cm FZ Si cells reveals a substantial reduction in S_{back} from 1,000 for the slow-ramped, furnace-alloyed BSF to 200 cm/s for the fast-ramped, RTP-alloyed BSF (see Fig. 9). Next, we replaced evaporated Al by screen-printed Al to make the process more rapid and manufacturable. The final SEM picture in Fig. 10 shows that the combination of low-cost, screen-printed Al and RTP-alloying results in the deepest Al BSF. This BSF was found to increase V_{oc} by 10 mV compared with cells with a furnace-alloyed BSF and by about 20 mV compared with cells with no BSF. Thus, the RTP-alloyed screen-printed Al-BSF is not only formed faster but is also more effective than a CFP-alloyed BSF.

2.3 Preservation of Bulk Lifetime and Gettering during RTP

Inherent to RTP is the rapid heating and cooling rates experienced by the silicon wafers. This can be detrimental to bulk lifetime because impurities can be frozen into electrically active sites upon quenching. To mitigate these problems we engineered a short *in-situ* anneal, or slow-cool, (during the simultaneous formation of the emitter and BSF) that helped prevent quenching-induced lifetime degradation. The importance of this anneal proved highly material specific. For example, dendritic web silicon resulted in a bulk lifetime of only 0.6 μs upon quenching but this value improved to 200 μs by slow-cooling. In contrast, higher quality materials like Cz and FZ silicon did not require slow-cooling to preserve the bulk lifetime. This *in-situ* annealing added a maximum of only three minutes to the RTP diffusion time.

Another challenge of RTP is to maintain the gettering efficiency during the short-time processing. CNRS demonstrated by SPV measurements considerable P-gettering in only 25 s in RTP (see Fig. 7). An optimum temperature of 850°C to 950°C was determined for peak gettering efficiency and maximum diffusion length. They also showed increased diffusion length by the simultaneous co-gettering of P and Al.

Fig. 8 shows that P+Al co-gettering results in very high diffusion lengths. The co-gettering was found to be superior than either P alone or Al alone. The difference between the curve representing SPV measurements after BSF removal and the curve representing P-gettering alone is indicative of Al gettering alone during RTP.

3. Rapid and Effective Surface Passivation by Rapid Thermal Oxides (RTO) and PECVD Silicon Nitride

The fundamental understanding of enhanced diffusion, simultaneous processing, lifetime preservation, and gettering resulted in RTP cells (using photolithography) with efficiencies up to 17.1%, 16.8%, 14.8%, and 15.1% on FZ, Cz, multicrystalline, and dendritic web silicon, respectively [11]. However, a comparison with cells formed by CFP revealed a consistently lower short wavelength IQE response for RTP cells [12]. This was because RTP cells formed by simultaneous emitter and BSF formation lacked adequate passivation of the emitter surface. To overcome this problem several researchers including ourselves investigated RTO passivation of emitters. Schindler, et al. [6] reported an RTO-passivated cell with an efficiency of 16.6%, however, a CFP emitter was employed. More recently, Sivoththaman et al. [13] fabricated fully RTP-processed 100 cm^2 cells on mc-Si, which utilized an RTO to achieve efficiencies up to 14.1%. Our work on RTO emitter passivation showed a decrease in J_{oe} from about 900 to 100 fA/cm^2 resulting in cell efficiency improvement of 1% (absolute). As a result RTP cell efficiencies with evaporated contacts reached 18% on FZ and Cz silicon. The implementation of the uniform and rapid RTP-alloyed screen-printed Al-BSF (see section 2.2) reduced S_{back} from 10^4 cm/s to 300 cm/s and raised RTP cell efficiencies above 19% [14]. Thus, RTO passivation of the emitter provided a rapid means for effective front surface passivation while the simultaneously-formed SP Al-BSF provided effective back surface passivation.

To provide a more effective passivation scheme than the RTO alone, the combination of RTO and silicon nitride deposited by PECVD was investigated. At the 26th PVSC, we reported [15] a novel RTO+SiN passivation scheme which resulted in S_{back} values as low as 20 cm/s on 1 Ω-cm Si. This passivation scheme was compared with TiO_2 and three different SiN films deposited by different institutes [16]. On 90 Ω/sq. emitters (Fig.11), RTO+SiN reduces J_{oe} down to below 50 fA/cm^2. On 40 Ω/sq. emitters, RTO+SiN was found to give J_{oe} values around 200 fA/cm^2, which represents a reduction of at least a factor of two compared with TiO_2 (which gives almost no passivation). For back surface passivation (Fig. 12), RTO+SiN was found to reduce the worst-case S_{back} value ($S_{eff,max}$) to as low as 12 cm/s on 1 Ω-cm Si *after* a 730°C screen-printed contact firing anneal. It is noteworthy, that all other passivation schemes degrade after the 730°C anneal, but the RTO+SiN passivation improves because hydrogen from the SiN is released during the anneal and helps in passivating the RTO/Si interface. Effective dielectric passivation is even more important as the trend moves towards thinner cells. Fig. 13 shows that RTO+SiN front and back passivation can result in 17%-efficient 100 μm thin cells with a lifetime of only 20 μs and sheet resistance of 40 Ω/sq. for screen-printed contacts, provided recombination at the back contacts can be mitigated by an effective local BSF (which is possible by RTP as discussed in section 2.2).

4. Transition to High Throughput, Continuous Beltline Rapid Thermal Processing

One of the final obstacles facing application of RTP in industry is the lack of a high-throughput RTP machine. The work presented up till now involved only single wafer RTP systems. Recently, we have been developing a process using continuous beltline rapid thermal processing. Beltline systems equipped with tungsten-halogen lamps have been used to perform emitter diffusion, BSF formation, and screen-printed contact firing. Table 1shows the lighted I-V data for cells fabricated on FZ, Siemens Cz, and Bayer mc-Si. On monocrystalline Si materials efficiencies in excess of 16.5% have been obtained and confirmed by Sandia National Laboratories. Cells on mc-Si have so far given efficiencies around 14%. The data also show a very uniform result for these 4 cm^2 cells fabricated completely by beltline processing and screen printing. Compared with single-wafer RTP systems, the lamps in the beltline system do not run as hot and therefore emit fewer high energy photons resulting in slightly longer diffusion time. Additionally, the Al-BSF formed by single-wafer RTP systems is presently superior to those formed in the continuous beltline system possibly because of the lower ramp-up rate in the beltline system. S_{back} was found to increase from 200 to 2,000 cm/s for the beltline system.

Despite these current disadvantages, beltline processing is the simplest and cheapest process. IMEC and ECN have also recently published results using a beltline RTP system and have achieved 16.1%-efficient Cz cells [17] and above 14%-efficient mc-Si cells [18,19]. ECN has shown absolutely no difference between cells formed by beltline RTP and those formed by a beltline furnace with resistance heating [19]. However, they report between 25 and 65% lower diffusion time for the RTP beltline furnace compared with the resistive beltline furnace.

5. Conclusions

This paper highlights the recent progress of RTP cells. The work of several researchers was presented showing how RTP can be used to replace all high-temperature processes necessary for solar cell fabrication. RTP has been successful in establishing rapid and improved emitter formation, BSF formation, and surface passivation. The recent trend to continuous beltline RTP systems promises to achieve the goal of rapid processing with high throughput and high-performance devices.

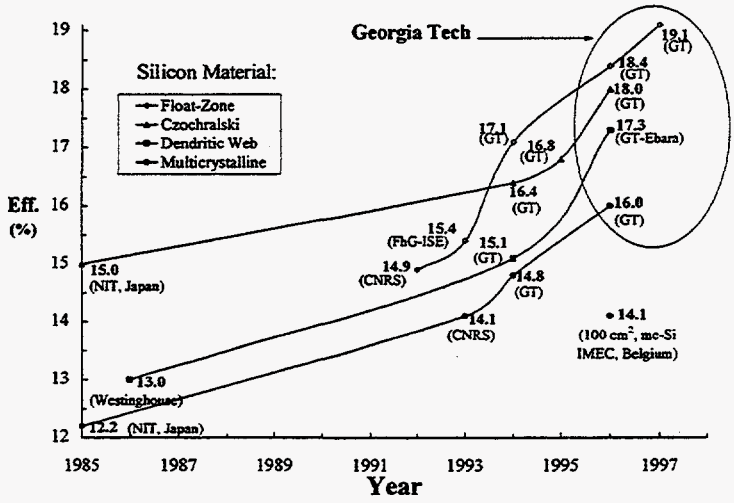

Fig. 1. Progress of RTP silicon solar cells fabricated with photolithography for contacts.

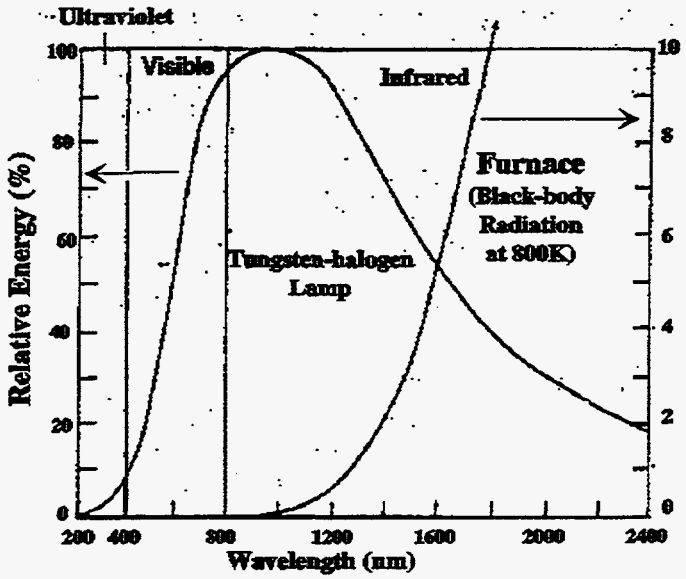

Fig. 2. Relative intensity of tungsten-halogen lamp and black body radiation at 800K (not drawn on same scale). [20]

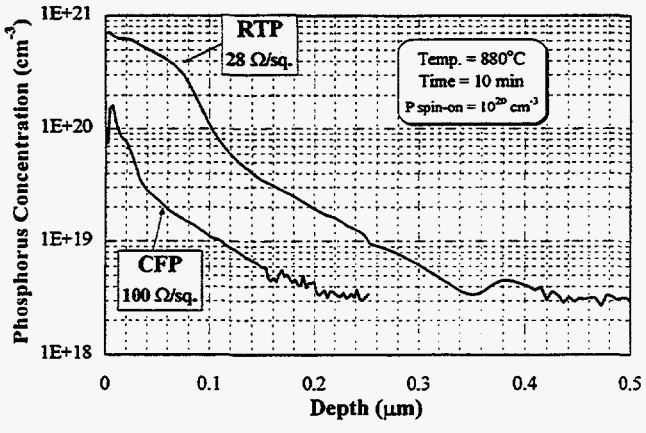

Fig. 3. SIMS profiles depicting enhanced diffusion in RTP under the same time/temperature/source conditions as CFP.

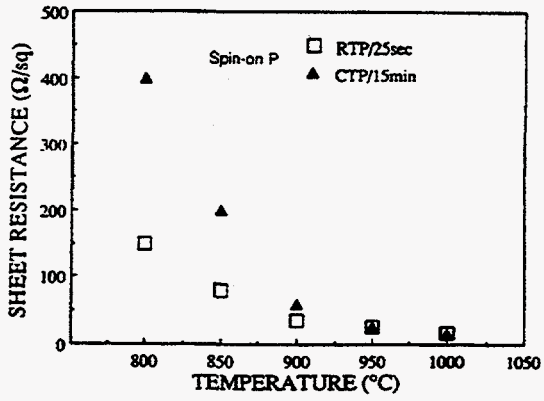

Fig. 4. Comparison between P-diffusion by RTP and CFP. [7]

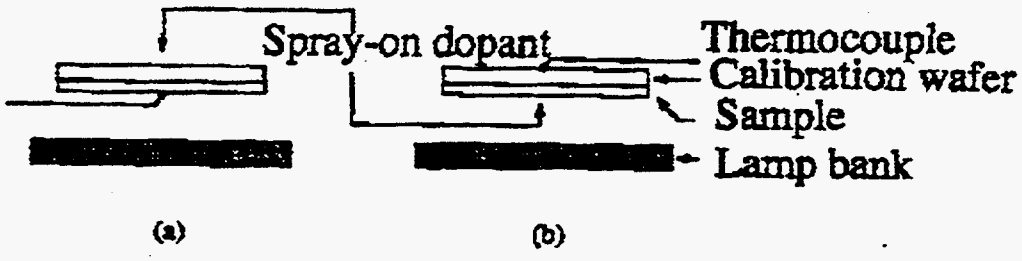

Fig. 5. (a) Back and (b) front irradiation setup for Singh's RTP diffusion experiment. [8]

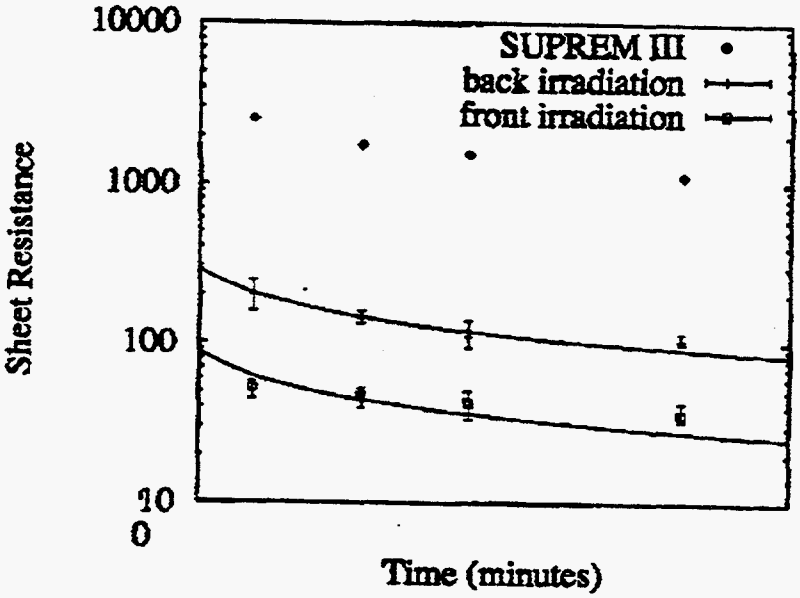

Fig. 6. Sheet resistance measurements for front and back irradiation at an RTP temperature of 860°C. Also shown are the results of SUPREM III calculations. [8]

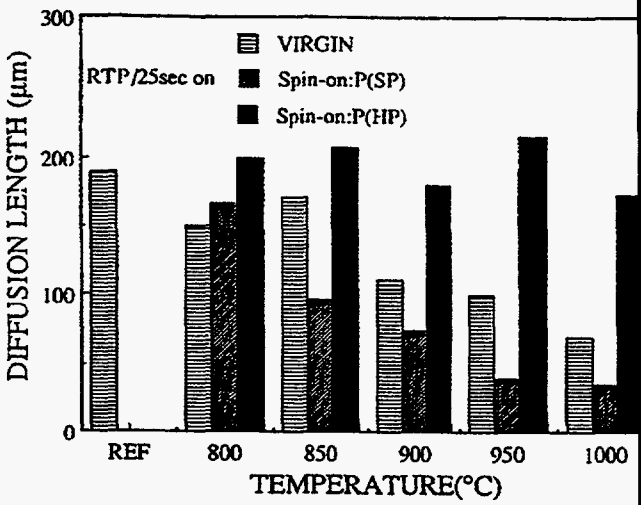

Fig. 7. P-gettering during 25 s of RTP. [7]

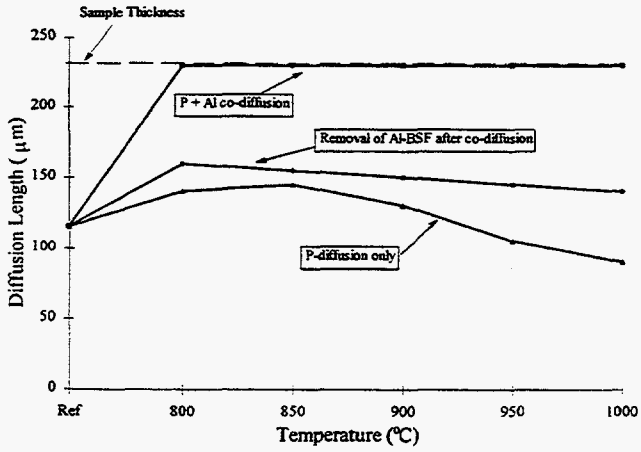

Fig. 8. Evidence of P + Al co-gettering in RTP. Difference between • and Δ marked curves represent the effect of Al gettering alone.

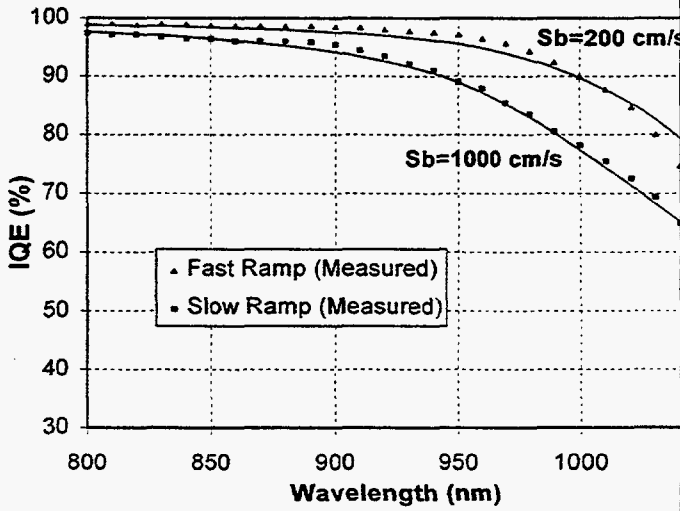

Fig. 9. Effect of heating rate on the long wavelength response with an Al BSF.

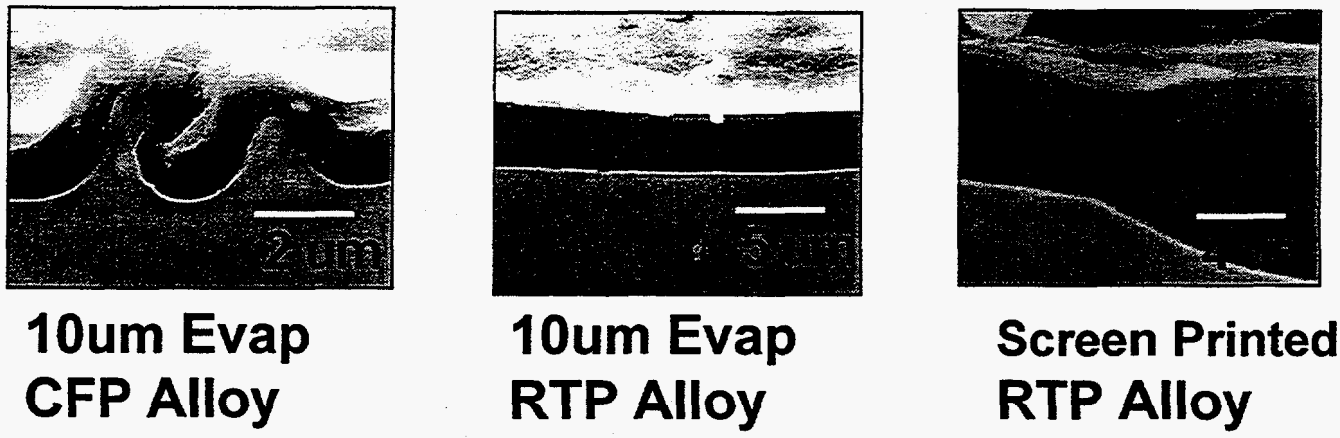

Fig. 10. SEM images of Al BSFs formed by alloying in the furnace and by RTP. The dark regions represent the p^+ regions

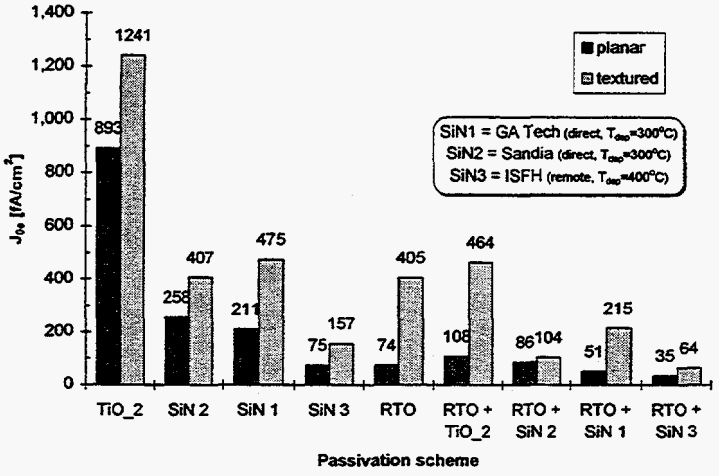

Fig.11. Comparison of various passivation schemes on a 90 Ω/sq. emitter.

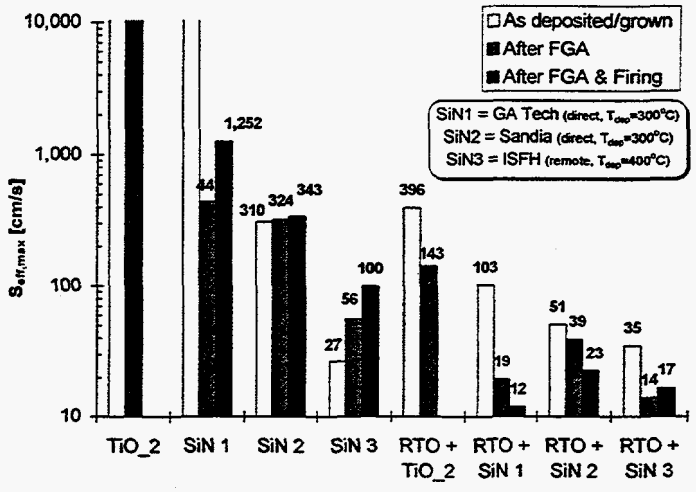

Fig. 12. Thermal stability of RTO+SiN films upon screen-printed contact firing.

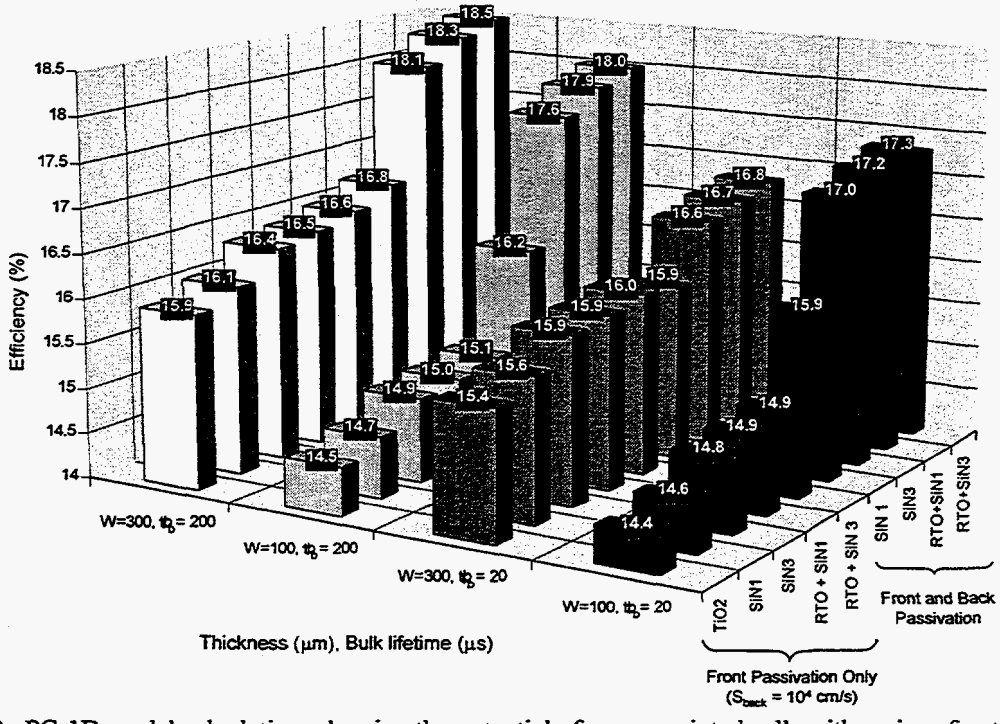

Fig. 13. PC-1D model calculations showing the potential of screen-printed cells with various front and back passivation schemes, cell thickness, and bulk lifetime. The calculations assume no effect of contacts.

Table 1. Cells formed completely by continuous rapid beltline processing and screen-printed contacts.

Run ID	Cell ID	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
BLP3	Bmc1-1	592	30.99	76.4	14.0
Bayer mc-Si	Bmc1-2	588	30.7	77.0	13.9
	Bmc1-3	584	30.53	75.4	13.4
	Bmc1-4	592	31.12	77.1	14.2
	Bmc1-5	589	30.61	73.9	13.3
	Bmc1-6	589	30.41	73.1	13.1
	Bmc1-7	592	31.43	73.7	13.7
	Bmc1-8	594	31.24	76.7	14.2
	Bmc1-9	591	31.00	76.4	14.0
	Average	590	30.89	75.5	13.8
BLP4*	F8-1	621	33.95	74.9	15.83
FZ (1.3 Ω-cm)	F8-4	625.5	34.28	77.6	16.63
	F8-5	625.7	34.21	77.4	16.51
	Average	624	34.1	76.6	16.3
BLP5	Scz1-1	620	33.66	78.0	16.2
Siemens Cz	Scz1-3	622	33.94	76.8	16.2
	Scz1-4	618	33.24	78.2	16.0
	Scz1-5	619	33.27	78.5	16.1
	Scz1-6	619	33.64	78.0	16.2
	Scz1-7	617	33.34	78.3	16.1
	Scz1-8	615	33.15	78.3	16.0
	Scz1-9	619	33.57	77.9	16.2
	Average	619	33.48	78.0	16.1
FZ (1.3 Ω-cm)	F2-1	622	35.02	77.2	16.8
	F2-2	622	35.02	77.0	16.8
	F2-3	622	35.15	77.0	16.8
	F2-4	624	34.94	77.5	16.9
	F2-5	621	34.77	76.9	16.6
	F2-6	620	35.03	76.9	16.7
	F2-7	624	34.99	77.4	16.9
	F2-8	622	34.77	77.0	16.7
	F2-9	623	34.81	77.3	16.8
	Average	622	34.94	77.1	16.8

*Confirmed by Sandia National Lab.

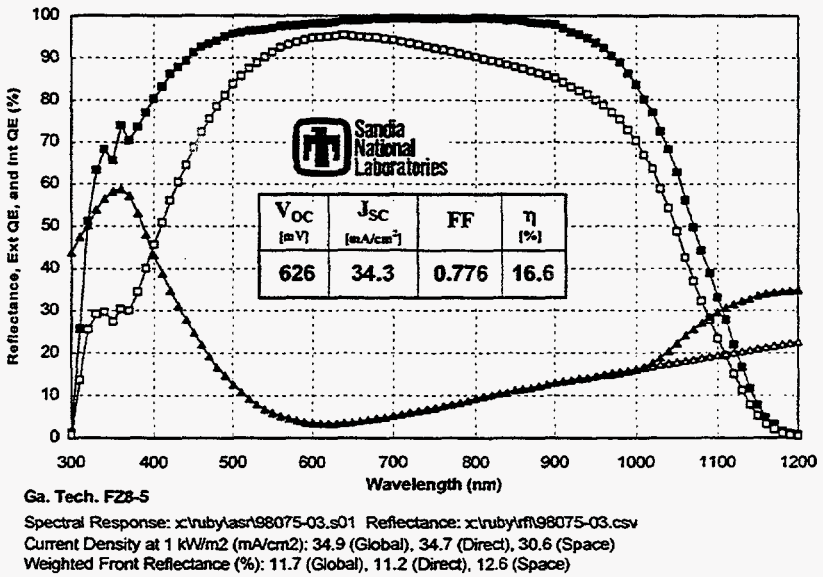

Fig. 14. Sandia measurement of the 16.6%-efficient screen-printed FZ cell made in the high-throughput continuous beltline RTP system.

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RTP OF SILICON SOLAR CELLS - LIFETIME EFFECTS AND SPECTRAL ENGINEERING

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The influence of rapid thermal processing steps on the volume lifetime in mc-silicon is investigated and a novel method of forming selective emitters is presented. Using spectral selection of the light utilized in RTP, diffusion profiles can locally be tailored to desired variations in sheet resistance of emitters.

1. INTRODUCTION

Rapid isothermal processing (RTP) based on incoherent radiation as the source of energy is emerging as a key low thermal budget processing technique for the manufacturing of advanced silicon integrated circuits. Rapid thermal processing has also been applied to solar cells in various laboratories. It was shown that all essential steps like diffusion of the pn-junction, formation of the back surface field or oxidation for surface passivation could be achieved by means of RTP ([1], [2], [3] and [4]). In these experiments the process times were kept short in the range of 10 to 30 seconds. Other experiments reported extended process times up to five minutes including an in situ anneal which bridges RTP to conventional processing [5].

Minority carrier lifetime variations can be observed in silicon samples after different processing conditions. There is no doubt that the minority carrier lifetime is an essential point in obtaining high solar cell efficiencies. The processing conditions can be optimized in order to get high minority carrier lifetimes in combination with the formation of a selective emitter.

2. EXPERIMENTAL PRINCIPLE

2.1 Formation of selective emitters

The black body radiation depends on the temperature of the energy source. In the case of furnace processing the substrate temperature and the furnace temperature are identical (thermal equilibrium). The spectrum of the radiation consists of photons in the infrared wavelength region. Thus, this radiation results in thermal reactions, where ground state levels of molecules or solids are raised to higher vibrational levels of the electronic ground state and dissociation or breaking of bonds can occur if sufficient energy is available.

In the case of rapid thermal processing the substrate temperature is low in comparison to the filament temperature of the lamps. The spectrum of the incoherent source of light consists of photons from vacuum ultra violet to the infrared energy region. Photons of appropriate wavelength (from far UV to visible) induce transitions from the ground state to a quantized electronically excited state in the case of atoms and to a quantized rotational and vibrational level of an upper electronic state in the case of small molecules [6].

The experiments described here make use of the difference in the spectrum of RTP when visible and shorter wavelength light is partially filtered. As a test structure stripes of a few mm width have been employed made of parallel slabs of multicrystalline silicon wafers. Also for Diffusion RTP system with dedicated UV lamps were used.

The diffusion of phosphorus atoms into p-type silicon is achieved by spin- or spray-coating of a thin film of dopant like Merck´s Siodop or Filmtronics 509 films acting as a diffusion source Also boron doped spin-on films are used. The wafers, monocrystalline and block cast type multicrystalline silicon, are processed in a commercially available AST-RTP system allowing individual control of upper and lower lamp arrays. Additionally a RTP system equipped with special

UV lamps was used. Both temperature and time were varied in the experiments in a systematical way.

The spectral selection of the light is achieved by placing a shadow mask made of suitable material in close distance next to the wafer (fig. 1). Due to absorption the shaded areas of the wafer only see the light which is not absorbed by the mask. If a silicon mask is used the shaded areas see light with wavelengths larger than the bandgap of silicon, i.e. > 1.06 µm (fig. 2).

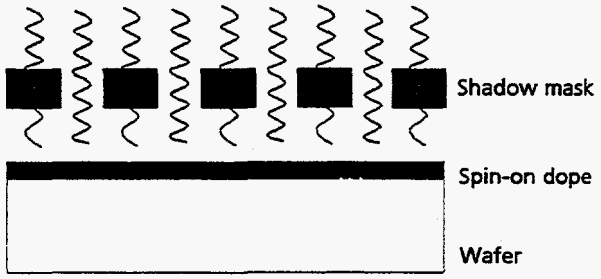

Fig. 1 Realization of the shadow mask

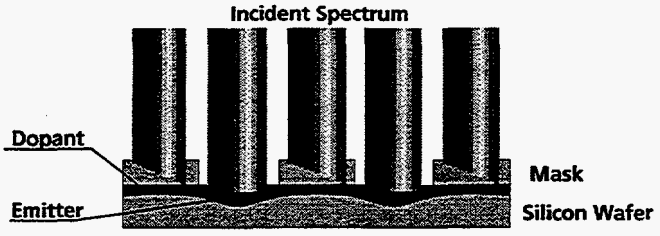

Fig. 2 Wavelength selection due to the shadow mask

2.3 Thermal treatment and lifetime measurements

The influence of rapid thermal treatments in different atmospheres or diffusion steps on minority carrier lifetime was investigated on monocrystalline and mainly on multicrystalline silicon wafers. The experiments on mc-silicon were carried out using a stack of consecutive wafers from a cast ingot. This allows the direct comparison of the minority carrier lifetimes of processed and unprocessed wafers, since the intrinsic properties of the wafers are assumed to be similar. Prior to processing the wafers were etched in order to remove the saw damage followed by an RCA clean. For the diffusion experiments either a 1 µm Al layer was evaporated or a phosphorus spin-on dopant was applied. For codiffusion experiments the Al layer was evaporated before the deposition of the spin-on phosphorus film. Immediately afterwards the wafers were processed.

The influence of heating and cooling gradients or ramps, process temperatures and times on minority carrier lifetime was investigated in a systematical way. Minority carrier lifetime measurements were performed at identical positions on the wafers by means of microwave photo conductance decay (MW-PCD). The diffused layers were removed chemically or mechanically before the lifetime measurements were carried out. The surfaces of the wafers were passivated with an iodine-ethanol solution during PCD measurements allowing the determination of the accurate minority carrier lifetime of the bulk [7].

3. ANALYSIS AND DISCUSSION

3.1 Selective emitter by Spectral Engineering

3.1.1 Sheet Resistance Topography

After diffusion - carried out in the way described above - sheet resistance topography was performed using a four point probe in van der Pauw orientation [8]. Fig. 3 shows an example of a sheet resistance variation of 10 Ω/sq. The difference in sheet resistance depends critically on the processing temperature and time. For short time processing variations of 150 to 60 Ω/sq have been observed and for higher temperatures variations from 40 to 30 Ω/sq.

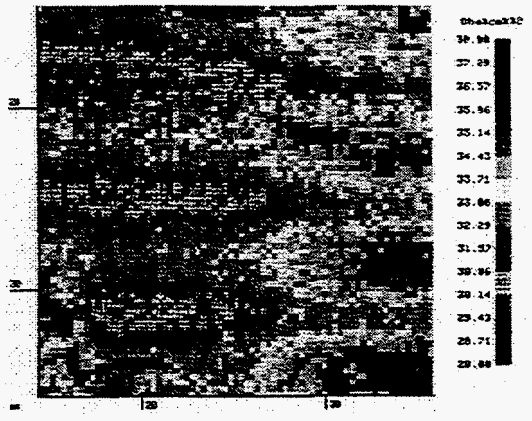

Fig. 3 Sheet resistivity mapping

3.1.2 Secondary Ion Mass Spectroscopy and ECV Profiling

Fig. 4 shows SIMS profiles of phosphorus obtained from fully shaded and completely unshaded wafers processed under similar conditions. It is remarkable, that the profiles for the shaded and unshaded process differ mostly in the surface concentration of phosphorus, while the depth of the diffusion profile is nearly the same. The profile of the unshaded process exhibits the typical feature of kink and tail which in the classical case is a result from high concentration phosphorus surface sources [9]. In the shaded case the kink and tail shape is not so pronounced.

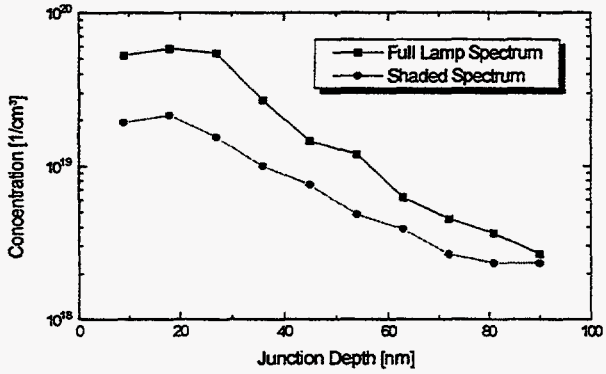

Fig. 4 SIMS profiles for shaded and unshaded regions.

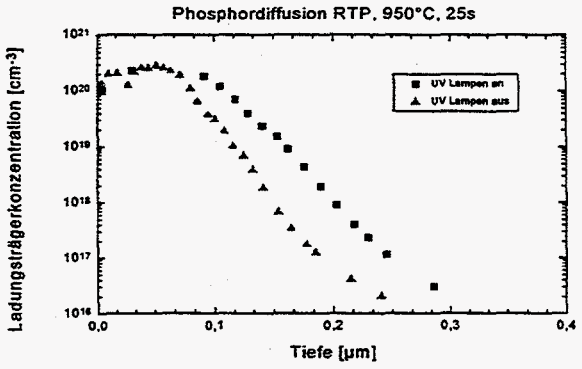

Fig. 5 shows the carrier concentration according to ECV profiling with and without UV photons available.

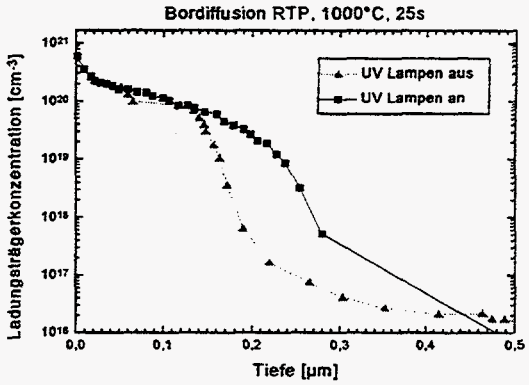

Fig 6 gives the ECV-profile of boron after RTP diffusion with and without UV light.

The analysis of the diffusion coefficient for phosphorus at 900 °C is 3.4 10^{-14} cm²/s. In comparison, the diffusion coefficient for classical furnace diffusion at the corresponding temperature is D = 3.6 10^{-15} cm²/s. This is one order of magnitude lower than in RTP [12].

The role of the short wavelength part of the spectrum responsible for the differences observed in the profile may be due to an effective enhancement of the solubility of electrically active phosphorus at the surface. The short wavelength light generates a large amount of electrons and holes in the electronic system, which directly or indirectly lead to an enhancement of phosphorus solubility.

In order to study the influence of UV or short wave length light on the diffusion properties of phosphorus and boron we performed drive-in experiments using classical predeposition steps. The P-glass and B-glass layers were removed prior to the RTP drive-in. As an example fig. 7 shows the ECV-profiles of phosphorus after RTP drive-in. Using UV lights did not yield in any different profile than using longer wavelength light.

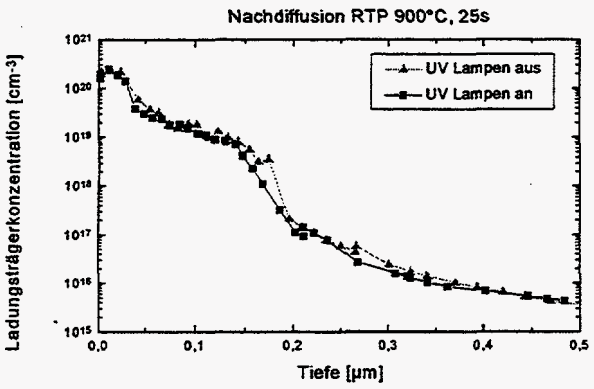

Fig. 7: RTP-dirve-in diffusion of P.

From the experiments we have to draw the conclusion that the enhanced diffusion due to the short wave lengths light effects at the interface between the dopant source or within the dopant source rather than in the silicon itself.

3.1.3 Reoxidation

After rapid thermal diffusion and subsequent etching of the phosphorus glass the wafers were oxidized using no shading mask, i.e. the wafers saw the full lamp spectrum. This oxidation is performed in order to demonstrate different surface concentrations of phosphorus. As observed earlier the oxide thickness varies according to the phosphorus surface concentration of the emitter [3]. As to be expected, enhanced oxide growth is observed in the more heavily doped regions resulting in corresponding variations of oxide thickness during reoxidation (fig. 7 and 8) - (Note: oxidation using the spectral shading described above results in higher oxidation rates in shaded areas compared to unshaded regions [13]!).

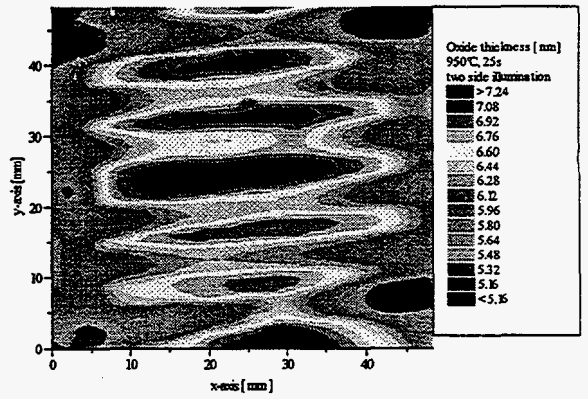

Fig. 5 Variations in oxide thickness for two-side illumination

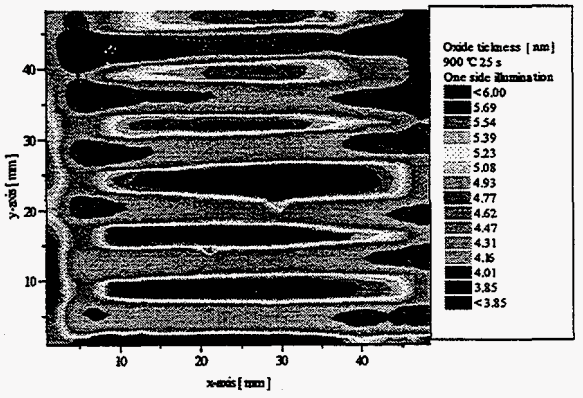

Fig. 6 Variations in oxide thickness for one-side illumination

3.1.4 Minority Carrier Lifetime Measurements

Measurements of the effective lifetime were performed using the modulated free carrier absorption technique (MFCA) [14]. Fig. 9 shows an example for the distribution of effective lifetime after selective emitter formation. Assuming the bulk lifetime to be constant throughout the wafer and not influenced by rapid thermal processing the reduction in lifetime is due to higher recombination in the emitter. The effective minority carrier lifetime is reduced in areas, where the concentration of phosphorus is higher. Thus the map of the effective lifetime reflects the phosphorus concentration of the wafer.

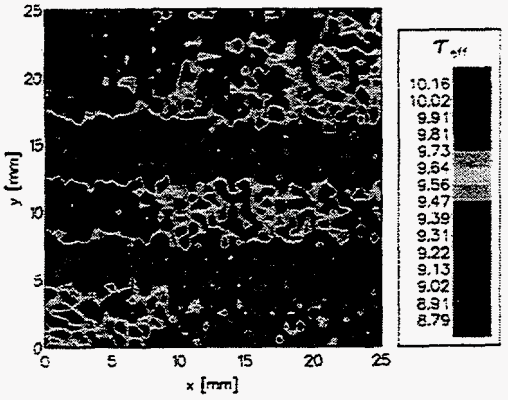

Fig. 7 MFCA map showing different surface concentrations of phosphorus

3.2 Selective emitter formation by Laser overdoping

In this method a homogenous lightly doped emitter is first made by RTP from a P-doped spin-on glass film. Afterwards laser overdoping of contact regions follows, to form the selective emitter structure, by writing the grid pattern using a laser beam [14a].

3.3 Effects on volume lifetime

3.3.1 RTP treatment in nitrogen ambient

Heat treatment of the wafers in nitrogen ambient with bare surfaces leads to a substantial reduction of minority carrier lifetime (fig. 10).

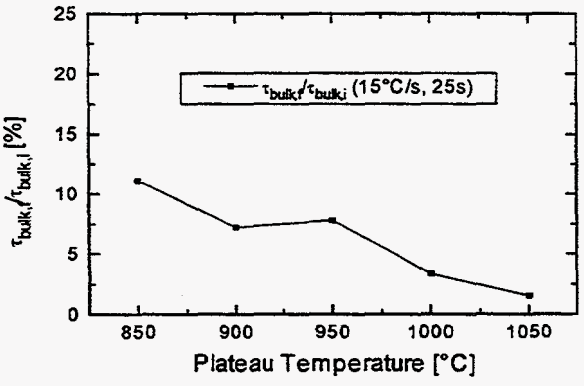

Fig. 8 Rapid thermal annealing: different processing temperatures

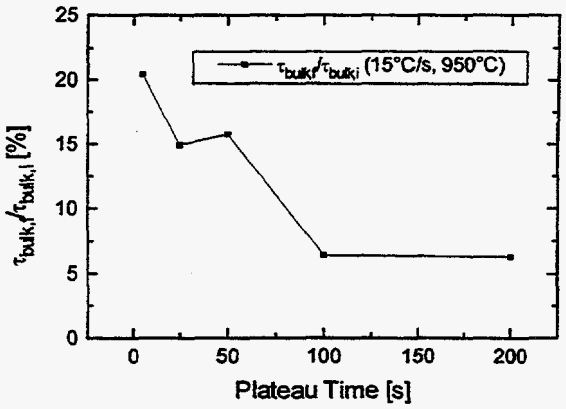

Fig. 9 Rapid thermal annealing: different processing times

The degradation is more pronounced for higher process temperatures and also depends on the process time at elevated temperature (fig. 11). No influence on temperature gradients can be observed in the range from 5 to 100 K/s.

As the degradation is very severe leading to minority carrier lifetime of few µs for FZ-silicon and less than 1 µs for mc-silicon it is supposed that deep level traps are introduced during processing. However, DLTS measurements did not reveal any chargeable point defects within the entire bandgap which are known to be lifetime killers in silicon, like Fe or similar impurities.

Etching experiments have shown that the lifetime degradation is not restricted to the near surface area but rather homogeneous throughout the bulk of the wafer. From this observation one can deduce that shallow traps may be responsible for the decay of minority carrier lifetime. The nature of these defects is unknown up to now.

Also experiments with thermally oxidized wafers were carried out. The wafers were oxidized in a conventional furnace for capping purpose. After rapid thermal annealing in nitrogen ambient lifetime measurements were carried out. They showed, that there is no degradation of minority carrier lifetime using capping layers.

3.3.2 RTP treatment in oxygen ambient

Replacing the nitrogen atmosphere by oxygen leads to less dramatic effects like those observed for treatments in nitrogen (fig. 12 and 13). The degradation is nearly independent of the temperature and only little influence is observed with increasing process time. Again, no influence on temperature gradients is observed.

The less dramatic effect during oxidation may be connected to the silicon/silicon-oxide interface. The moving interface is an efficient sink for self-interstitials and vacancies which are generated during the heat treatment.

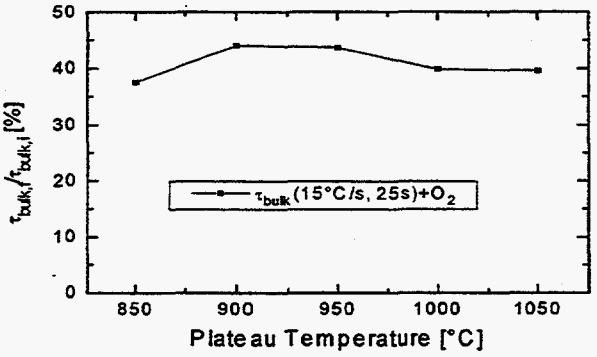

Fig. 10 Rapid thermal oxidation: different processing temperatures

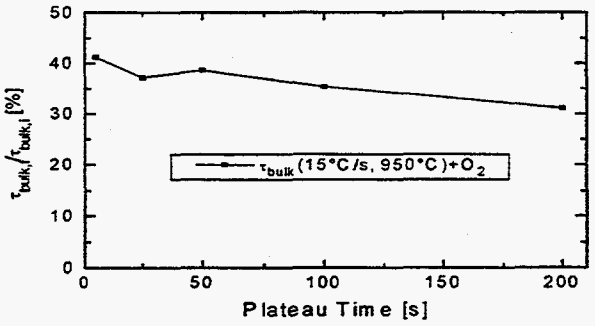

Fig. 11 Rapid thermal oxidation: different processing times

3.3.3 Rapid thermal diffusion

The experiments involving diffusion of aluminum or phosphorus differ from the above mentioned experiments because at least one side of the wafers is covered by a layer of dopant solution or Al. This could be seen as a kind of capping of the surfaces.

The results are given in fig. 14, 15 and 16. Compared with the experiments described above the degradation of minority carrier lifetime is much smaller during phosphorus diffusion. On the given scale the degradation seems to be independent of ramp slopes, process temperatures and process times.

This effect may be attributed to some kind of gettering, which does not occur during annealing in nitrogen or during oxidation. The gettering effect runs in parallel to the above discussed degradation effects.

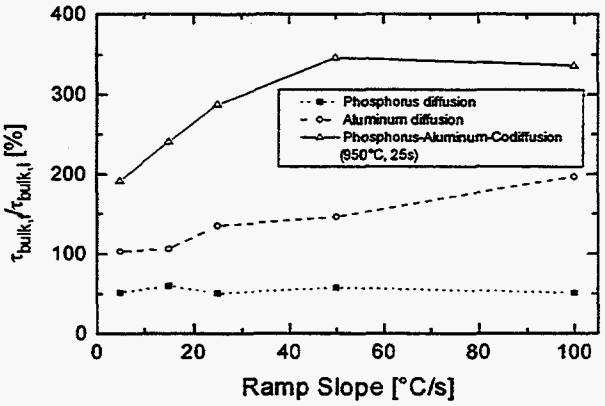

Fig. 12 Rapid thermal diffusion: different ramp slopes

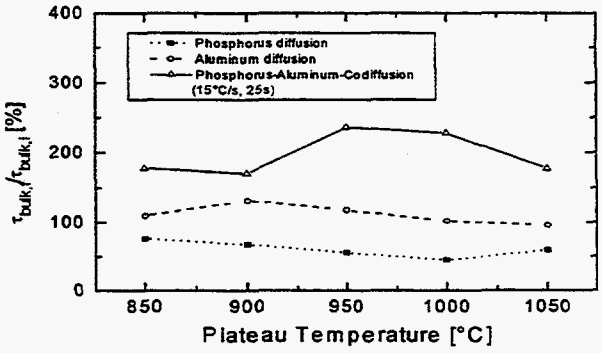

Fig. 13 Rapid thermal diffusion: different processing temperatures

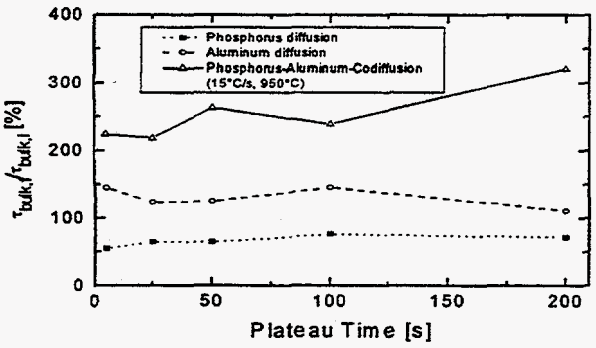

Fig. 14 Rapid thermal diffusion: different processing times

For aluminum diffusion lifetime does not degrade or even can be improved. Process time and process temperature do not influence lifetime. The temperature gradient however seems to influence the lifetime improvement. For larger heating and cooling gradients (80-100 K/s) lifetime improvements by a factor of 2 are observed. Again this is attributed to gettering. Al seems to be superior to phosphorus diffusion gettering under RTP conditions.

Codiffusion of phosphorus and aluminum, each on opposite sides of the wafer, is superior to any of the individual diffusion steps: an optimum process temperature of about 950°C can be found. The lifetime is increasing with increasing process time. Furthermore, temperature gradients exceeding 40 K/s yield minority carrier lifetime improvements by more than 300% in mc-silicon.

The gettering effect in codiffusion of phosphorus and aluminum is well known in the photovoltaic community, although the exact mechanisms are not understood up to now. The surprising effect in the investigations presented is the large improvement in minority carrier lifetime using only short process times.

4. APPLICATIONS TO SOLAR CELLS

Using process conditions derived from the investigations on development of volume lifetime silicon solar cells with an area of 50x50 mm² were processed on Cz and mc type silicon. In contrast to the volume lifetime investigations the diffused layers of p^+ and n^+ are not removed but used as backsurface field and emitter, respectively. Emitter and backsurface field were diffused in one single RTP step. Both homogeneous and selective emitters were also formed during this single RTP step. After etching of the phosphorus glass a passivation oxide was grown by means of rapid thermal oxidation. Following metallization by evaporation a double antireflection coating was applied.

Solar cell efficiencies of 16.3% (AM1.5) were achieved in Cz material for both homogeneous and selective emitters. A detailed analysis showed, that for the selective emitters the doping concentration was too high which yielded in losses in spectral response for short wavelength of the incident light. Compared with classical processed solar cells the backsurface fields of the ones processed in a RTP furnace lead to a better response in the long wavelength range.

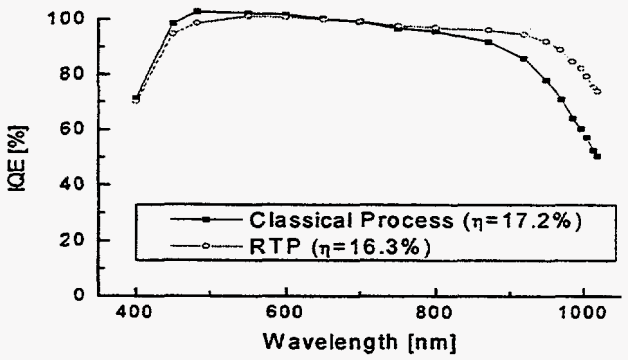

Fig. 15 Comparison of the spectral response of solar cells processed in classical and RTP furnace

Efficiencies in mc-cast material reached up to 13.2% due to serious losses in the bulk diffusion lengths during RTP.

5. CONCLUSION

By selecting parts of the spectrum of incoherent RTP light sources the profiles of phosphorus doped emitters can be "tailored". This allows to process selectively doped areas on the wafers without any photolithographic masking or etching step. The variation in sheet resistance is dominated by a higher surface concentration of phosphorus rather than by differences in junction depths. Lifetime degradation during RTP treatment is observed if no

gettering is applied. The source of the defects or impurities responsible for the degradation of the minority carrier lifetime has not been identified.

ACKNOWLEDGMENT

The authors appreciate the skillful assistance of the solar cell technology group.

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Light induced effects in Rapid Thermal Diffusion processes from doped oxide sources*

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Abstract
The formation n^+p or n^+pp^+ junctions by rapid thermal diffusion or co-diffusion into silicon is opening new possibilities for low-cost and environmentally safe solar cell production. In this work we analyze the influence of the higher energetic part of the lamp spectrum on phosphorus diffusion, and the impact of evaporated aluminum for back-surface field formation during a P-Al co-diffusion step. The diffusion of phosphorus from doped glass films spun onto monocrystalline silicon material in different furnace conceptions with front, back or double sided heating is studied to investigate the influence of the radiation spectra on the dopant profiles. The experiments reveal a relation to the amount of ultraviolet radiation reaching the surface. Therefore a modified RTP-System is used for further investigations to demonstrate the influence of the UV light on the diffusion profiles. These experiments show clearly, that the influence of the UV light is mainly on the densification of the spin-on-glass and not on the diffusion kinetics in silicon. The simultaneous formation of a back surface field is of special interest for solar cells. Former studies of the simultaneous diffusion of phosphorus and aluminum in order to form a n^+pp^+ structure show deeper n^+ emitters compared to a single phosphorus diffusion. Using glass densification and oxidation experiments on such prepared samples a correlation was found between the decrease in emissivity on the aluminum coated part of the wafer and the increase in temperature, which is responsible for the deeper profiles.

Introduction

Forming p-n junctions by Rapid Thermal Diffusion (RTD) is opening new possibilities for low-cost and environmentally safe solar cell production, as it has been shown in several laboratories[i,ii,iii]. Higher diffusion kinetics compared to classical diffusion processes are observed in RTD systems[iv]. Further important differences between several commercial available RTP furnaces, are found. This leads to the question if the radiation spectra, especially the UV part has an influence on the diffusion mechanisms or on the glass densification of the spin on glass (SOG). One of the central interest in RTD for solar cells as well as for microelectronics is, if UV light has an impact on phosphorus diffusion in silicon during an RTP anneal, in order to reduce the thermal budget. These effects of the lamp spectrum will be reviewed and discussed in part 1.

Another important object discussed in part 2 is the possibility to form n^+pp^+ structures in a single thermal cycle[v,vi,vii], by using phosphorus spin-on dopant (P-SOD) film as dopant source on the front surface and an evaporated aluminum layer on the backside. Beyond the formation of a back surface field, the rapid thermal co-diffusion of P enhances the gettering efficiency of the metallic impurities and induces deeper emitter junctions [vi,vii]. The improvement due to the presence of aluminum on the back side is explained by the formation of an Al-Si eutectic which acts as a sink for the metallic impurities. However the reason of the enhanced phosphorus diffusion is so far not well established. Assumptions involving an increase of injected self-interstitials through the substrate as well as an increase of the total absorbed energy due to the light confinement have been brought forward. Different colors of the remaining doped oxide have been observed after rapid thermal treatments when aluminum is present on the backside compared to samples without aluminum, which suggest a difference in temperature of the bulk materials.

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PART I: Influence of UV-light on Rapid Thermal Diffusion of phosphorus into silicon

Experimental Procedure

Different Furnace Conceptions

Two RTP systems with different conceptions were used for the dopant diffusion experiments. Figure 1 shows a schematic of the JIPELEC furnace, representing a cold-wall furnace with one-side irradiation. The water cooled chamber is made of stainless steel serving as a reflector. The wafer is heated from the top through a double-quartz window with water circulation in between using 12 halogen lamps. The temperature is monitored by a pyrometer which has been calibrated using a thermocouple instrumented wafer.

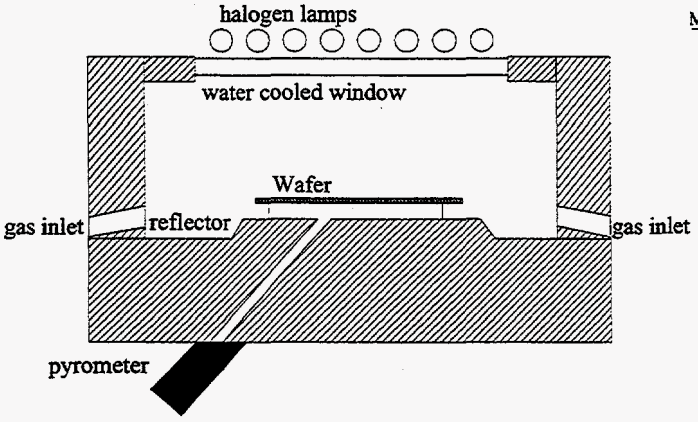

Figure 1: RTP furnace conception with one lamp bank and back reflector (JIPELEC)

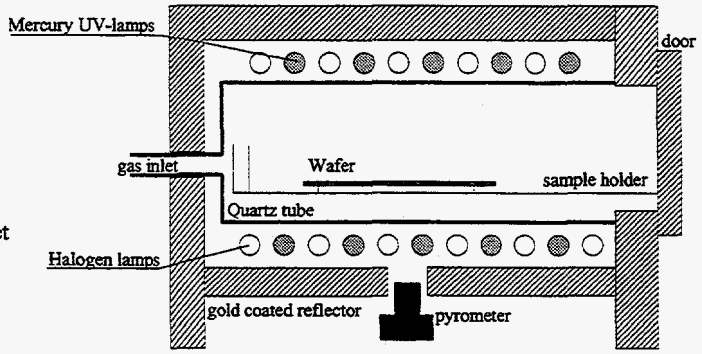

Figure 2: RTP furnace conception with two lamp banks and front and back reflector (STEAG-AST)

Figure 2 shows a schematic representation of the STEAG-AST warm-wall furnace. The gold coated reflector chamber is water cooled and contains a quartz tube with a sample holder. In this furnace 22 IR lamps and 16 low pressure mercury UV-lamps are arranged alternatively above and below the quartz tube between reflector wall and quartz chamber. The temperature is also measured by a calibrated pyrometer. The UV-lamps have a total power of 300W and emit their radiation mainly on two lines: 254 nm and 185 nm (intensity approximately 15 % of 254 nm line). This furnace offers the possibility to heat the wafer with the IR-lamps from both sides (case A), only from the bottom (case B) and only from the top (case C). In all three illumination modes all UV-lamps can be switched on or off. Case C was used to approach the JIPELEC conception (J).

Sample Preparation

A thin film of phosphorus glass (PSG) acting as a dopant source was deposited onto p-type silicon wafers using the spin-on technique. A spin-on dopant (SOD) of high phosphorus concentration ($C_{Phos}=2x10^{21}$ cm^{-3}), considerable as an infinite doping source was selected. After spinning, the SOD film was immediately baked at 200°C for 10 min. before rapid thermal treatment.

Rapid Thermal Treatment

During the diffusion process, the SOD film always was placed topside up. (Figure 3). The experiments were done at temperatures between 850 and 950 °C in nitrogen ambient for 25 s. All diffused junctions were analyzed in terms of sheet resistance by four-point probe method, Secondary Ion Mass Spectroscopy (SIMS), Electrochemical Capacitance-Voltage (ECV) profiling and Boltzmann-Matano analysis.

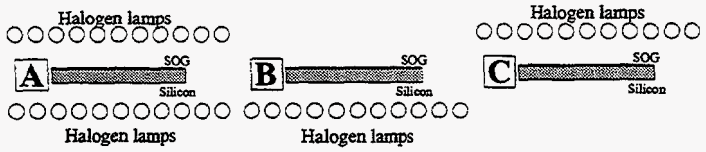

Figure 3: Used lamp configurations on the STEAG-AST furnace.

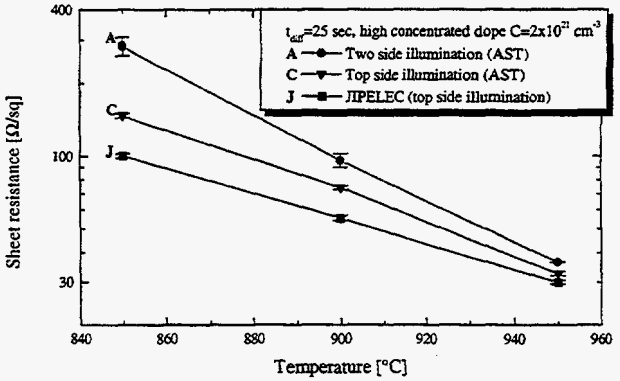

Figure 4: Resulting sheet resistances of different illumination modes on the STEAG-AST furnace compared to the JIPELEC furnace.

Comparison of the different reactor designs in terms of radiation

The spectrum of halogen lamps in RTP furnaces is described by the black body radiation and depends on the filament temperature. The greatest intensity of the spectrum is emitted in IR/visible/UV region for classical applied process temperatures (800°C - 1100°C). As less lamps are used, as in the JIPELEC conception or case C of the STEAG-AST furnace, the same radiation energy has to be assured to reach a comparable sample temperature. Therefore the lamp power is reaching higher values and the filament is pushed to higher temperatures, leading to a lamp spectrum with higher visible and UV quantities. For similar process conditions (temperature, diffusion time), great differences on diffusion results can be observed on furnaces with a different conception of lamp geometry, as the furnaces presented here.

Working with comparably prepared samples (spinning and pre-baking), leads in this used furnaces to different results for comparable process conditions. Figure 4 reports the sheet resistance values measured on silicon samples after RTD in JIPELEC and AST units. We observe decreasing values for increasing temperature, indicating higher dopant activation. Comparing case A and J, is showing generally higher values in function of temperature for case A than J. This trend can also be observed between case A and C. In fact we notice reducing sheet resistance values and therefore higher dopant activation for the lamp configuration (case J) last specified.

Observing this higher dopant activation at the same sample temperature, for furnace configurations with higher lamp power and therefore higher filament temperature (C), leads us to examine the diffusion behavior of phosphorus in silicon in an RTP furnace with additional UV-lamps (AST), in order to accentuate the phenomena. The configurations A, B and C were analyzed with additional UV.

Spectral distribution in RTP furnaces

Theoretical calculations based on the Planck's radiation law allows to know approximately the flux of photons reaching the silicon surface. For this model it is assumed that the quartz windows have no absorption and the reflector is reflecting 90% of the light. Knowing the lamp geometry, the flux of power I at the emplacement of the sample can be calculated for a given lamp pitch, filament length and lamp power. The expression for the emitted number N of photons between λ and $\lambda+d\lambda$ per second and per unit area can be found as:

$$N(\lambda,T) = I \cdot \beta \cdot \frac{d\lambda}{\lambda^4 T^4 \cdot \left(\exp\left\{ \frac{\gamma}{\lambda T} \right\} - 1 \right)}$$

with T : Filament temperature
λ : Wavelength
I : calculated power density for given lamp geometry and lamp power [W/m^2]

Assuming equivalent power flux for the two illumination modes, as the samples have the same temperature, the only parameter able to vary is the filament temperature. Weighting the number of photons with their energy, allows to determine the spectral power density and to compare it for both

modes analyzed here (Figure 5). A spectral shifting to shorter wavelengths for the top side illumination (C) can be observed, in comparison to the two-side illumination mode (A), due to Wien's law.
From this observations we can conclude a relationship between dopant diffusion and the spectral distribution of the furnace lamps. We generally observe lower sheet resistance results for power spectra with higher power densities in smaller wavelengths. The different spectra are made responsible for the different diffusion results. For all following experiments and conclusions, we will base our observations and reflections on the AST furnace, used with and without additional UV-light.

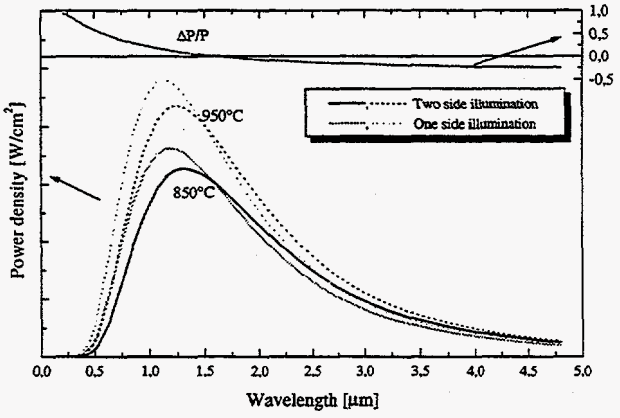

Figure 5: Estimated power spectra for the studied illumination modes and calculated relative spectral differences.

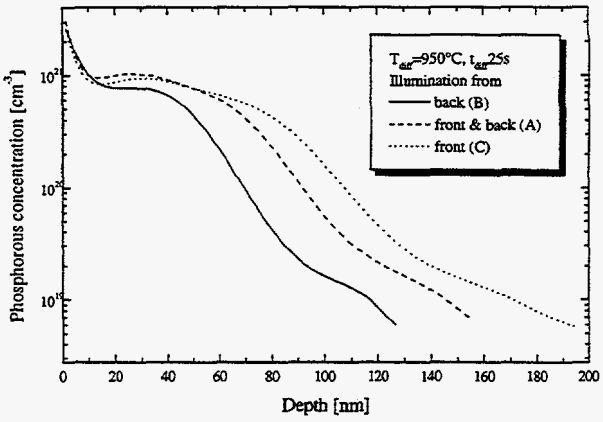

Figure 6: Measured SIMS profiles at 950°C process temperature for illumination cases B, A and C

Diffusion results and analysis

Dopants distribution results

The phosphorus distribution into silicon after RTD was monitored by SIMS. The resulting profiles are shown in Figure 6 for processing temperatures of 950°C and 25 seconds diffusion time.
The profiles show increasing junction depths going from back side (B) over double side (A) and front side (C) heating. This can be correlated to the amount of short wavelength light reaching the spin on glass surface. In case B no direct light reaches the sample surface with the SOG. In case C all light reaches the surface. Comparing case A and C the power per lamp is lower in case A. The amount of high energy photons is therefore expected to be higher in case C. This may indicate a diffusion enhancement in presence of high energy photons. Therefore further experiments with additional UV-light were carried out.
Diffusion coefficients as calculated by Boltzmann-Matano analysis using SIMS profiles are shown in Figure 7. We see a decreasing diffusion coefficient value looking from case A to case B. As in case B the sample is illuminated from the back, only the transmitted spectrum to the doping interface is contributing in diffusion mechanisms. As we turn on additional UV light (case B & UV) the value is nearly coming back to the diffusion coefficient obtained in case A. This is showing the close connection between UV-light and diffusion results.
It should be mentioned, that diffusion coefficients in the sample volume can be influenced from the surface, by injection of interstitials or other mechanisms and therefore affect the volume diffusion through different surface or interface states.

Annealing of pre-diffused samples

For this experiment samples are prepared in a conventional $POCl_3$ furnace. After HF etching to remove the PSG layer the samples were annealed in the STEAG-AST RTP furnace with and without additional UV illumination. No significant variation in surface concentration as well as in junction depth has been detected (Figure 9). This result rules out the contribution of the UV light to a diffusion enhancement

when a doped oxide layer is not present on the surface. This leads to assumption that the short wavelength photons interact with the doping oxide and the P-SOD/Si interface where photochemical effects may play a role e.g. through bond breaking and oxide densification.

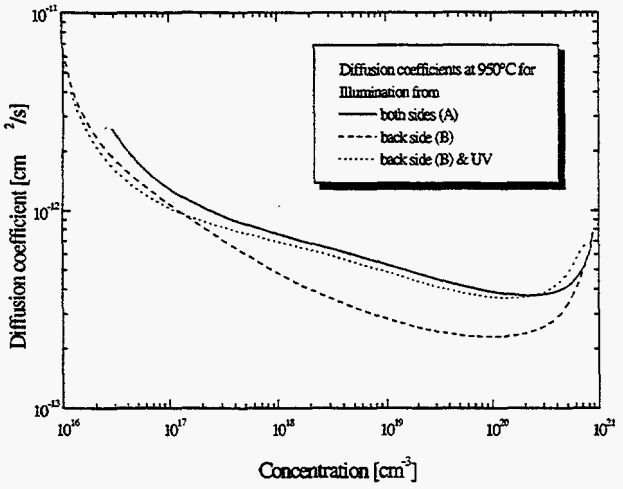

Figure 7: Calculated diffusion coefficients by Boltzmann-Matano analysis at 950°C for illumination modes A, B, B&UV

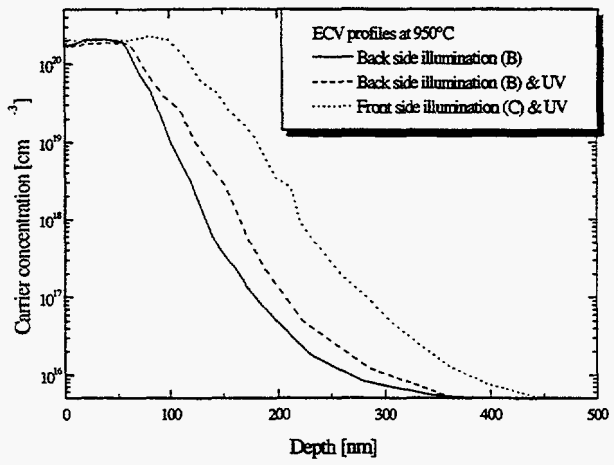

Figure 8: ECV profiles for front side illumination (C) with additional UV-light and back side illumination (B) with and without additional UV-light.

Discussion

Knowing the absorption coefficients of silicon at the used sample temperatures[viii,ix] the spectral density reaching the doping interface for back illumination (B) can be calculated. This calculation shows, that all high energetic (UV) and visible photons emitted by the halogen lamps are absorbed. Only a few photons in the range of 1500 nm is reaching the doping interface. That means, in case of back side illumination and additional UV light, only the part from the upper UV lamps can be made responsible for any variation in diffusion results. For the modes A and C the entire spectrum of the halogen lamps is incident towards the sample. These photons can affect the diffusion process from the surface. From the observation of the drive-in following conventional diffusion, we have to conclude that the spectral influences are of importance in the densification of the spin-on film as well as the P-SOD/Si interface rather than in the diffusion into silicon.

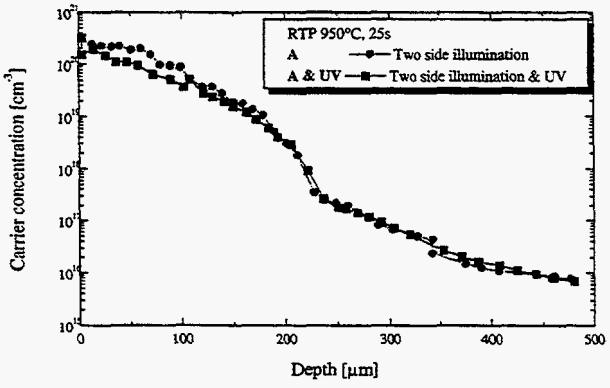

Figure 9: ECV-profiles of pre-diffused samples after RTP anneal at 950°C with and without additional UV-light.

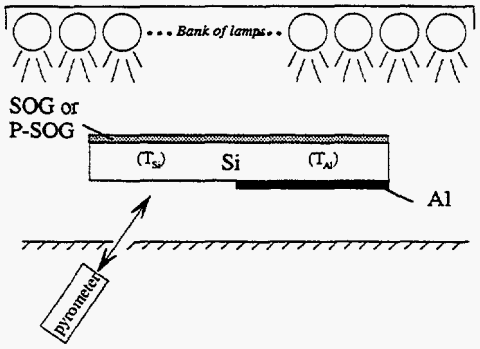

Figure 10: Experimental setup : The pyrometer is looking the uncovered wafer half, while the tungsten halogen lamps are illuminating the hole surface.

PART II: Impact of aluminum during simultaneous rapid thermal diffusion

Experimental procedure

This study was carried out on a p-type material (1-10 Ω.cm, CZ, <100>, 500 µm thick. The polished front surfaces of the samples were coated by an undoped spin-on glass (SOG) films provided from

Filmtronics Co (USA) at a spin-on velocity of 3000 rpm in order to have a 200 nm thick layer after a drying at 200°C for 15 min. An aluminum layer, 1 µm thick was evaporated on the half part of the backside of each sample as indicated in Figure 10.

All samples were annealed in argon at temperatures ranging from 700 to 1000°C by steps of 50°C for 25 seconds in a JIPELEC lamp furnace. The furnace characterizations are equivalent as mentioned in Figure 1. The temperature T_{Si} of the sample is measured by a calibrated pyrometer on the bare silicon backside without aluminum. Rapid thermal processing as shown in Figure 10 makes sure that the incident energy from the lamps is the same on the whole surface of the sample at a given temperature T_{Si}.

Phosphorus doped spin on glass

Phosphorus doped P-SOG films were deposited on the front surface of the samples and annealed at the same condition as described above. The doped oxides were then removed and the sheet resistance measured using the four points probe method.

Figure 11 shows the sheet resistance values as measured on P-SOG coated and RTA treated samples as a function of temperature T_{Si}. The sheet resistance of the P-SOG/Si/Al region are systematically lower than those measured in the P-SOG/Si areas. This behavior was observed elsewhere [v,vi,vii] and is explained by phosphorus diffusion enhancement during co-diffusion of P and Al.

This behavior was not observed during co-diffusion in a classical thermal furnace and therefore an increase of the temperature in the P-SOG/Si/Al structure could also be the cause of this phosphorus diffusion enhancement. The difference in temperature between the two regions is expected to increase when increasing the diffusion temperature. It is estimated about 25 and 50°C for annealing temperature of 800 and 950°C respectively.

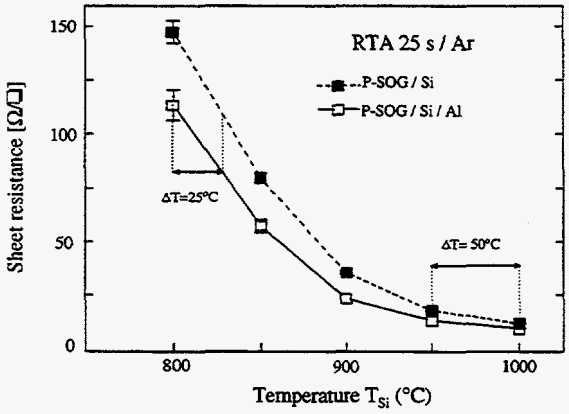

Figure 11: Sheet resistance values versus T_{Si} after phosphorus diffusion from P-SOD source.

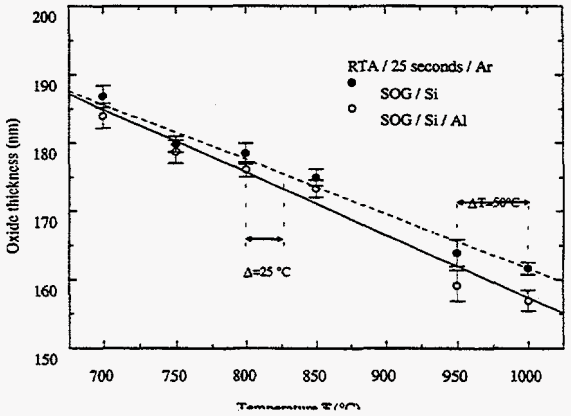

Figure 12: Evolution of the oxide thickness versus T_{Si}.

Undoped spin on glass

To clarify this point, we have carried out a similar experiment as above but using simply an undoped SOG layer instead of a phosphorus doped SOG film. The oxide film thickness decreases with increasing temperature because of the chemical reaction which converts silanol of the SOG film in silicon dioxide[x,xi]. Therefore a difference in oxide densification should be observed if a simple thermal effect takes place. The oxide thickness after processing was measured on both parts of the samples using ellipsometry with an accuracy of 5%.

Figure 12 reports the oxide thickness values measured on the rapid thermal annealed samples. The oxide thickness measured on the SOG/Si/Al structure is systematically lower than those measured on the SOG/Si structure. As the densification of the SOG film is assumed to be only temperature dependent, the difference in film thickness suggests that the temperatures in the two regions are different with $T_{Al} > T_{Si}$ (see Figure 10 notations). Moreover, the temperature difference $T=T_{Al}-T_{Si}$ is seen to increase with increasing the processing temperature. Another remarkable feature is that the ΔT values deduced from

Figure 12 are consistent with those observed in Figure 11; i.e. ΔT=25 and 50°C for T=800 and 950°C respectively. This result shows that the phosphorus diffusion enhancement observed for the P-SOG/Si/Al structure can only be explained by a thermal effect, rather than other considerations.

Discussion and theoretical approach

Three reasons can be put forward to explain the increase in temperature and therefore to explain the increase of the total amount of absorbed energy: (1) The IR light confinement due to the high reflectivity of the Al and Al-Si eutectic. (2) The difference in heat transfer by convection between the Al-Si eutectic/Ar gas interface and the silicon/Ar gas interface. (3) The difference in surface emissivity between the Si and the Al-Si eutectic which could lead to a heat confinement in the SOG/Si/Al structure.

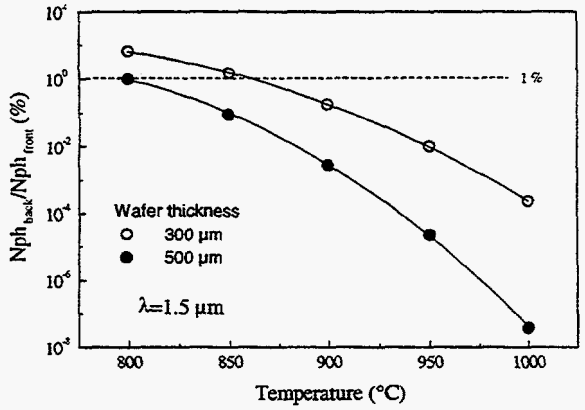

Figure 13: Calculated ratio of the number of photons at λ=1.5µm reaching the backside by the number of incident photons at the front side, versus the annealing temperature and for two different wafer thickness'.

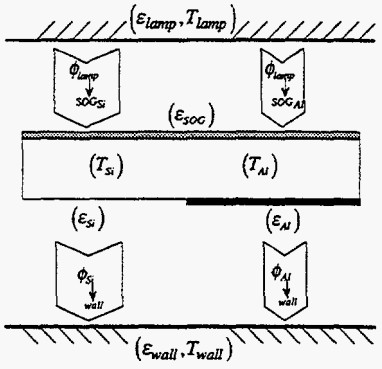

Figure 14: Physical representation of the heating system in terms of net radiated energies, temperature and emissivities

IR light confinement

The spectra of the halogen lamps is ranging from 0.3 to 3.5 µm. The absorption coefficient of silicon at the processing temperatures passes through a minimum value located around 1.5 µm [viii,ix]. The penetration depth of light is then maximum at this wavelength. Using Lambert's law, we have reported in Figure 13 the ratio of the number of photons which cross the whole silicon sample by the number of incident photons versus the annealing temperature T_{si} and for two wafer thickness. The reflectivity at the front surface was neglected.

It is clear from Figure 13 that a few photons (less than 1 % at 800°C for a wafer thickness of 500 µm) will reach the Al layer. These values are even much lower at higher temperature ($<10^{-4}$% at 950°C). This means that quasi no light is reflected on the Al-Si eutectic layer during the thermal treatment. Therefore the contribution of light confinement cannot explain the temperature increase in the Si material in presence of Al on the backside.

Heat transfer by convection

The heat transfer by convection depends on the temperature of the ambient gas, on its flow rate and on the processed material. In our case, the gas is in contact with a silicon surface in solid phase as well as with an Al-Si eutectic in liquid phase. The net heat transfer is expected to be different in both cases. Therefore, we conclude that convection phenomena are of lower order in this observed effect.

Impact of the emissivity

The heating furnace shown on Figure 10 can be modeled by two parallel and uniform surfaces characterized by the set of parameters $(\varepsilon_{lamp}, T_{lamp})$ and $(\varepsilon_{wall}, T_{wall})$ as indicated on Figure 14. The emissivity is a physical parameter with great importance as it governs together with temperature, the

transfer of the radiated energy between bodies. The net radiated energy exchanged between two parallel surfaces characterized by the set of parameters (ε_1,T_1) and (ε_2,T_2) is given by the relation:

$$\Phi_{1\to 2} = \bar{\varepsilon}\sigma\left(T_1^4 - T_2^4\right) \qquad (1) \text{ with } \bar{\varepsilon}: \ \bar{\varepsilon} = \frac{\varepsilon_1\varepsilon_2}{1-(1-\varepsilon_1)(1-\varepsilon_2)} \qquad (2)$$

σ: Stefan Boltzmann constant in $Wm^{-2}K^{-4}$, T_1, T_2 : Temperature in Kelvin.

The emissivity of the cold wall (written ε_{wall}) is expected to be low because of the high reflectivity of the stainless steel. The Al emissivity is also known to be low with values ranging from 0.05 to 0.2 depending on the optical treatment of the layer, while the silicon emissivity is quite high with values in the range 0.6-0.7 [viii,xii]. The emissivity at the front surface (written ε_{SOG}) is also high because of the presence of the SOG film which reduces the reflection coefficient. The energy losses are then reduced when the aluminum is present.

Consequently the phosphorus diffusion enhancement could be attributed to a difference in emissivity between the silicon surface and the surface covered by the aluminum layer. By lowering the back surface emissivity we reduce the radiated energy losses and therefore we confine the heat in the sample leading to an increase of temperature.

Conclusion

In a first part of this work, an impact of the short wavelengths of the lamp spectrum on Rapid Thermal phosphorus diffusion into silicon could be shown. The observed acceleration is more due to an effect in the deposited spin-on dopant glass or the oxide/silicon interface, than an effect in the silicon volume itself. Further experimental and theoretical analysis are planned to deepen the understanding of this diffusion enhancement.

A second part, was dedicated to an observed diffusion enhancement of phosphorous into silicon during Rapid Thermal co-diffusion with aluminum on the back side of the sample. It could be shown that the reduction of emissivity due to the presence of aluminum, induce an optical heat confinement, resulting in a higher sample temperature. This thermal variation is made responsible for the observed diffusion enhancement.

Concluding, optical effects are playing an central role in Rapid Thermal Diffusion mechanisms. Further analysis and experiments are needed to understand in a deeper way the origins and allow precise applications in the solar cell or micro-electronics industry.

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RECENT EXPERIMENTAL AND THEORETICAL RESULTS FOR H_2 IN Si

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Abstract

Recently, there has been great progress made toward understanding molecular hydrogen in Si. The vibrational modes of two hydrogen dimers, interstitial H_2 and an alternative configuration called H_2*, have been identified. There have also been several new theoretical studies which help to elucidate the properties of these hydrogen dimers and their interactions with other defects. This paper is a brief survey of these results.

1. Spectroscopy of hydrogen dimers in c-Si: Success at long last

1.1. Introduction

Isolated hydrogen in Si is mobile below room temperature (i.e., near 200 K)[1.1, 1.2] so at room temperature, H in semiconductors is bonded to other defects or present in the form of H_n aggregates. The smallest H_n aggregates involve just two hydrogen atoms. Two possible hydrogen dimers have been considered theoretically and may play an important role during hydrogen indiffusion and in a variety of hydrogen reactions. However, until recently these hydrogen dimers had not been observed spectroscopically so that their structures or their role in defect reactions might be studied. The first is the hydrogen molecule, H_2, that has been predicted to lie at a tetrahedral interstitial site in Si.[1.3-1.5] Molecular hydrogen is believed to be a slow diffusing species Si and has often been invoked as the product of reactions that release hydrogen from other defect complexes. The second is an alternative configuration for H_2 that has been named H_2*.[1.3, 1.6, 1.7] After several unsuccessful attempts over the years and an interesting recent false start, the hydrogen-stretching vibrations of H_2 and H_2* have been identified.

1.2. H_2 in Si

The stretching vibration of an H_2 molecule in the gas phase does not give rise to an oscillating dipole moment and is therefore infrared inactive. However, Raman spectroscopy can be used to study the stretching vibration of an H_2 molecule. In a Raman study by Murakami *et al.*,[1.8] a broad vibrational band was observed at 4158 cm^{-1} at room temperature for Si samples treated in a hydrogen plasma at 400°C. When Si samples were exposed to a deuterium plasma, a band at 2990 cm^{-1} was observed. These vibrational frequencies are close to those observed previously for H_2 and D_2 in gas, liquid and solid phases, and led to the assignment of the 4158 and 2990 cm^{-1} bands to isolated H_2 and D_2 trapped at tetrahedral interstitial sites in Si. The rationale for the assignment[1.8, 1.9] is as follows: Exposure of a Si sample to a hydrogen plasma at a temperature near 250°C gives rise to extended platelet defects that give rise to Si-H Raman and infrared absorption bands near 2100 cm^{-1} (refs. 1.10, 1.11). Murakami *et al.* found the new band at 4158

cm^{-1} in Si that had been exposed to an H_2 plasma at higher temperatures where it was argued that platelet formation was suppressed and that isolated H_2 molecules were formed.[1.8, 1.9]

In further studies, the assignment of the 4158 cm^{-1} band to isolated H_2 at a tetrahedral interstitial site has been contested. Leitch *et al.* have found that the 4158 cm^{-1} band has the same annealing behavior as the 2100 cm^{-1} Raman bands assigned to platelets and proposed that the 4158 cm^{-1} band is due to H_2 gas molecules trapped in the platelet defects.[1.12] These authors find that plasma exposure at elevated temperature (400°C) does give rise to a stronger 4158 cm^{-1} band, similar to the results of Murakami *et al.*,[1.8, 1.9] but suggest that H_2 molecules become mobile at elevated plasma-exposure temperatures and readily migrate and become trapped by the platelets.[1.12, 1.13]

Leitch *et al.*[1.13] have also found a new Raman band at 3618 cm^{-1} (10K) that is produced by plasma exposure at 150°C. It was argued that the isolated H_2 molecules are not mobile enough to become trapped at platelet defects for this lower plasma exposure temperature. Raman spectra measured by Leitch *et al.*[1.13] of Si that had been exposed to hydrogen and deuterium plasmas are shown in Fig. 1. In (a) and (b) the weak lines assigned to isolated H_2 and D_2 molecules are seen (3610 and 2622 cm^{-1} at room temperature). In spectrum (b), a stronger line at 2990 cm^{-1}, first observed by Murakami *et al.*[1.8] and now assigned by Leitch *et al.*[1.12, 1.13] to D_2 gas that is trapped within platelet defects, is also present.

Theoretical calculations[1.14-1.16] performed for H_2 at a tetrahedral interstitial site in Si find that the H_2 stretching frequency should be shifted to a value lower than the gas phase value by more than 500 cm^{-1}. These results support the assignment by Leitch *et al.*[1.13] of the 3618 cm^{-1} band to isolated H_2 and also the assignment of the 4158^{-1} band seen by Murakami *et al.*[1.8] to H_2 gas molecules trapped in extended defects created by the hydrogen plasma exposure. It is important to note that while the assignment of the 4158 cm^{-1} band to *isolated* H_2 by Murakami *et al.*[1.8] is now believed to be incorrect, it was this work that initiated the recent activity on H_2 in Si. Furthermore, the H_2 gas trapped in platelets is also an important species for understanding hydrogen reactions in Si.

Surprisingly, infrared absorption bands have also been observed independently by Pritchard *et al.* for interstitial H_2 and D_2 in Si.[1.17, 1.18] For these experiments the hydrogen was introduced by annealing Si at elevated temperatures ($1000<T<1300$°C) in H_2 gas. Two bands at 3789 and 3731 cm^{-1} were assigned to H_2 molecules trapped in the vicinity of interstitial O impurities.[1.17] A third band at 3618 cm^{-1}, also reported in ref. [1.17], was subsequently assigned to isolated H_2,[1.18] in agreement with the Raman study of Leitch *et al.*[1.13] The vibrational absorption bands associated with H_2 are roughly 100 times weaker than would be expected for an allowed local vibrational mode. The presence of a weak vibrational absorption line for the H_2 center led Pritchard *et al.* to conclude that the H_2 lies along a lattice direction that removes the inversion symmetry of the molecule.[1.18]

Pritchard *et al.*[1.19] have also begun studies of the reactions of H_2 molecules with other defects and impurities. It had been known that there was a "hidden" source of hydrogen that could be released during low temperature (~175°C) anneals and interact with other impurities.[1.20] This hidden hydrogen is now attributed to H_2 molecules.[1.19]

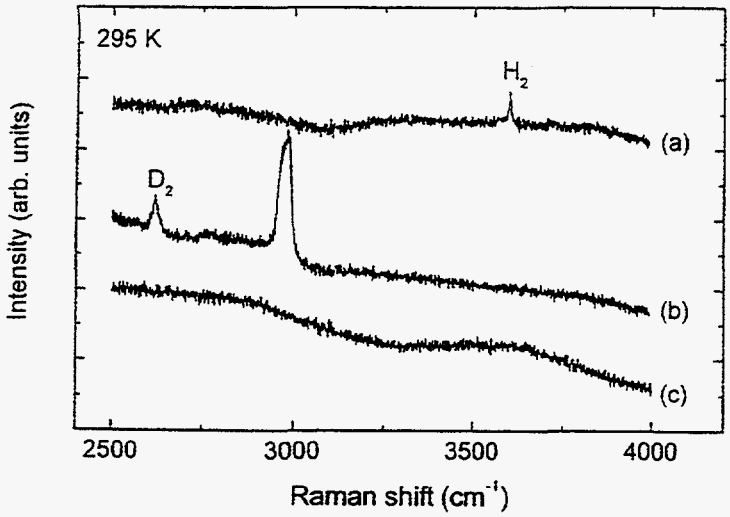

Fig. 1. Room temperature Raman spectra of Si after exposure to (a) an H_2 plasma, (b) a D_2 plasma, and (c) no plasma for reference. From ref. [1.13].

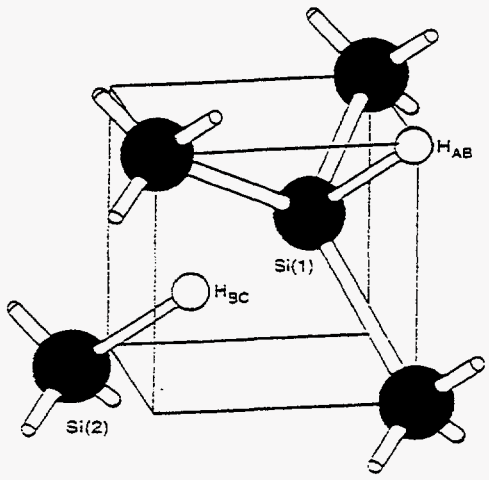

Fig. 2. Configuration of H_2 in Si. From ref. [1.23].*

1.3 H_2* in Si

An alternative configuration for a hydrogen dimer named H_2* has been examined in several theoretical calculations.[1.3, 1.5, 1.6, 1.21] The H_2* defect in Si has been predicted to consist of one hydrogen atom at a BC site between two Si neighbors and a second hydrogen atom bonded to one of these Si neighbors at an antibonding site (Fig. 2).

It has been known since 1975 that implanting protons into Si gives rise to numerous hydrogen-related vibrational absorption bands.[1.22] Recently, several of these bands have been assigned to the H_2* defect.[1.23] From a comparison of the experimental frequencies to a theoretical calculation for H_2*, the vibrational lines at 2062 and 1838 cm^{-1} have been assigned to the stretching modes of hydrogen atoms at the BC and antibonding sites, respectively. A line at 817 cm^{-1} has been assigned to the wagging mode of the hydrogen atom at the antibonding site. H_2* has been proposed as a possible configuration for hydrogen in Si that might diffuse more quickly that H_2.[1.3, 1.6, 1.24] At present the mobility of H_2* has not been established.

The electron irradiation of Si that contains hydrogen, presumably in the form of interstitial H_2 molecules, is known to produce the H_2* defect.[1.20, 1.25] H_2* does not contain vacancy or interstitial defects that are produced by the irradiation, making the formation of H_2* from H_2 and native defects difficult to understand. Now, with spectroscopic signatures known for H_2, H_2* and several vacancy- and interstitial-H_n complexes,[1.26] the complicated interactions of hydrogen with vacancies and interstitials have the potential to be understood.

2. Theoretical studies of hydrogen dimers in c-Si

2.1. Introduction

Theorists have predicted that two hydrogen dimers are stable in Si long before they had been experimentally identified. The two dimers are the interstitial H_2 molecule[2.1] and the H_2^* pair.[2.2] In the latter complex, one Si–Si bond is replaced by two inequivalent Si–H bonds on the same trigonal axis. The first H is near the bond-center (BC) site bound to one Si atom, and the second H is anti-bonding to the other Si atom (for a review of the theory, see Ref. 2.3). Both dimers have now been experimentally identified (see Refs. 2.4-2.5 for H_2 and 2.6 for H_2^*). Large concentrations of H_2 molecules in Si can be obtained following plasma exposure[2.4] or by quenching a crystal grown in a hydrogen ambient or exposed to an H_2 gas near the melting point of Si.[2.5] On the other hand, H_2^* has only been seen in irradiated material[2.5] and anneals out[2.5] at 200 °C.

Theorists agree that the H_2 molecule is stable at (or near) the tetrahedral interstitial (T) site. Various authors differ on the lowest-energy orientation. In the most recent studies, it is predicted to be along the $< 110 >$ (Ref. 2.7) or $< 100 >$ directions (Refs. 2.8-2.9). However, theorists agree that its activation energy for rotation is very small (less than 0.1 eV), and for diffusion, it is of the order of 0.8 to 1.0 eV. There is no consensus as to which of H_2 or H_2^* is the more stable, but theorists always predict them to be within a few tenths of an eV.

2.2. Defect-induced dissociation of H_2

We have studied[2.9,2.10] the interactions between H_2 and the vacancy (V), the self-interstitial (I), and the ring-hexavacancy.[2.11] The results summarized below have been obtained with the 'ab-initio tight-binding' molecular-dynamics (MD) simulations technique developed by Sankey and co-workers.[2.12] The electronic problem is solved using the density-functional theory with either the Harris energy functional or a (slower but more accurate) fully self-consistent scheme.[2.13] The host crystal is represented by periodic supercells (typically 64 Si atoms) and the time step varies from 0.2 fs to 2.0 fs depending on whether H is present in the calculation or not. The methods allows constant-temperature simulations lasting up to a few picoseconds as well as fast or slow quenches leading to local or global minima of the potential energy surface, and therefore to potential energy differences.

The equilibrium concentrations of V's and I's in Si are low.[2.14] However, these defects diffuse rapidly through the material in above-equilibrium concentrations during processes such as ion implantation, etching, deposition of surface layers (Al back-contacts, n^+ layers, anti-reflection coatings), etc. Both V and I interact readily with each other, with impurities, and with other defects. These interactions often affect the electrical and optical properties of the material.

MD simulations predict that isolated interstitial H_2 is stable in defect-free Si. However, if placed inside a vacancy or even the much larger ring-hexavacancy, it spontaneously dissociates. H_2 cannot remain molecular so close to weak or reconstructed Si–Si bonds.

We then considered the situation where H_2 is near but outside V or I. When V (or I) and H_2 are at a large separation d, the only possible configuration is H_2 plus V (or I). As d becomes smaller, deeper minima of the potential surface become accessible. They correspond to configurations with two Si–H bonds near or at V (or I). When d is very small, the energy barrier separating the molecular from the dissociated states disappears, H_2 melts, and the two H's may participate in the defect (at lower temperatures) or escape as isolated interstitials (at higher temperatures).

These calculations are performed as follows. We begin with H_2 and V (or I) at third-NN sites and quench. This guarantees that our starting configuration is a local minimum of the potential energy. Then, we raise the temperature (300 to 1000 K) in order to allow the defect to react with H_2. We always end up with a dissociated molecule and a substantial reduction in potential energy. The gains in energy come from the formation of two Si–H bonds and a reduction of the strain associated with the original defect.

The potential energy difference between V infinitely far from H_2 and $\{V, H, H\}$ is $4.0eV$. The lowest-energy configuration of $\{V, H, H\}$ has two Si-H bonds with both H atoms pointing toward the center of the vacancy.[2.15] The potential energy difference between I infinitely far from H_2 and $\{I, H, H\}$ is $1.7\ eV$. The lowest-energy structure of this defect is a split-$< 110 >$ configuration with one H bound to each of the two split Si atoms.[2.16] We obtained a metastable configuration of $\{I, H, H\}$, $0.4\ eV$ higher in energy. It has I at a puckered BC site with both H bound to it.

Our calculations imply that interstitial H_2 is stable only when it is surrounded by perfect or near-perfect Si–Si bonds. If H_2 is near stretched, distorted, or otherwise weak Si–Si bonds, it dissociates with a substantial gain in energy. The result is the formation of two Si–H bonds and a reduction of the strain associated with the defect. The further H_2 is from strained Si–Si bonds, the longer it remains in molecular form.

Several experimental results can be explained with our predictions. *(i)* In proton-implanted samples, the $\{I, H, H\}$ complex has been observed[2.16] but not the simpler $\{I, H\}$ complex. This suggests that I's may often be interacting simultaneously with *pairs* of H atoms. Our results show that the interaction of I with H_2 leads to the complex observed. *(ii)* Si samples grown in an H_2 ambient contain high concentrations of hydrogen. Such samples have been electron-irradiated and studied by FTIR.[2.17] Before irradiation, only a few, weak, Si–H lines are seen. After irradiation, a very dramatic increase in the number and amplitude of the IR lines is observed. This implies that the hydrogen present in the material changed from an IR-inactive state to an IR-active one, where many Si–H bonds are seen. These observations can be understood if H_2 interstitials are dissociated by the rapidly diffusing V's and I's generated by the irradiation.

2.3. Formation of H_2^*

Our calculated formation energies for V and I are 4.0 and $4.2\ eV$, respectively. The calculated Frenkel pair formation energy is therefore $8.2eV$. This amount of energy is much

larger than the gain from the reactions $V + H_2 \rightarrow \{V, H, H\}$ $(4.0\,eV)$ or $I + H_2 \rightarrow \{I, H, H\}$ $(1.7\,eV)$. This suggests that, given a sufficient amount of V's and/or I's, further reactions may take place.

Ron Newman suggested that the H_2^* complex, only seen in irradiated material,[2.5] results from the reactions $\{V, H, H\} + I \rightarrow H_2^*$ or $\{I, H, H\} + V \rightarrow H_2^*$. We have tested these possibilities. We started an MD simulations with a (quenched) configuration that combined $\{I, H, H\}$ (or $\{V, H, H\}$) and V (or I) at a third-NN site in the same cell. After 4,000 times steps, $\{I, H, H\} + V$ did produce H_2^* but $\{V, H, H\} + I$ did not react under the same conditions. We believe that the latter reaction does occur but requires much longer simulation times than computationally tractable.

3. Conclusion

The hydrogen-stretching vibrations of interstitial H_2 and an alternative dihydrogen complex, H_2*, have been observed in Si by Raman and infrared absorption spectroscopies. These results confirm the long standing hypothesis that molecular hydrogen is an important and often present species in Si. The discovery of a spectroscopic fingerprint for these hydrogen dimers opens up promising new avenues for experimental studies of the interaction of hydrogen with other defects and impurities in Si. Several new theoretical studies of hydrogen molecules and their interactions with native defects have already been reported.

In this survey, we have focussed on the hydrogen dimers H_2 and H_2* whose vibrational spectra have been identified. Photoluminescence spectra have also been reported for two additional hydrogen dimers in crystalline Si that have trigonal symmetry [A.N. Safonov, E.C. Lightowlers, and G. Davies, Phys. Rev. B **56**, 15517 (1997)]. At present, it is not known whether these hydrogen dimers are related to the H_2 and H_2* complexes discussed above, showing that there may be addtional hydrogen dimer species in Si and that there is still much about H_2 complexes in Si that is not well understood. We expect that exciting new experimental and theoretical results for H_2 in semiconductors will continue to appear during the next few years.

Acknowledgments

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Thin Film Si Solar Cells: A Review of Material Issues and Device Design Concepts

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ABSTRACT

Thin-film Si solar cells offer many advantages, including a lower cost, the potential for high efficiency with lower-quality material, and use of smaller quantities of silicon. However, there are a number of challenges in making such a device. These challenges arise from both the design and the fabrication process(es) of the device. A major issue in the device design is that Si is an indirect bandgap material that requires thick wafers to absorb a significant part of the sunlight. The solution to this problem is a method for efficient light trapping that is compatible with a low-cost cell design. Our calculations have shown that a film thickness of about 10 μm is sufficient to yield photocurrent densities of 35 mA/cm^2 in fairly simple device structures. The other aspects of device design are related to the carrier collection approaches such as the nature of junction(s), electrode geometry, and electronic and optical reflectors. An important consideration in the cell fabrication comes from requirements of low overall fabrication costs. This in turn necessitates the use of inexpensive substrates and high-throughput Si deposition techniques. It is generally perceived that a low-cost substrate is needed to support the thin film. Low-cost substrates generally imply materials that may not be compatible with the high temperatures required for forming and processing Si film. This incompatibility can be caused by impurities in the substrate that can diffuse into the Si film, softening of the substrate, thermal mismatch, and less desirable electronic properties of the interface.

This paper will review requirements and various proposed designs for thin-film Si cells. Various approaches for fabricating such devices in a manner compatible with low-cost, manufacturable processes will be discussed.

Thin Crystalline Si Solar Cell Research Activities in NEDO Sunshine Projects

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1. Introduction

In 1997, the New Energy and Industrial Technology Development Organization (NEDO) in Japan has started a new 4 years' program of Sunshine Project to achieve a technological runaway towards the huge mass production of solar photovoltaic systems in the coming century. The priority subjects of thin film cells such as amorphous Si, crystalline Si, and poly-crystalline CdTe and Cu(In, Ga)(S,Se) have been effectively promoted in the fields of film formation, cell fabrication, and module preparation technologies. Especially, thin crystalline Si cells have been attracted much attentions since relatively high and stable efficiency can be obtained at low costs. In order to realize practical cells and modules in near future, one should solve technological subjects not only in film growth methods but also novel cell fabrication processes. In this report, the latest results in the active projects promoted by NEDO are reviewed and discussed.

2. Advanced Thin Crystalline Si Film Formation Methods and Cells

Table1 Thin Film Crystalline Si cell Activities in Japan

Crystal growth
- Liquid Phase Epitaxy (Daido-Hoxan)
- Chemical Vapor Deposition (NAIST, Mitsubishi)
- Flux method (Kyocera)
- Thin film/Sheet Hybrid (Sharp)

Cell production
- ZMR (Mitsubishi)
- Single Crystalline Si seperated by porous-Si (Sony)
  - Delamination by H^+ implantation (Ion Engineering Institute)

Novel Structures
- STAR structure on glass (Kaneka)
  (naturally Surface Texture and enhanced Absorption with back Reflector)
- Solid Phase Epitaxy (Sanyo)

The research activities relating with thin crystalline Si cells are classified in Table 1. Several technologies for film growth are investigated using not only conventional liquid phase epitaxy, and/or chemical vapor deposition, but also novel flux method and Si sheet growth. Daido-Hoxan developed [1] a new carbon substrate with the almost same thermal expansion coefficient as Si, and achieved polycrystalline Si films with relatively large grain size (0.5 - 3.0 mm). These fundamental investigations should be carried out continuously in order to reveal the film growth mechanisms on foreign substrates for the future practical applications.

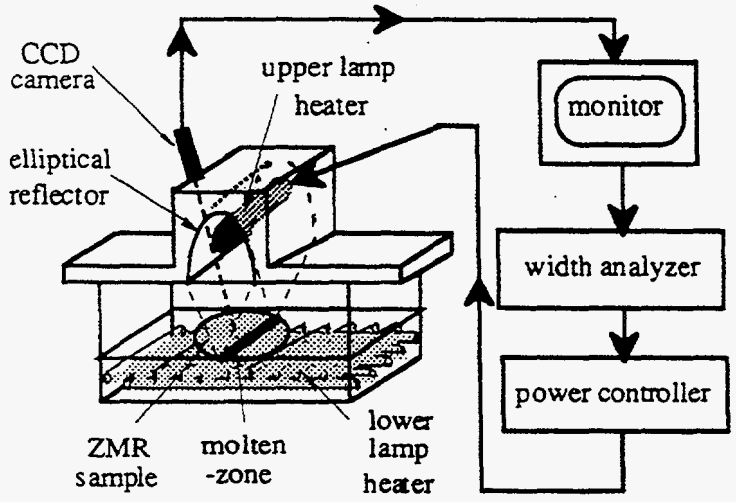

Fig.1 Zone-melting recrystallization (ZMR) apparatus

Polycrystalline Si cells with high efficiency have been realized using zone-melting recrystallization (ZMR) technique by the Mitsubishi group [2,3]. The key factor to get high quality seed layers was found to be in the control of molten zone as shown in Fig.1. Precise feedback using CCD camera images of the boundaries of a molten zone gave low defect densities in the order of 10^6 cm^{-2} at a high scanning speed of 5.0 mm/sec. The highest efficiency of 16.0 % (588.7 mV, 35.6 mA/cm^2, 0.763) was obtained for a cell size of 100 cm^2 with a typical epitaxial layer thickness of 80 μm. To get high throughput of epitaxial growth on a seed layer, a multi-wafer CVD reactor was developed. More than 20 wafers could be set at one time. Preliminary growth conditions yielded uniform epitaxial layers at a growth rate of 5 μm/min with a source gas utilization efficiency of around 50 %.

A novel technology to fabricate single crystalline Si thin film cells on plastic substrates has been developed by Sony Corp [4]. The process sequence was shown in Fig.2. A unique structure of porous Si layers was formed by a devised anodization sequence. High quality Si epitaxial layers with a thickness of 10 μm could be grown on porous Si surfaces using a conventional CVD process. After processing of junction formation and electrode deposition, etc., a fabricated cell was transferred to a plastic film utilizing a high porosity Si layer as a separation layer. Epitaxial Si layers

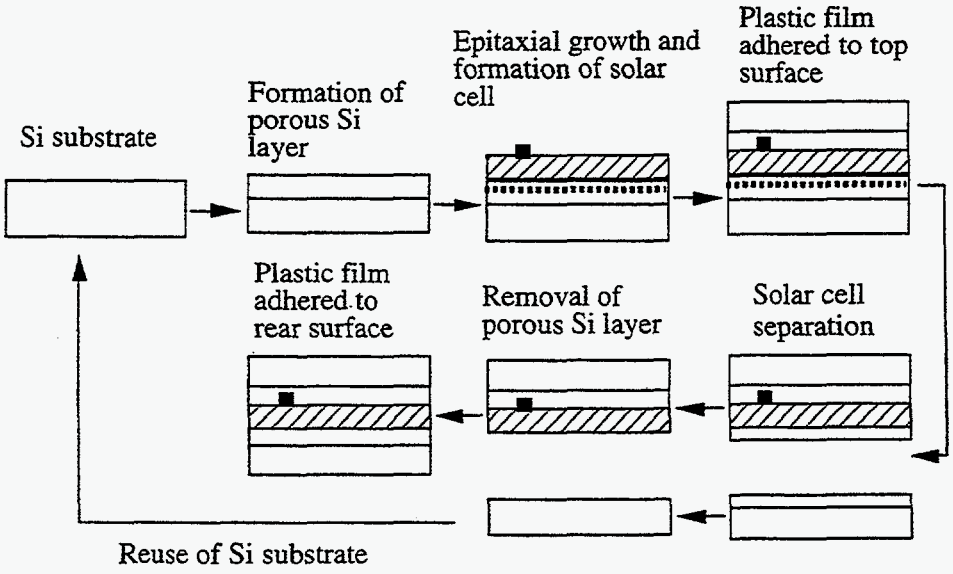

Fig.2 Cell fabrication sequence using porous Si as a separation layer

with a carrier density of 4×10^{16} ~ 4×10^{17} cm^{-3} had a long minority carrier lifetime of about 60 μs or more estimated by the microwave photoconductivity decay method. The porous Si layer might act as not only separation layer but also gettering sites of metal impurities. The maximum separated area was 50 cm^2 (8cm ϕ). The substrate was expected to be used repeatedly, which reducing material amount and cost effectively. Preliminary cell with a area of 4 cm^2 showed a relatively high efficiency 12.5 % (623 mV, 25.5 mA/cm^2 , 0.790), which demonstrated the feasibility of single crystalline thin Si cell as a promising candidate for a high efficiency and low-cost solar cell.

A novel STAR (naturally Surface Texture and enhanced Absorption with back Reflector) structure cell on glass has been investigated by Kaneka Corp [5,6]. Very thin polycrystalline Si layers could be deposited on seed layers crystallized by laser annealing. A high intrinsic efficiency of 10.7 % (aperture 10.1 %) could be realized with a cell area of 1.2 cm^2. It should be noted that a high short circuit current of 26.6 mA/cm^2 could be achieved with an active layer thickness of only 2 μm, which showed high electronic properties and effective light trapping. Taking into account of the numerical analyses of cell performances, long diffusion length (7 ~18 μm) and high front internal reflectance of 70 % were estimated. A stacked structure of poly-Si/amorphous-Si tandem cell showed a stabilized efficiency higher than 11 %, and practical applications for large area modules are now investigated.

3. Conclusion

Crystalline (poly- and single-) Si thin film cells have been attracting much interests as high efficiency and low cost cells in the coming century. In the NEDO Sunshine Projects, many activities have been intensively investigated in these years. Not only the fundamental approaches of film depositions on foreign substrates but also challenging trials of cell fabrications using novel

techniques have been developed so far. The achieved latest results have demonstrated the expecting feasibility of crystalline thin Si cells in future.

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HIGH TEMPERATURE SUBSTRATES FOR THIN FILM POLY-SI ELECTRONICS

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1. Introduction

Thin film silicon solar cells exploring light trapping need only to be a few microns thick to absorb most (80%) of the incident light [1]. If designed to collect from depleted regions, the poly-Si thin film cell becomes largely insensitive to crystalline defects such as grain boundaries and dislocations and can achieve a high conversion efficiency [2]; offering an attractive alternative to a-Si:H, III-V, or column VI based thin film solar cells.

A crucial issue for the *low cost* production of such cells is how to deposit, in an economical manner and using standard processes, the very thick (by IC standards) poly-Si films needed.

The standard Si processing steps of deposition, oxidation, diffusion need temperatures of 800 to 1000 C to operate effectively. This, and the increase in grain size of CVD poly by a factor 6 between 700 C and 1100 C [3], make it highly desirable to process the poly-Si thin film cell at elevated temperatures, between 900 and 1000 C.

The highest temperature at which commercially available glass substrates matching the coefficient of thermal expansion, CTE, of Si can be processed is about 620 C. No low cost substrate is currently available capable of withstanding temperatures up to 1000 C and matching the CTE of Si. But glass-ceramics are poised to fill this void.

2. Chemical Vapor Deposition of thick poly-Si films.

The most compelling argument for using a high temperature substrate is the increased deposition rate achievable in atmospheric pressure chemical vapor deposition, APCVD; an established and economical deposition technique that lends itself well to the continuous operation to required to fabricate solar cells at low cost.

The deposition rate of the gases used in CVD (SiH_4, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$) increases exponentially with temperature, $\Delta H = 1.6$ eV [4] until the mass transport limited regime is reached. The temperature at which the rate saturates varies somewhat with reactor design and operation conditions but typically is about 850 C for silane and 1100 C for $SiCl_4$. In the mass controlled regime, the deposition rate is one the order of 1μm/min, permitting to deposit a 20 μm thick solar cell in about 20 minutes.

3. Substrate requirements

A suitable substrate must meet a host of requirements of which the ability to withstand temperatures up to 1000 C, and to match the thermal expansion coefficient of Si are the

most important ones. For cells using the substrate as cover glass, it is important that the substrate is highly transparent and that antireflex features can incorporated, at low cost, into the substrate.

A high chemical stability is desirable since acids are used during cell processing. Good mechanical properties (a high Young's modulus, and high fracture strength) are very important in mass production as breakage not only decreases yield but may require to shut down equipment to clean out fragments.

Economical constraints on substrates are the necessity to use low cost ingredients, and low cost fabrication methods, which in turn, translate into materials specification. For example, the use of the fusion draw process, which yields glass substrates of exceptional surface finish without polishing, sets constraints on the high temperature viscosity, which in turn limits the compositions that can be used.

4. Available substrates

i. Glass

Corning Code 1737 is a specialty glass developed specifically for a-Si:H thin film electronics. This glass, a follow-up on Corning Code 7059, is fabricated using the fusion draw process and is used in the majority of active matrix flat panel displays fabricated world-wide.

The highest temperature at which Code 1737 can be processed for extended periods, say hours, is 620 C . While this temperature far exceeds the requirements of a-Si:H based thin film electronics, it is marginal for the fabrication of poly-Si films and insufficient to achieve, using conventional gases and equipment, the high Si deposition rates required for low cost production.

Glasses capable of being processed at 1000 C have been made at Corning Inc. and GEC (UK) [5] but have not been put into production. In general, glasses with high strain points are difficult to fabricate.

The GEC glass was used by Bergmann et al. to deposit, via $SiHCL_3$ APCVD at 1000 C, up to 35 μm micron thick, p-doped, poly-Si films at a rate of 1 μm/min [6]. The average grain size was 1.26 μm, and the hole mobility, μ(p), 37cm^2/Vs at a carrier concentration of 7E17/cm^3. In lower doped films, with a Hall carrier density of 1E16/cm^3, the hole mobility fell to "a few cm^2/Vs"; suggesting that intrinsic material, required in some cell designs, may have an even lower mobility.

Hydrogenating the highly doped material improved its hole mobility to 68 cm^2/Vs. The minority carrier (electron) diffusion length was around 2 μm, reaching a maximum of 3.1 μm in a 20 μm thick film.

No diffusion barrier was inserted between the glass and the poly-Si. Our experience with glass ceramics, described below, suggests that some of the glass constituents may have migrated from the glass into the poly-Si film, altering its electronic properties.

ii. Glass Ceramics

Glass ceramics are formed by heating glass to which a nucleation agent, such as Titania, was added. This permits to form the material as a glass - e.g. an antireflex coating can be rolled onto one side - prior to the transformation into the glass-ceramic state which is brought about by a high temperature anneal ('ceraming'). After this transformation, the material consists of a mixture of small crystallites embedded into a continuous, silica rich vitreous matrix.

Glass ceramics were invented at Corning and are sold commercially as "machinable glass" and by Schott - under license to Corning - as high-end electric range tops. The former application exploits the materials high fracture toughness and the latter its ability to withstand high temperatures for prolonged times.

The glass ceramic investigated at Cornell, LGA 139, is an experimental glass ceramic fabricated at Corning Inc. by Dr. L. Pinckney. The material is specifically designed to have a high transparency and to match the thermal expansion coefficient of Si.
The chemical composition is based on the SiO2-Al2O3-ZnO-MgO-TiO2-ZrO2 system. TiO(2) serves both as the nucleation agent and as integral component of the spinel crystals.

In the precursory glassy state, the material has a strain point of about 700 C, which though high, permits all glass forming operations. After transformation into the glass ceramic state, the strain point moves to 945 C and the thermal expansion coefficient increases by some 30% to $35\text{-}40\cdot10^{-7}$/C, matching the CTE of silicon. The transformed material consists of 100 Å crystals of spinel solid solution in highly siliceous residual glass phase. Its strain point, therefore, approaches that of fused silica and quartz materials which require significantly more expensive manufacturing processes. The material is transparent since the crystals are too small to scatter light. The ratio of Ti^{+4} to Ti^{+3} is kept high to suppress color formation. Young's modulus, Knoop hardness, and modulus of rupture of the glass ceramic all are about 20 % higher than those of fused silica [7].

5. Preliminary outdiffusion experiments

Stress test carried out at Cornell on poly-crystalline thin film transistors fabricated at 520 C one a variety of commercial available glass substrates matching the CTE of Si showed that the device life time varied greatly with the substrate material used, see Table 1. The lifetime increased and its variation decreased to one order of magnitude when an intermediate 'barrier' layer of 1000 A of SiO_2 was inserted between the substrate and the device. A hypothesis consistent with these observation, as well as with the chemistry of

Substrate	RCA	1000 Å	5000 Å
Code 1737	0.41 ± 0.05	1.00 ± 0.09	0.44 ± 0.15
Non-US Glass 1	0.20 ± 0.13	0.51 ± 0.03	
Non-US Glass 2	0	0.11 ± 0.07	
Oxidized Si		4.03 ± 1.98	

Table 1: Normalized lifetime of transistors fabricated on different glass substrates, either RCA cleaned or covered with a 1000 or 5000 Å thick SiO_2 barrier layer, stressed by applying 50 V between source and drain. The reference is 1000 Å covered Code 1737.

the glasses, is that during 620 C processing, impurities migrate from the substrate into the device. These observations strongly suggested that at the higher temperatures at which we planned to fabricate our devices on LGA 139, a barrier layer would be needed to eliminate outdiffusion of glass ceramic components.

To investigate such barrier layers, we deposited by CVD onto the glass ceramic a multiple thin film stack consisting of four one 1000 A thick SiO2 layers and three 1000 A thick SiNx layers. The deposition sequence used was SiO2/SiNx/SiO2/SiNx/SiO2/SiNx/SiO2; i.e. both the substrate and the poly-Si channel layer contacted SiO2. (The former is convention, but the latter is required to minimize electron trapping at the back channel interface).

To test for outmigration, the package was annealed for 8 hours at 900 C. The time chosen was twice that of the 4 hr, 900 C treatment required to make the thin film transistors described later.

SIMS was then used to profile the movement of all glass components (Al, Mg, Zn, Ti, Zr, Si) as well as Na. The results obtained are shown in Fig. 1

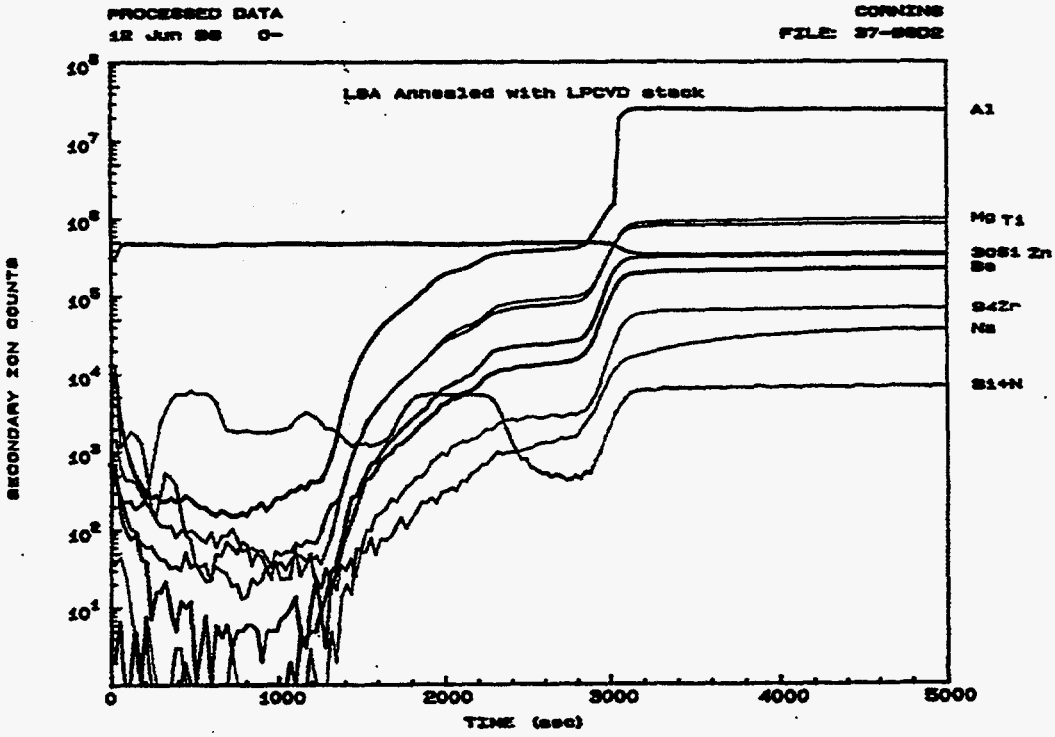

Fig. 1 SIMS Profile of LGA1, covered with a multiple barrier layer consisting of three 100 nm thick nitride layers and four 100 nm thick oxide layers. See text for details

The location of the three SiNx layers is clearly indicated in this figure by the three nitrogen + silicon peaks visible at the left. Note that the first oxide layer (the one in contact with LGA 139) is saturated with glass components at concentrations set by their 900 C solubility. However, the concentration of all glass components, except for Al, decreases within the first nitride layer to values below the detection limit of SIMS. After the second nitride layer, the SIMS signal of all glass components is below the detection limit.

These results indicate :

i) Barrier layers are required
ii) A double nitride layer conservatively meets all requirements.

We are carrying out further experiments on the design of barrier coating, with the aim to minimize the numbers of layers needed.

It is possible that a single nitride layer might suffice, as the particular glass ceramic used had a high surface roughness (500 Å) that, e.g. might increase the pinhole density in the nitride. We are carrying out experiments on chemical- mechanical polished (CMP) glass ceramic wafers, to investigate the influence of substrate roughness on barrier layer performance.

6. Fabrication of Thin Film Transistors

Poly-Si thin film transistors are convenient test vehicles to derive information on carrier mobility and density of trapping states, among others. The process to fabricate such transistors on glass is highly developed at Cornell, and the 'glass' process, therefore, provided a convenient starting point to test the glass ceramics.

On *glass*, fabrication of the self-aligned, 15 x 15 μm transistor starts with the deposition of a 1000 Å thick SiO_2 barrier layer. Next, the 1000 Å thick channel poly is deposited at by LPCVD of silane at 620 C and patterned. The 1000 Å thick gate oxide is deposited at 450 C using diethylsilane (DES). The gate poly is 2500 Å thick and deposited at 620 C. Source drain implant is done using 105 KeV P^+ ions at 1E15/cm^2. Dopant activation is carried out by annealing the device at 600 C for 4 hrs.

The process used to fabricate transistors on a barrier coated *glass ceramic* begins with the deposition of 1000 Å of amorphous Si by LPCVD at 550 C. The gate oxide, 1000 Å thick, is again deposited at 450 C using diethylsilane. The poly gate stack, 2500 Å thick is deposited at 620 C. The P source/drain implant uses 105 KeV P^+ at 1E16 /cm^2. The transistor are then annealed at 900 C for 4 hours to activate the dopant and to convert the channel into poly-crystalline Si.

Fig. 2 compares the device characteristics of thin film transistors made with the above two processes. The device made on the glass ceramic at 900 C has a lower leakage

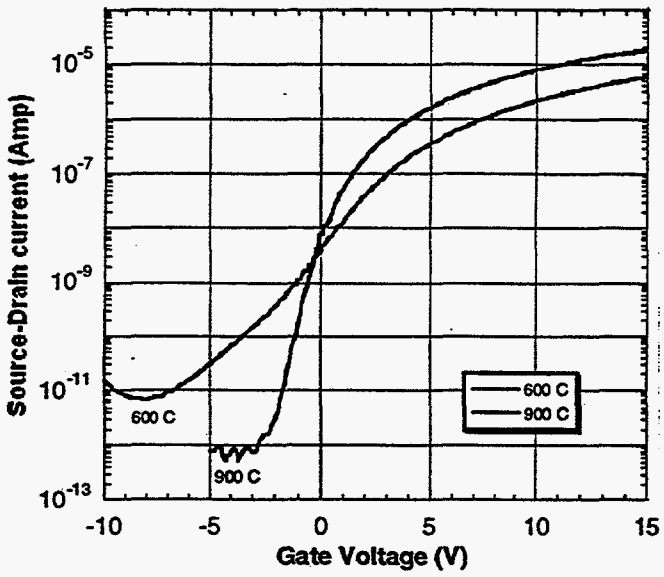

Fig. 2 I_{SD} vs V_g of TFTs made on 1737 (600 C) and on LGA 139 (900 C)

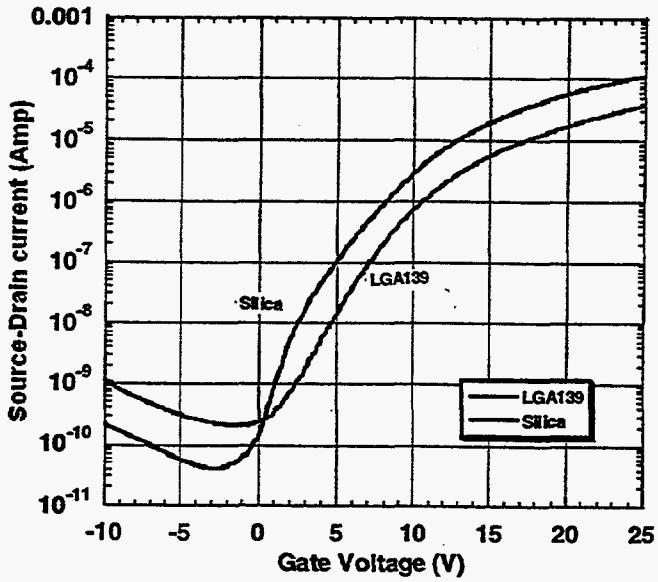

Fig. 3 I_{SD} vs V_g of TFTs made on LGA 139 and, for reference, on fused silica

current, lower threshold, lower subthreshold slope and higher on current, all indicating that the electronic properties of the poly-crystalline material are much better. In particular, the electron mobility is higher by a factor 6.6.

The results of a quantitative analysis using Levison Theory [8] are given in Table 2, which lists the average values for 118 devices made on LGA 1. Note that Levison's theory, which fits poly-Si transistors more accurately than the more simple single crystal MOSFET theory used to fit data in many publications, tends to return lower values for the mobility. This should be kept in mind when comparing data from different groups.

NN8Bx	Vfb	Imin	I0	I15	mu	Qtrap	S	Vth	N	Notes
1	-1.2	231	260	5750814	34.31	5.05	2.19	7.8	118	LGA139
	0.3	23	39	1515035	3.53	0.14	0.15	0.6		
2	-2.9	49	208	19006100	118.25	5.40	1.34	6.6	120	fused silica
	1.1	9	220	8011165	43.17	0.25	0.12	0.7		
3	0.6	45	435	5972658	76.61	5.18	1.90	9.4	120	Si
	0.3	2	3127	3590079	5.90	0.09	0.10	0.2		

Table 2. TFT parameters for transistors made on LGA 139, fused silica and oxidized Si wafers. See text for details.

The columns list, left to right, the flat band voltage, V_{fb}; the current at the flat band voltage, I_{min} in units of pA; the source drain current, in pA, at zero gate voltage; the source drain current, in pA, at a gate voltage of 15 V; the intrinsic electron mobility in cm^2/Vs, the trap density in multiples of $1E12/cm^2$; the subthreshold swing in units of

V/decade; and the threshold voltage. N is the number of devices which were measured. The line below lists the standard deviation of these parameters.

Fig. 3 shows a comparison of the TFT fabricated on the glass ceramic, LGA 1, and on fused silica. The lower performance of the former is most likely caused by the high surface roughness (500 A) of the particular glass ceramic used to process this run. A rough Si/SiO2 reduces the channel mobility [9]. Inspection of Table 3 shows that highest average mobility of 118.25 cm^2/Vs was measured for the 120 TFTs fabricated on polished, fused silica. It is likely that the mobility could be improved further by hydrogenation.

7. Summary

Transparent glass ceramics substrates with thermal expansion coefficient matching that of Si and strain points ~ 945 C were fabricated. SIMS measurements show that the barrier coating applied reduces the outmigration of glass components below the detection limit. Thin film poly-Si transistors were fabricated on these glass ceramic substrates and their properties, averaged over > 100 devices, were measured and compared to those made on two other substrate materials: fused silica and oxidized Si wafers.

The TFTs fabricated on the glass ceramic have properties comparable to those fabricated on the other high temperature substrates. The differences observed are tentatively ascribed to the higher surface roughness (50 nm) of the glass ceramic.

ACKNOWLEDGMENTS

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A Review of Hotwire Deposition of Amorphous and Microcrystalline Si

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Abstract:

I will review progress in the deposition of amorphous and microcrystalline silicon using hot -wire(filament) chemical vapor deposition (HWCVD). This technique, started nearly 20 years ago has seen increased emphasis in the last decade because of rapid deposition of high quality hydrogenated amorphous silicon over a much wider range of deposition conditions than are possible with plasma-assisted chemical vapor deposition (PECVD). Although much of the work with the amorphous phase is directed toward photovoltaic applications, the interest in the microcrystalline material is also for thin film transistor applications.

In this talk I will describe the deposition process and compare the properties of material produced by both HWCVD and PECVD. It is in the amorphous phase where the electronic and structural properties show the most significant differences, that I will emphasis in this talk. However, I will review the present status of the microcrystalline material.

CROSS-CONTAMINATION AS A NOVEL TECHNIQUE FOR STUDYING IMPURITIES IN MULTICRYSTALLINE SILICON

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ABSTRACT: Deliberate cross-contamination of high quality single crystal wafers by effusing impurities from multicrystalline samples is presented as a technique for studying the effect of the impurities on electronic properties. The method allows the impurities to be characterised in isolation from the crystallographic defects of the multicrystalline samples. By fitting simple Shockley Read Hall curves to the lifetime versus injection level data of the deliberately contaminated wafers, the relative concentrations of mobile impurities in the original multicrystalline samples can be obtained. Such information, coupled with a knowledge of the crystallographic quality of the material, allows an understanding of the electronic properties of the substrate, including whether the material will improve after gettering.

1. INTRODUCTION

Recombination processes in multicrystalline silicon are generally more complex than those in single crystal material. The presence of relatively large densities of crystallographic defects, such as grain boundaries, dislocations, and microdefects, as well as atomic impurities, result in lower lifetimes in multicrystalline samples [1-3]. A further complication is introduced due to the interactions between the defects and impurities, such as metallic decoration of microdefects and the gettering effects of dislocations and grain boundaries [4,5]. In this paper we present a technique for physically separating the effects of impurities and crystallographic defects in multicrystalline silicon, allowing the problem to be broken into more easily studied parts.

Many lifetime degrading impurities in multicrystalline silicon, such as transition metals, are highly mobile at typical processing temperatures (900-1000°C). As a result, a small but significant proportion will effuse out of the surface of the samples and into the surrounding gas stream. If clean, high lifetime samples are placed close to these 'dirty' samples, a proportion of the effused impurities will be adsorbed onto the surface of the clean wafer, from where they are free to diffuse into the bulk and consequently degrade the lifetime. The final concentration of impurities in the previously clean sample will increase monotonically with the initial concentration of impurities in the dirty sample. Subsequent analysis of the degraded samples reveals information about the nature of the impurities. Such information is difficult to extract directly from multicrystalline samples due to the obscuring effects of crystallographic defects and their interaction with the impurities.

If the degraded samples are of good crystallographic quality, then it is reasonable to expect that the lifetime will be described by a simple Shockley Read Hall (SRH) model, which states, among other things, that the maximum lifetime is inversely proportional to the impurity density [6]. By fitting SRH curves to experimental data from the degraded wafers, it is possible to infer the relative concentration of impurities in the original multicrystalline samples.

2. EXPERIMENTAL METHODS

The multicrystalline material used in this study came from one p-type ingot which was grown by directional solidification at Eurosolare, SpA. Due to segregation from the solid to liquid phase, the distribution of impurities is expected to vary along the length of an ingot. In addition, contamination from the crucible can occur [7]. Consequently, wafers were selected from four regions, in order to

examine the effect of different concentrations of impurities. The resistivity of the samples varied from 0.8 to 0.9 Ωcm.

To achieve cross-contamination, the multicrystalline samples were sandwiched between two high quality float zone (FZ) wafers, as depicted in Figure 1. The length of the entire quartz boat is about 30cm, whilst the distance between the multicrystalline and the FZ wafers was about 5mm. The wafers were then given a light phosphorus diffusion at 840°C using a $POCl_3$ source for 25 minutes. A thin oxide layer was then grown at 900°C for 30 minutes (including the last 10 minutes in N_2), followed by a 25 minute forming gas anneal at 400°C. The purpose of the light diffusion and oxidation is to passivate the surfaces of the wafers in order to allow bulk lifetime measurements to be taken. The high temperature of course also allows effusion of impurities to take place. The sheet resistivity of the diffused layer was typically 250 Ω/□.

The FZ wafer upstream of an effusing sample should receive a lower dose of impurities than the downstream wafer, which is likely to be subjected to impurities on both surfaces due to turbulence in the gas stream. Accordingly, experiments showed that upstream FZs had lifetimes 2 to 3 times longer than the downstream ones for sufficiently contaminated samples.

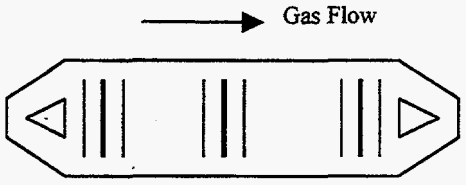


Figure 1: Diagram of wafer positions in quartz boat during cross-contamination experiment. The heavy vertical lines represent multicrystalline wafers, the lighter ones float zone wafers.

Clearly it is important to avoid impurities from upstream groups of wafers contaminating the FZ wafers surrounding other multicrystalline wafers further downstream. To minimise the risk of this happening, the separation between each group of three wafers was kept as large as possible (about 10cm). Also, wafers which were known to contain large amounts of mobile impurities were placed at the downstream end of the boat. As a result of these measures, contamination from upstream wafers was negligible, as indicated by the lifetimes of the control wafers in front of each sample. The downstream FZ wafer lifetimes were used for analysis, because they were least likely to be affected by other batches upstream, and also because they were exposed to a greater dose of impurities from the corresponding multicrystalline sample.

The experiment was performed using 1000Ωcm FZ wafers, and bulk carrier lifetimes were measured using two different techniques. All of the FZ wafers exhibited lifetimes in excess of 100μs, so the conventional transient photoconductance decay method was used for such samples. However, the multicrystalline wafers had lifetimes well below 100μs, requiring the use of the quasi-steady state photoconductace technique (QSSPC) [8,9].

3. RESULTS AND DISCUSSION

The bulk lifetimes of the multicrystalline samples and the corresponding contaminated FZ samples are depicted in Fig. 2. The lifetimes shown are maximum lifetimes, and occur at a carrier density of about $1\times10^{15}cm^{-3}$ for most samples. In an uncontaminated environment, the high resistivity FZ wafers would yield a lifetime of around 4ms under the light phosphorus diffusion conditions used in this study. Fig. 2 reveals that the central multicrystalline wafers are essentially 'clean', evidenced by the FZ lifetimes being almost equal to the value expected from an uncontaminated environment. The top and bottom wafers are clearly heavily contaminated, while those from just below the top have moderate concentrations of mobile impurities.

It is interesting to compare the degraded FZ lifetimes with the corresponding multicrystalline samples. Assuming that the impurities degrade the lifetime through a SRH type recombination mechanism, then the lifetime of the multicrystalline samples is inversely proportional to the

concentration of impurities in them, which in turn should be proportional to the lifetime of the FZ wafers. For the central and near-top wafers, an increasing concentration of impurities is reflected by a proportional decrease in the multicrystalline sample lifetime. However, the lifetimes of the top and bottom multicrystalline wafers are only around 1μs, much lower than one might expect considering the lifetimes of the FZs. This is due to the fact that the dominant recombination mechanisms in these multicrystalline wafers are not SRH in nature, but are due to complex interactions between crystallographic defects and impurities.

Figure 2: Lifetimes of multicrystalline and contaminated 1000Ωcm FZ wafers.

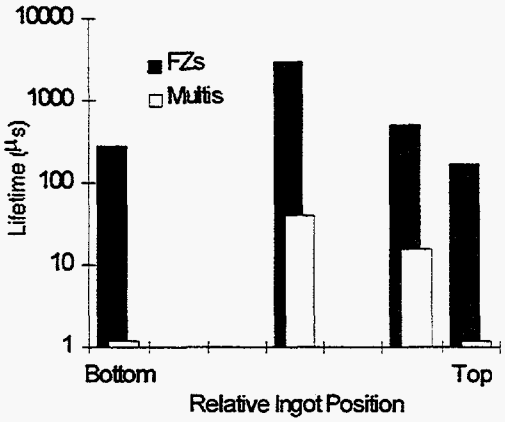
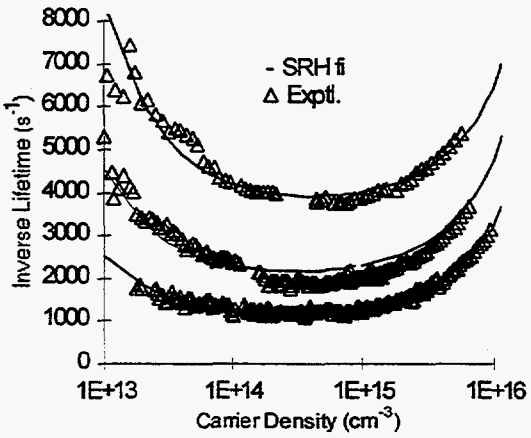


Figure 3: Experimental and fitted curves for contaminated FZ wafers.



To further examine the effects of the impurities on carrier lifetime, plots of lifetime against carrier density were obtained. Due to the very low concentration of crystallographic defects in FZ silicon, it is reasonable to expect that the presence of impurities will cause the lifetime to vary with carrier density as per the SRH model [6]:

$$\tau_{SRH}=[\tau_{n0}(p_0+p_1+n_e)+\tau_{p0}(n_0+n_1+n_e)]/(n_0+p_0+n_e)$$

where the thermal densities of free electrons and holes are defined by:

$$n_1=n_0 exp((E_f-\phi)/kT)$$
$$p_1=p_0 exp((\phi-E_f)/kT)$$

and where n_0, p_0 are the equilibrium electron and hole concentrations, ϕ the Fermi energy, E_f the flaw (impurity) energy level and n_e the excess density of electrons. The fundamental lifetimes τ_{n0} and τ_{p0} are defined in terms of the impurity density N_f and the capture cross-sections c_n and c_p via $\tau_{n0}=1/(c_n N_f)$ and $\tau_{p0}=1/(c_p N_f)$.

Recombination also occurs in the lightly diffused regions [10], where the saturation current density is J_0, requiring the addition of another term to the inverse carrier lifetime, so that:

$$1/\tau_{total} = 1/\tau_{SRH} + 2J_0(N_A+n_e)/qn_i^2W$$

where N_A is the acceptor density, n_i the intrinsic carrier density and W the substrate thickness. The first term tends to dominate at low injection, while the second is more important in high injection. The

presence of Auger recombination at high injection is dealt with by subtracting the component of the lifetime that increases as n_e^2.

Fig 3 gives some experimental data for the contaminated FZs, and also shows the fit obtained by applying the above equation. Once the electron and hole capture cross-sections were fitted for one sample, only the impurity density required changing to obtain a good fit for the other samples. This fact implies that the impurities causing the lifetime degradation are present in approximately equal proportions in each sample. Secondary Ion Mass Spectrometry (SIMS) has confirmed this fact, identifying the two main impurities as Cr and Fe. The important energy levels of these elements for recombination in silicon are 0.31 and 0.58eV below the conduction band [11]. As a result, in the SRH model used here, the impurity energy level was chosen to be at the centre of the energy gap. The difference in the impurity levels of the two elements is not very important, as the goodness of fit of the theoretical curve does not depend strongly on this parameter.

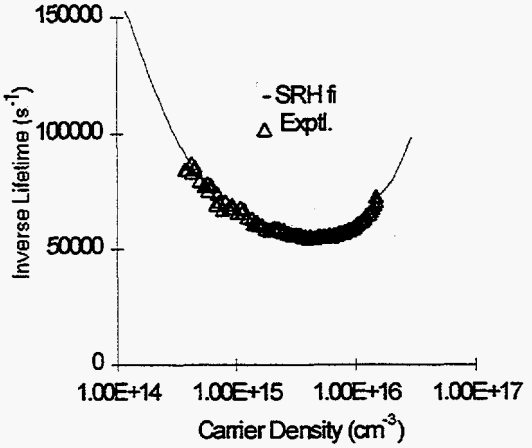
The impurity densities corresponding to each fit are given in Table I, and are approximately inversely proportional to the maximum lifetimes as expected from the SRH model. The value of the saturation current density J_0 was slightly different for each sample, with a typical value being 5×10^{-13}Acm^{-2}. The results imply that the density of mobile impurities in the bottom, central, near-top and top regions of the multicrystalline ingot go in the ratio 16:1:2:360.

The obvious next step is to determine if the capture cross-section parameters determined for the FZ wafers can be used to describe the lifetime curves of the original multicrystalline samples. However, most of the multicrystalline samples display a low injection trapping phenomenon which obscures the SRH lifetime dependence. The effect is less marked in samples with good crystallographic quality. Fig 4 shows the lifetime curve for one multicrystalline wafer that did exhibit some SRH behaviour. The data for the corresponding contaminated FZ wafer is given in Table I, directly above the entry for the multicrystalline sample. The same cross section parameters can be used to fit both curves, indicating that the recombination processes are similar for the two wafers, at least in the carrier density range shown. At lower injection levels, the multicrystalline wafer shows an *increasing* lifetime (trapping) due to interactions between the crystallography and the impurities. However, these results show that in good quality multicrystalline wafers, SRH behaviour is often present and dominates at some injection levels.

Table I: SRH fit parameters c_n, c_p and N_f for curves shown in Figs. 3 and 4.

Region, Type	Resist. Ωcm	c_n cm^{-3}s^{-1}	c_p cm^{-3}s^{-1}	N_f cm^{-3}
Bottom FZ	1000	4e-8	3e-10	1.2e13
Centre FZ	1000	4e-8	3e-10	3.6e12
Neartop FZ	1000	4e-8	3e-10	6.5e12
Top FZ	1000	4e-8	3e-10	1.3e14
Centre FZ	1000	1e-7	3e-12	8.5e12
Centre Multi	0.9	1e-7	3e-12	2.5e12

Figure 4: Experimental and fitted values for a multicrystalline sample.



The fact that the multicrystalline sample has a lower impurity density according to the SRH model, despite it's lower maximum lifetime, is due to the differing resistivities. However, the relative concentrations between samples of the same resistivities are still valid, meaning that other multicrystalline samples could be ranked against the one shown.

Previous work [12] has shown that when the concentration of mobile impurities is high, then the substrate will exhibit a significant improvement in lifetime after gettering, provided that the dislocation density is sufficiently low. Consequently, cross-contamination is a useful tool for qualitatively predicting wether a sample will improve after gettering.

4. CONCLUSIONS

Cross-contamination of FZ wafers by effusing impurities from multicrystalline wafers provides a technique for studying the impurities in a less complex substrate. This allows a simple SRH model to be fitted to the lifetime versus injection level curve, which in turn provides data on the relative concentration of impurities in the original multicrystalline wafers.

The method could be extended by applying Deep Level Transient Spectroscopy (DLTS) to the contaminated FZs in order to determine the absolute concentration of impurities. SIMS analysis of gettered layers of the multicrystalline samples would then provide information on the relative concentrations of impurities in those samples. Combined, the information would allow the cross-contamination process to be calibrated, and further lifetime measurements of contaminated FZs would imply an absolute value for the density of impurities in the corresponding multicrystalline sample.

ACKNOWLEDGMENTS

This work has been partially supported by the Australian Research Council. Thanks to Chris Samundsett for assisting with sample preparation.

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Defect Characterization in PV Polycrystalline Silicon Using Room-Temperature Photoluminescence

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Scanning room-temperature photoluminescence (RTPL) is applied to characterize "bad" areas with low minority carrier diffusion length in EFG poly-Si. Separate mapping of two RTPL maximums – band-to-band (1.1eV) and "defect" (0.8eV) is performed. A clear correlation is observed between 1.1eV band intensity and SPV diffusion length measured across the whole wafers, which proves that radiative efficiency is related to bulk defects. Spatial distribution of "defect" RTPL band corresponds to high-dislocation areas revealed by PVScan technique. We observed a spectacular localization of 0.8eV defects around grain boundaries.

It was reported previously that mapping of room-temperature photoluminescence (RTPL) corresponding to band-to-band emission provides a valuable feedback to electronic quality upgrading during solar cell processing in EFG poly-Si [1]. A clear evidence of recombination property improvement after P-diffusion, hydrogenation, and Al-firing was confirmed using SPV and RTPL techniques [1,2]. In this paper, we correlated PL/SPV mapping with distribution of dislocations and grain boundaries in solar grade poly-Si. Our special concern was localization of "defect" PL band, which strongly correlates with "bad" regions of a wafer with low minority carrier diffusion length.

Experimental details. (a) RTPL spectra were analyzed using SPEX-500M monochromator coupled with liquid nitrogen cooled Ge detector. The excitation source was either 514nm Ar-laser line with power ranging from 25 to 60mW or 870nm pulse IR laser diode with average power of 21 mW. By using these two laser sources a penetration depth of the excitation beam of 1μm and 25μm could be selected. Spatial resolution of PL mapping was determined as a largest between minority carrier diffusion length spanning form 40 to 300μm and a laser spot varying between 10μm and 3mm. We notice, that RTPL set-up offers either high-resolution scanning of Si wafers or fast mapping with data reading of 100msec per point. (b) Minority carrier diffusion length (L) was measured by surface photovoltage using commercial CMS-III system. Point-by-point correlation of RTPL intensity and L values were performed at the same wafer and identical resolution. (c) Distribution of the dislocation density and grain boundaries across the wafers was obtained by PVScan 5000 system using scattering laser beam from the etched surface of sister wafers.

Results. Typical RTPL spectra taken at two different points of the same EFG wafer are shown in Figure 1. Generally, only two bands are observed above 90K: band-to-band emission with $h\nu_{max}$=1.1eV and "defect" PL band with maximum at about 0.8eV. Both bands are distributed strongly inhomogeneously. Regarding intensity of 1.1eV band (I_{bb}), we found a straight correlation with SPV diffusion length (Figure 2). Across the wafer, I_{bb} is changing approximately as L^2 and consequently proportional to minority carrier lifetime. Additionally, band-to-band RTPL mapping is similar for Ar-laser and IR laser excitation. This is a strong indication that RTPL is indeed a measure of bulk recombination and can be used, like L, to track electronic quality of PV poly-Si.

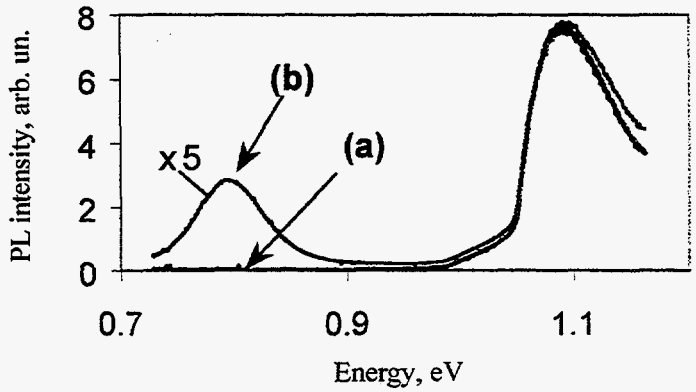

Fig.1 RTPL spectra of EFG poly-Si at two wafer regions: (b) corresponds to grain boundary area shown in figure 5.

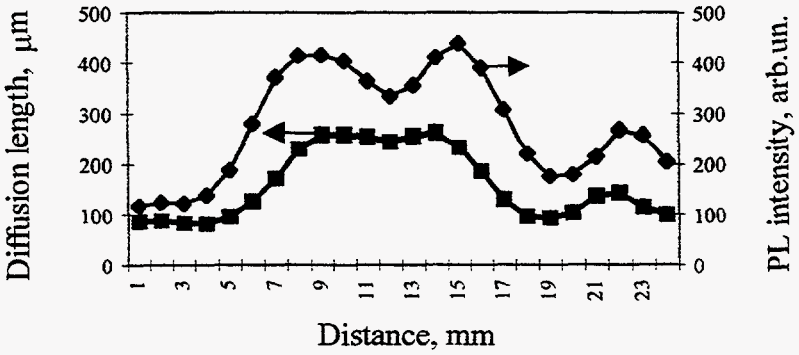

Fig.2 Room temperature band-to-band PL intensity correlates with the distribution of minority carrier diffusion length.

PVScan technique allows correlating a distribution of recombination centers with extended defects: grain boundaries and dislocations. In Figure 3, two maps of dislocation density and band-to-band RTPL of the same cast wafer are shown. It is straightforward, that I_{bb} is inversely related to the concentration of dislocations. Specifically, an increase of dislocation density up to $9x10^3$ cm^{-2} correlates to a drop of I_{bb} by factor of 5 compared

to I_{bb} at dislocation low region. This observation consistent with general concept that dislocations in Si serve as gettering sights for point defects providing precipitation of heavy metals such as Fe, Ni, Cu, etc. Defect precipitates are strong non-radiative centers and a reason of "bad" regions with a low minority carrier lifetime and reduced RTPL intensity.

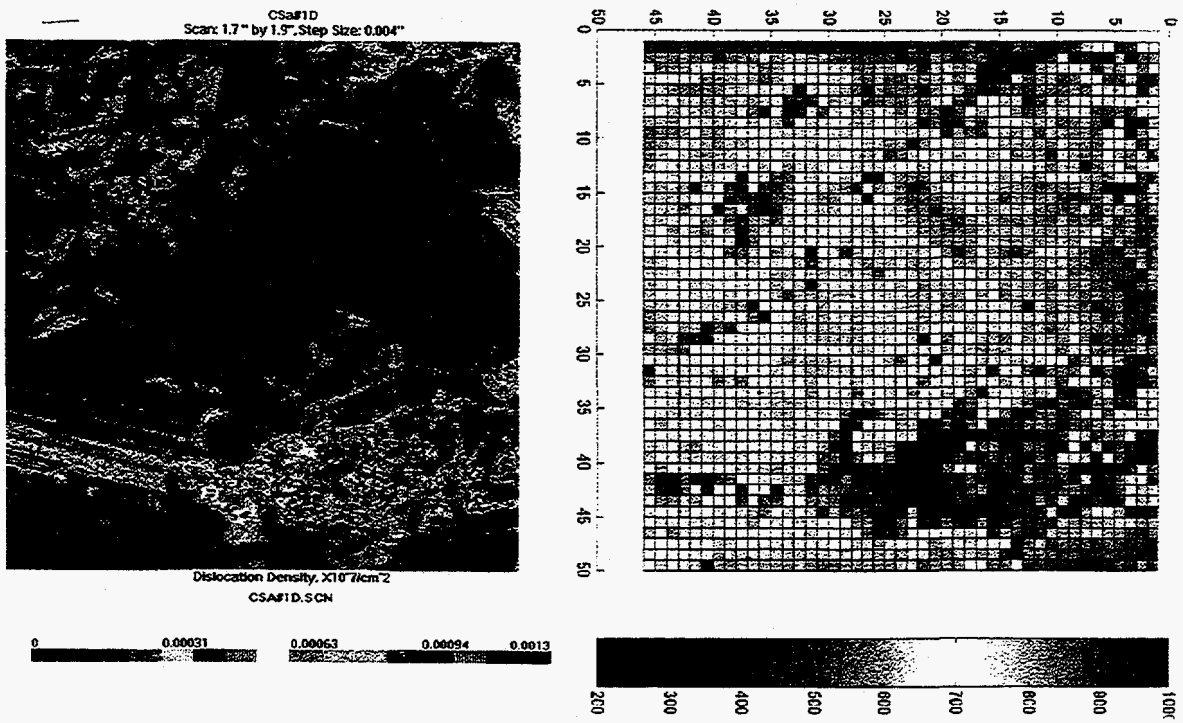

Fig.3 Two-dimensional map of the dislocation density measured with PVScan method (left) correlates with map of the room-T band-to-band PL intensity (right). Higher dislocation density regions possess lower band-to-band PL.

We also performed RTPL mapping of the "defect" band and correlated its intensity (I_{def}) with band-to-band emission. Scanning across entire 4"x4" EFG wafer did not reveal point-by-point correlation between I_{def} and I_{bb}. At the same time, using high-resolution mapping we observed an inverse relation of both bands at selective localized areas of EFG wafers as shown in Figure 4. We noticed, that I_{def} is localized in areas with high concentration of extended defects. To illustrate this effect, a distribution of I_{bb} and I_{def} is shown around the individual grain boundary in Figure 5. A dramatic increase of 0.8eV band by a factor of 25 at grain boundary is accompanied by a ten-fold reduction of the band-to-band intensity.

Such a competing behavior of "defect" luminescence with regards to I_{bb} and consequently minority carrier lifetime, allows suggesting that strong non-radiative recombination centers accompany the 0.8eV band. One of possibilities is that unpassivated dangling Si bonds are in charge for a low diffusion length in regions of dislocations (Figure 3) and grain boundaries (Figure 5). This was confirmed using DLTS and will be published elsewhere.

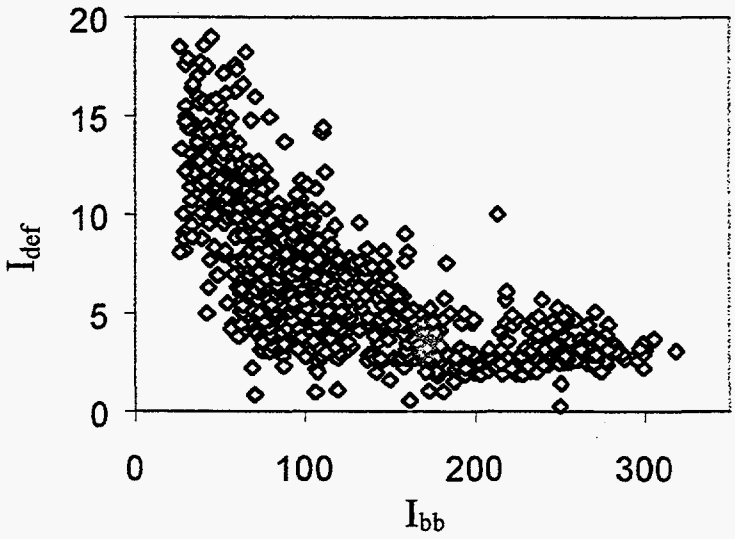

Fig.4 "Defect" vs band-to-band RTPL for an EFG wafer subjected to P-diffusion and H-passivation. Mapping area 15 x15 mm.

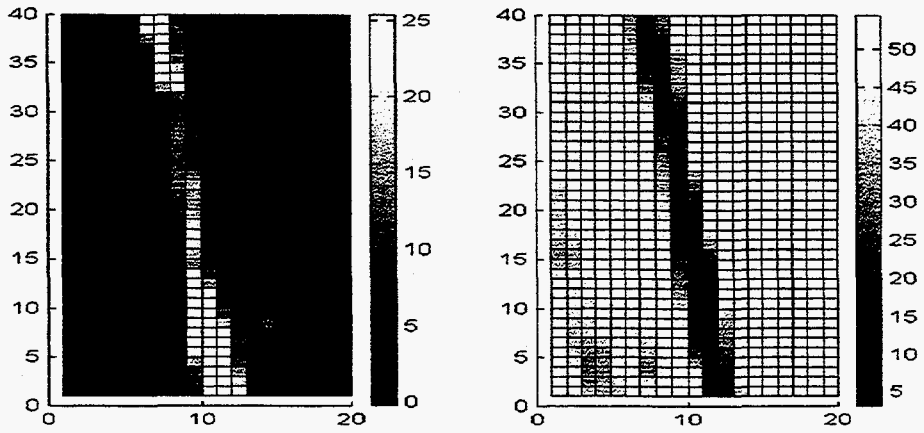

Fig.5 5 mm x 10 mm mapping of defect (left) and band band-to-band (right) RTPL around a grain boundary in EFG wafer. The spectra in figure 1 were measured at the grain boundary (b) and out of the grain boundary (a).

Conclusions. New approach to defect diagnostics in PV poly-silicon using scanning room temperature photoluminescence is developed. Spectrally selective RTPL mapping offers a high throughput, adjustable spatial resolution, and information on a local upgrading of PV materials. It can be used for on-line monitoring of electronic quality in crystalline Si solar cells.

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Interstitial Copper in Silicon

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Despite the importance of copper in the silicon semiconductor industry as a major contaminant, the electrical and structural properties of *Cu* are poorly understood [1]. Even such a fundamental property of *Cu* in *Si* as its diffusion coefficient remains uncertain. This hinders quantitative studies of gettering of copper in silicon. In this paper, we discuss the problem of determination of effective and intrinsic diffusion coefficients of copper and the role of *Cu*-acceptor pairing for understanding of *Cu* precipitation kinetics.

Unlike most other 3d transition metals, copper diffuses in silicon in the positively charged state [2]. The theory of diffusion of positively charged ions in the presence of immobile acceptors was developed by Reiss *et al.* [3]. They showed that, due to the processes of trapping and releasing of donors by acceptors, the effective (apparent) diffusivity D_{eff} of donors in *p*-type material is lower than their diffusivity in intrinsic material D_{int} and in the case of $N_D << N_a$ is given by $D_{eff}=D_{int}/(1+\Omega N_a)$, where N_a is the acceptor concentration, N_D is the concentration of mobile donors and Ω is the pairing constant.

The first data point on copper diffusivity was obtained on intrinsic silicon by Struthers [4]. First temperature dependent measurements were done by Hall and Racette [5] on heavily boron doped *p*-type *Si* ($N_a=5\times10^{20}$ cm^{-3}). Later Heiser *et al.* [6] measured the effective copper diffusivity in *In* and *Ga*-doped *p-Si* around room temperature by the Transient Ion Drift (TID) technique. The studies reported in [5, 6] were made on *p*-doped silicon and consequently only an effective diffusion coefficient of copper was measured. Yet, Hall and Racette [5] neglected the donor-acceptor pairing and suggested the expression $D=4.7\times10^{-3}\times exp(-0.43\ \text{eV}/k_BT)\ cm^2s^{-1}$ for the intrinsic copper diffusion coefficient in silicon. In the following papers[6, 7, 8, 9] an attempt was made to re-evaluate the intrinsic diffusion coefficient using the theory of Reiss *et al.* [3] and assuming a Coulomb interaction between Cu ions and acceptors. This model implies that the potential energy of donor-acceptor interaction *V(r)* should depend only on the acceptor charge state and not on its chemical nature. Yet, recent experimental studies of the copper-acceptor dissociation energy reported by Wagner *et al.* [10] revealed that the dissociation energy is different for different types of acceptors (0.61 eV for *CuB*, about 0.70 eV for *CuAl*, *CuGa* and *CuIn* and 0.85 eV for *CuPt*), thus indicating that the binding in these pairs has a covalent component. This conclusion is in agreement with theoretical calculations done by Estreicher [11]. As follows from the results presented below, the assumption of a purely Coulomb interaction [8, 6, 9] resulted in an underestimation of the pairing constant Ω by more than an order of magnitude and the previously published 'intrinsic' diffusion data need to be reconsidered.

In this study we designed experiment in such a way that the intrinsic diffusivity of interstitial copper could be determined directly from the experimental data. Thus, estimation of Ω from theoretical models based on an uncertain interaction potential was avoided. Sample preparation is described elsewhere [6]. Effective diffusion coefficient of copper in the temperature range of T=240 K to 380 K was determined using Transient Ion Drift (TID) [6]. The time constant of the TID transients τ_{TID} is proportional to the *Cu* effective diffusion coefficient [6, 12, 13], which in turn is proportional to the intrinsic diffusion coefficient. Using equations from Refs. [6, 14], we obtain

$$\tau_{TID} = \alpha \times \frac{\varepsilon\varepsilon_0 k_B T}{q^2 N_a D_{\text{int}}} \times \left(1 + 4\pi\beta \times N_a D_{\text{int}} R_C \tau_{diss}\right) \qquad (1)$$

where ε and ε_0 are the dielectric permittivity of silicon and vacuum, respectively, q is the elementary charge, τ_{diss} is the temperature-dependent time constant of dissociation of copper-acceptor pairs, and R_C is the capture radius of Cu_i^+ by acceptors. Coefficients α=2.85 and β=1.95 are two correction factors introduced by Heiser *et al.* [13]. The process of trapping is characterized by a capture radius R_C, which is calculated from the condition that the average thermal energy k_BT equals the attractive potential energy $V(r)$, i.e., $k_BT=V(R_C)$. Since in most cases R_C is as large as several *nm*, the covalent component of the ion interaction can be neglected and $V(R_C)$ can be approximated by a screened Coulomb potential:

$$k_BT = \frac{q^2}{4\pi\varepsilon\varepsilon_0 R_C} \times exp\left[- R_C / \left(\frac{\varepsilon\varepsilon_0 k_B T}{q^2 p} \right)^{1/2} \right] \qquad (2)$$

where p is the free hole density. For the doping levels $N_A \leq 10^{17}$ cm^{-3} the exponential term in Eq.(2) can be neglected, and R_C can be expressed explicitly. In this case, Eq.(1) becomes:

$$\tau_{TID} = \alpha \times \frac{\varepsilon\varepsilon_0 k_B T}{q^2 N_a D_{\text{int}}} + \alpha \times \beta \times \tau_{diss} \qquad (3)$$

The first term on the right-hand side of Eq.(3) describes the average drift time of unpaired copper ions through the depletion region. The second term describes the dissociation of copper-acceptor pairs. If $\tau_{TID} >> \alpha \times \beta \times \tau_{diss}$, the pairing is weak and the TID time constant is determined primarily by the intrinsic drift of copper ions through the depletion region. The intrinsic diffusivity D_{int} can in this case be determined directly from the experimental data as follows:

$$D_{\text{int}} = \frac{\alpha\varepsilon\varepsilon_0 k_B T / (q^2 N_a)}{\tau_{TID} - \alpha \times \beta \times \tau_{diss}} \qquad (4)$$

On the other hand, if $\tau_{TID} \approx \alpha \times \beta \times \tau_{diss}$, then the pairing is strong and the denominator in Eq.4 becomes arbitrary close to zero. In this case the information on the intrinsic diffusion coefficient contained in the dependence $\tau_{TID}(T)$ drops below the measurement errors and D_{int} cannot be extracted unambiguously from the experimental data. Previously reported data on room-temperature *Cu* diffusivity [6] were obtained under the conditions of strong pairing, and Eq.(4) could not be used for determination of D_{int}. An analysis of Eq.(4) and numerical simulations of the temperature dependence of the TID time constants revealed that the conditions of weak pairing can be achieved in a wide temperature region using boron-doped samples with low doping level. Experiments, which will be reported in more detail elsewhere [15], showed that for FZ silicon samples with the doping level of 1.5×10^{14} cm^{-3}, the conditions of the weak pairing are maintained at the temperatures above approximately 255 K, whereas below 255 K the pairing of copper with boron is dominant and determines the effective diffusivity. Using Eq.(4) and the equation for dissociation rate of *CuB* pairs, reported by Wagner *et al.* [10], the intrinsic diffusivity of copper was calculated as a function of temperature, using our experimental data points. The obtained diffusivities are presented in Fig.1 as an Arrhenius plot. A linear regression to our data together with the data obtained on intrinsic silicon at 1173 K by Struthers [4] yielded the following expression for the interstitial copper intrinsic diffusion coefficient:

$$D_{\text{int}} = (3.0 \pm 0.3) \times 10^{-4} \times \exp\left(-\frac{0.18 \mp 0.01 \text{ eV}}{k_B T}\right) \ (\text{cm}^2 / s) \qquad (5)$$

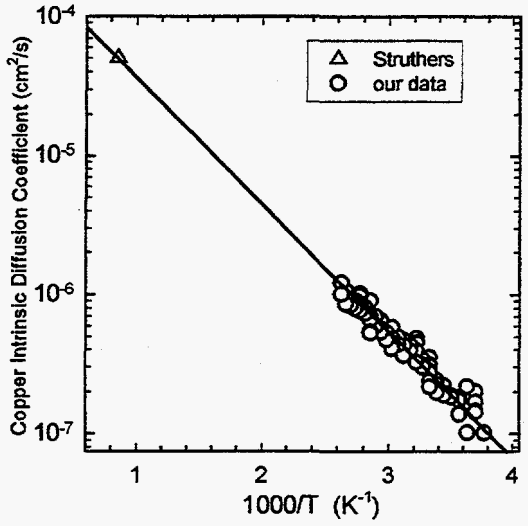

Fig.1. Intrinsic diffusion coefficient of copper determined from our experimental data (N_a=1.5×10^{14} cm^{-3}) in the temperature range 265 to 380 K (circles) and experimental data point reported by Struthers ([4], open triangle).

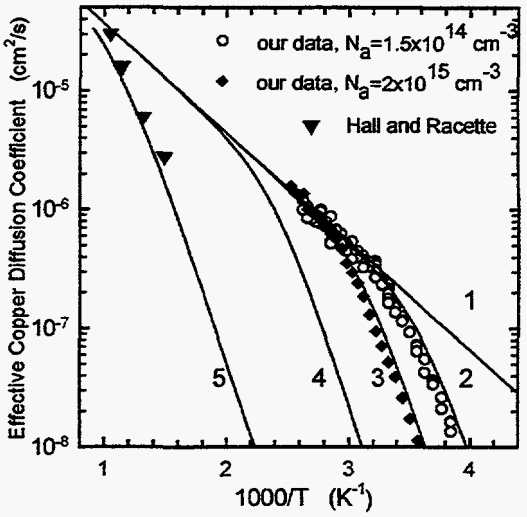

Fig.2. Effective diffusion coefficient of copper in silicon calculated for different boron doping levels (lines) and experimental data obtained in this study (circles, N_a=1.5×10^{14} cm^{-3} and diamonds, N_a=2×10^{15} cm^{-3}) and by Hall and Racette [5] (triangles, N_a=5×10^{20} cm^{-3}). Curve 1 - intrinsic silicon, curve 2 - N_a=1.5×10^{14} cm^{-3}, curve 3 - N_a=2×10^{15} cm^{-3}, curve 4 - N_a=1×10^{17} cm^{-3}, curve 5 - N_a=5×10^{20} cm^{-3}.

The intrinsic diffusion barrier of 0.18 eV in Eq.(5) is indeed much lower than it was assumed before, but it is close to the values recently predicted theoretically by Woon *et al.* [16].

We would like to emphasize that Eq.5 describes the copper diffusivity in the absence of copper-acceptor pairing and is valid only in intrinsic or *n*-type silicon, if no other trapping process exists. In *p*-type material, however, it is the effective diffusivity D_{eff} which describes copper diffusion and which is relevant for all practical applications. Using the equations discussed above, we obtain a convenient numerical equation for effective diffusion coefficient in moderately boron-doped ($N_a \leq 10^{17}$ cm^{-3}) silicon:

$$D_{eff} = \frac{3\times10^{-4}\times\exp(-2090/T)}{1+2.584\times10^{-20}\times\exp(4990/T)\times(N_a/T)} \qquad (6)$$

In Fig.2 we present the effective copper diffusivity calculated for different doping levels. Also presented are the effective copper diffusivities determined from TID measurements and the data of Hall and Racette [5]. The calculations agree over the whole temperature range not only with the data used for the determination of D_{int}, but also with the data measured in the medium doped material (N$_a$=2×10^{15} cm^{-3}). This confirms the validity of Eq.6 used for the intrinsic diffusion coefficient. The agreement also extends over the whole investigated doping level range (1.5×10^{14} to 5×10^{20} cm^{-3}) since Hall and Racette's data points (triangles) are close to the calculated dependence (curve 5). This confirms that the data of Hall and Racette represent the effective diffusion coefficient for N_a=5×10^{20} cm^{-3}, and explains their significant deviation from the intrinsic diffusivity curve. Furthermore, since the effective diffusion coefficient depends nonexponentially on temperature (see Eq.6), the exponential expression suggested by Hall and Racette can be used only as an approximation in the temperature range where the data points were taken and may result in significant errors if extrapolated outside of this range.

Copper precipitation behavior differs significantly from that of other transition metals. As it was discussed above, *Cu* diffusion in *p-Si* is determined by the effective diffusion coefficient D_{eff}, which, for

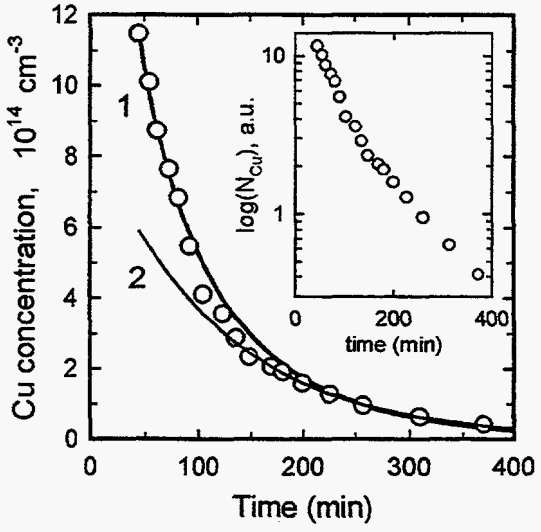

Fig.3. An experimentally measured *Cu* precipitation kinetics (FZ *Si*, $N_a=3\times10^{15}$ cm^{-3}, diffusion temperature 700^{0}C) (circles) and its fit using non-exponential dependence given by Eq.7 (curve 1) and by an exponential fit to the tail of the decay (curve 2). Inset: the same experimental data in logarithmic scale.

a given temperature, depends on the concentration of copper N_{cu}. pairing constant Ω, and the concentration of shallow acceptors N_a. The complete equation for $D_{eff}=D_{eff}(N_a, N_{Cu}, \Omega)$ can be found in Ref. [3]. In the case of $N_a<<N_{cu}$, this equation reduces to $D_{eff}=D_{int}/(1+\Omega N_a)$. The knowledge of the intrinsic diffusion coefficient of *Cu* enabled us to describe the precipitation kinetics of interstitial copper. Using Ham's equation [17] with the effective diffusion coefficient given by Eq.6:

$$\tau^{-1}_{precip}(N_{Cu}) = 4\pi \times D_{eff}(N_{Cu}) \times nr_0 \qquad (7)$$

where n is the density of precipitation sites and r_0 is their effective radius. Note that the value of D_{eff} changes with the decreasing interstitial copper concentration. This makes the precipitation kinetics of interstitial copper non-exponential, and requires Eq.7 be solved iteratively.

An example of *Cu* precipitation kinetic measured by TID is shown in Fig.3. A non-exponential fit according to Eq.7 (curve 1) provides a much better agreement with the experimental data than a single-exponential fit (curve 2). This confirms the validity of Eq.(7) and shows that Eq.(7) can be used in predictive simulations of gettering of copper in silicon wafers.

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CHEMICAL STATE AND ELEMENTAL DISTRIBUTION OF METAL IMPURITIES IN POLYCRYSTALLINE SILICON SOLAR CELLS

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ABSTRACT

The work presented here directly measures the chemical state and elemental distributions of metal impurity in as-grown polycrystalline silicon used for terrestrial-based solar cells. The goal was to determine if a correlation exists between poorly performing regions of solar cells and metal impurity distributions as well as to ascertain the chemical state of the impurities. Synchrotron-based x-ray fluorescence mapping and x-ray absorption spectroscopy, both with a spatial resolution of 1μm, were used to measure impurity distributions and chemical state, respectively, in poorly performing regions of polycrystalline silicon. The Light Beam Induced Current method was used to measure minority carrier recombination in the material in order to identify poor performance regions. We have detected iron, chromium and nickel impurity precipitates and we have recognized a direct correlation between impurity distributions and poor performing regions in both as-grown and fully processed material. Furthermore, from x-ray absorption studies, we have initial results, indicating that the Fe in this material is in oxide form, not $FeSi_2$. These results provide a fundamental understanding into the efficiency-limiting factors of polycrystalline silicon solar cells as well as yielding insight for methods of solar cell improvement.

INTRODUCTION

Polycrystalline silicon can be used to fabricate solar cells with a moderate solar conversion efficiency and low fabrication costs. Although these cells are presently manufactured for terrestrial-based applications, an improvement in the efficiency of these cells would greatly increase their commercial viability. Presently, polycrystalline solar cells have efficiencies of 13-15% as compared to more expensive, single crystalline solar cells with efficiencies of 17-20% [1]. The primary cause for lowered efficiencies is localized regions of high minority carrier recombination, which possess high concentrations of dislocations [2-4]. However, it is known that minority carrier recombination at "clean" dislocations is relatively weak but greatly increases by decoration or precipitation of transition metal impurities [5-8]. This suggests dislocations in high recombination regions of polycrystalline silicon are decorated with transition metals. Past work, [9], has provided indirect evidence that metal impurities are precipitated in regions of high carrier recombination while other work, [10], has revealed metal impurity agglomerations at dislocations in polycrystalline silicon. However, no direct evidence has been provided to relate high minority carrier recombination with transition metals in this material. In fact, carbon or oxygen may play an important role since these impurities are found in high concentrations in most polycrystalline silicon, $\approx 10^{18}$ atoms/cm^3.

The first *direct* evidence of a relationship between metal impurities and poor performance was by this research group [11]. In this work, we have performed mapping of metal impurity distributions using the x-ray fluorescence microprobe, beamline 10.3.1 at the Advanced Light Source (ALS), with which we have obtained a direct correlation between metal impurities, such

as Fe, Cr and Ni, and poor performance regions of the material. Additionally, we have initial results on the chemical state of Fe in this material, specifically the Fe is in an oxide form, not a silicide. These results have serious implications in regards to strategies for material improvement.

EXPERIMENT

Boron doped polycrystalline silicon grown by an electromagnetic casting method [11] or the rapid growth on substrate (RGS) method, [12], were used in this study. Minority carrier recombination was mapped across the as-grown material with the Light Beam Induced Current (LBIC) method, using 880nm wavelength light. The frontside of the samples were analyzed using synchrotron-based x-ray fluorescence (XRF) mapping in order to determine metal impurity content and distribution. The XRF equipment is located at the microprobe beamline, 10.3.1, in the ALS. It uses 12.5keV monochromatic radiation to excite elements in the sample with a spatial resolution of $1\mu m^2$ and a Si-Li detector to measure fluorescence x-rays from the sample, all in atmospheric conditions. The XRF microprobe sensitivity is impurity and matrix specific but, for example, the system can detect a single Fe or Cu precipitate/agglomerate in silicon greater than 10-20nm in radius. The sampling depth for 3d transition metal impurities in silicon is approximately 50μm. It should be noted that the sensitivity of the microprobe drops considerably for elements with an atomic number < 16. X-ray absorption studies were carried out at beamline 10.3.2 in the ALS. A four crystal Si monochromator produces a tunable monochromatic x-ray beam, which is focussed to a $1\mu m^2$ spot with a pair of grazing incidence mirrors. A Si-Li detector was used to detect fluorescence x-rays and quantify absorption for specific elements. Detail of the absorption apparatus is given in [13].

RESULTS AND DISCUSSION

LBIC mapping of minority carrier recombination across the polycrystalline silicon sample revealed localized regions of high carrier recombination. A typical LBIC map in a portion of the cast polysilicon is shown in Figure 1 where dark regions indicate areas of high carrier recombination. Note the regions of high recombination located approximately in the center of the LBIC scan area.

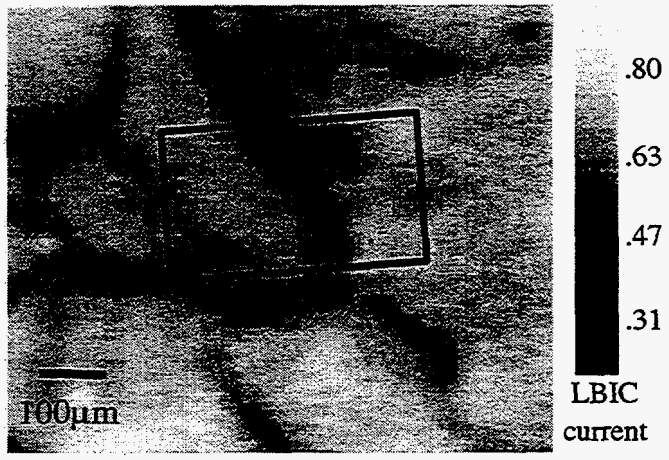

Figure 1: Light Beam Induced Current map of carrier recombination across a portion of multicrystalline silicon. Dark regions indicate high carrier recombination. The black box denotes the area analyzed with x-ray fluorescence.

X-ray Fluorescence (XRF) spectra were taken at $1\mu m^2$ points in the region of Figure 1 as denoted by the black box. No impurity-generated x-ray fluorescent radiation emits in regions of low minority carrier recombination. However, x-ray fluorescent radiation associated with Cr, Fe and Ni emits from regions of high carrier recombination. Concentrations of impurities at each $1\mu m^2$ spot were calculated by data analysis of the collected spectra and comparison to standard samples with known concentrations of impurities. Impurity maps were produced in the region denoted by the black box in Figure 1. Figure 2 is an impurity map of Fe in this region. Maps of Ni and Cr revealed the exact same distribution as the Fe, indicating a preferred precipitation site exists for these impurities. Clearly there is a correlation between

metal impurity distributions and minority carrier recombination. These results indicate metal impurities are the cause for high carrier recombination regions in polycrystalline silicon and, therefore, play a significant role in the performance of the material as a solar cell.

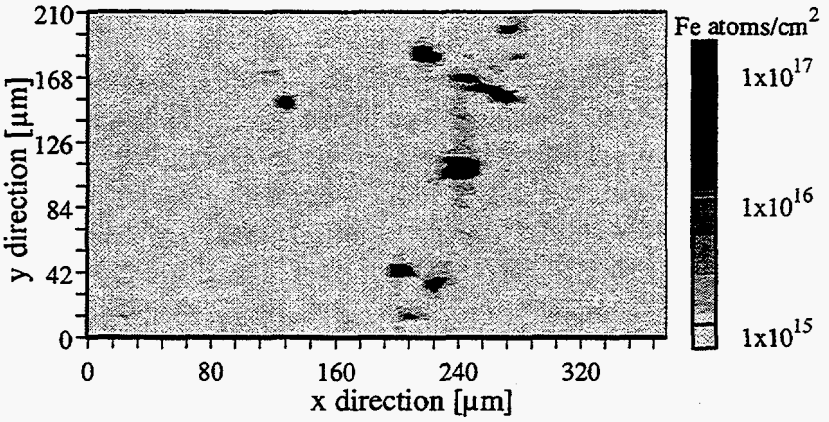

Figure 2: Fe distribution in polycrystalline silicon. The mapped area directly corresponds to the area in the black box of Figure 1. Note the correlation between metal impurity distributions and carrier recombination.

At each high impurity content region of Figure 2, a single precipitate or a number of precipitates may reside in each 1μm^2 spot. If only one precipitate is assumed present, the diameter can be calculated from the measured impurity concentrations and assuming the precipitate is located at or near the surface. For instance, the measured concentration of 5x10^{16} atoms/cm^2 for Fe shown in Figure 2 would suggest one precipitate with a diameter of 288nm is present in that area. However, considering earlier work [10,14], the impurities in Figure 2 are more likely a fine dispersion of impurity precipitates.

We have also performed x-ray absorption studies on this polysilicon material. Spectra were taken with a 1μm^2 spot on regions of high Fe content. A summation of spectral scans at the Fe K absorption edge taken in the Fe-rich region is shown in Figure 3. Additionally, for purpose of comparison, we present the summed spectrum of a standard sample with Fe in α-Fe_2O_3 with an octahedral coordination in the +3 charge-state in Figure 4. The spectra shapes are closely matched, especially in the near edge region, indicating the Fe in polysilicon also has octahedral

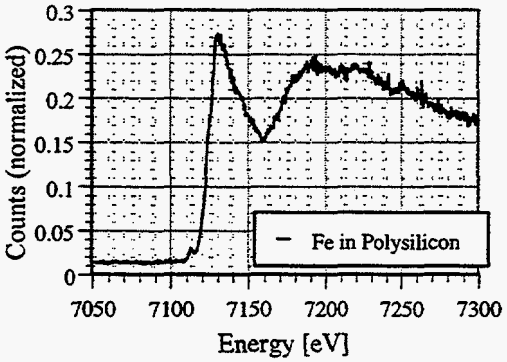

Figure 3: Summed spectrum of Fe in polycrystalline silicon. Note the similarity with Figure 4.

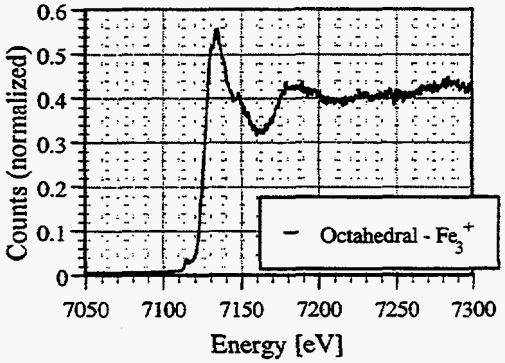

Figure 4: Summed spectrum of Fe_3^+ in octahedral coordination. Note the similarity with Figure 3.

coordination. Considering $FeSi_2$ is in either a tetragonal or orthorhombic coordination while α-Fe_2O_3 possesses an octahedral coordination, our results indicate the Fe in the polysilicon is not $FeSi_2$ but is in an oxide state. It is important to note that the binding energy of a Fe iron to a Fe oxide phase is drastically higher than Fe to a Fe silicide phase, [16]. This could constitute a lower concentration of dissolved Fe impurities in the presence of a Fe oxide particle as compared to a Fe silicide particle. Therefore, the identification of Fe oxide in polycrystalline silicon has serious implications for removal of impurities from the silicon because the flux of Fe impurities out of the material is strongly dependent on the dissolved Fe concentration.

CONCLUSIONS

In summation, metal impurities were found in polycrystalline silicon used for solar cells. The distribution of impurities correlated directly with poor performing regions of the material. These results are the first direct proof that metal impurities significantly affect the performance of polycrystalline silicon solar cells. Furthermore, we have initial results, which indicate that the chemical state of Fe in this material is Fe oxide, which would significantly retard removal of Fe from polysilicon.

ACKNOWLEDGMENTS

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Comparison of Residual Strains in Different Silicon Materials for Solar Application

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Abstract

The "Stress Distribution Scanner SDS 150" was used to measure the residual strain in different crystalline silicon materials for solar cell production. The method was found to provide reproducible and comparable results concerning magnitude and distribution of grown in stresses. Correlations between strain and grain distributions were found. Electrical cell qualities such as the efficiency seem not to be influenced by the residual strain of the wafer materials.

Introduction

The knowledge of the magnitude and distribution of residual strains in silicon wafers used for the development of photovoltaic solar cells may be interesting for both the production of crystalline starting material and the thermal wafer treatment during the cell production. In the last ten years some methods were developed which can measure the residual strain in semiconductor materials which are tranparent for near infrared light ($\lambda \approx 1$ µm) via the value of the anomalous birefrigence [1 to 8]. We investigated different materials such as EFG-Si wafers produced by ASE-Americas, mc-Si wafers from Eurosolare/Italy and BAYER/Germany and RGS-Si wafers from BAYER/Germany.
The applied method is said to give quantitative results, but there were doubtful discussions concerning this statement. We attached a great importance to a method which provides reproducible results which make it possible to compare residual stresses in different wafers of the same material and between materials produced with different growth methods. For comparison of the results and estimation of the method materials nearly free of residual strains (dislocation free FZ-silicon and Czochralski silicon crystals) and a monocrystalline material with relative high residual strain (LEC-GaAs) were investigated additionally.

Apparatus and experiments

The strain measurements were carried out with the automatic "Stress Distribution Scanner SDS-150", manufactured by *Electronstandard, 194021 St. Petersburg, Russia* (see Fig. 1). The equipment allows to investigate round wafers with diameters up to 150 mm or square resp.

rectangular shaped wafers with diagonals up to 150 mm. The wafer thickness is not very critical, but it should be in the range between 200 and 1000...1500 µm. The diameter of the laser spot amounts to 150 µm, the smallest possible step of scan is 200 µm. The scan width to be applied depends on the required resolution of the strain distribution. It has to be regarded, that the maximum number of measuring points is 12.000, so that by application of the smallest step large area wafers can be measured only partially. A measurement with application of the maximum number of measuring points needs 6 hours, without consideration of wafer preparation, heat-up time of the laser and wafer adjustment.
Thin wafers cut with multi-wire saws or annular diamond saws may be measured after a short chemical polishing with HF-HNO_3 = 1:4 (2...3 min, room temperature). Wafers with more than 500 µm thickness were chemomechanically polished on both sides. EFG wafers were investigated as grown.

Results

In Fig. 2 a survey is given about the average residual strains in the investigated materials. In EFG silicon (we had only wafers from the run 41N61D) in the single wafers residual strains between 3 and 10 MPa were measured. The strain distribution is in a rather good accordance with the grain structure of the wafers. EFG is the material with the maximum measured residual strains and inhomogeneities in the strain distribution.
In spite of an average strain value of a little more than 2 MPa, RGS wafers show a preverably homogeneous strain distribution. It has to be mentioned that only a few samples were available for the investigations.
Cast mc silicon from both Bayer and Eurosolare have residual strains which are a little higher than strains measured in Czochralski monocrystals. The materials show a preverably homogeneous strain distribution which may correlate with the grain structure or not. The materials from both manufacturers may differ in the average grain sizes. Generally was found: The higher the grain size the lower the average strain value.

Conclusion

The method of strain determination via the measurement of the anomalous birefrigence was found to give good comparable and reproducible results about the magnitude and distribution of residual strains in crystalline solar silicon materials. Additional measurements of dislocation free (111)- and (100)- FZ-silicon crystals with extremely low residual strains emphasize these results. In the near future works should be done concerning the correlation of residual strains with structural material properties, material and cell production and the electrical cell behaviour. The latter seems to be only little influenced by the residual strain of the employed wafer material. Strain measurements may be important for the modelling of growth processes.

Acknowledgment

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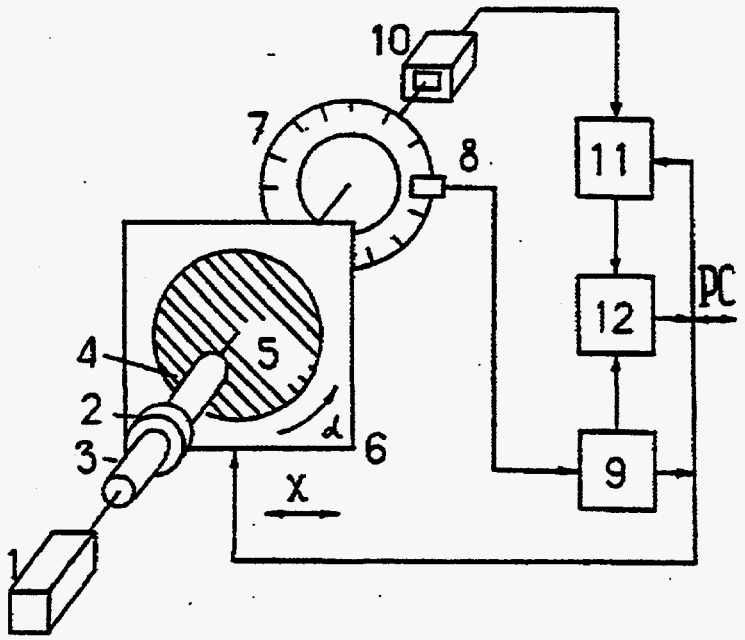

Fig.1: Functional scheme of the automatic stress distribution scanner SDS-150 after [1]:

1) He-Ne laser, wavelength $\lambda = 1.15$ µm, light spot diameter 200 µm. 2) Phase plate $\lambda/4$. 3) Optical system for beam expanding. 4) Objective for beam focussing. 5) Investigated sample, diameter (or wafer diagonal) up to 150 mm. 6) Double-coordinate scanning table. 7) Rotating analyzer. 8) Angular coder. 9) Pulse former. 10) Radiation detector. 11) Amplifier. 12) Analogue-to-digital converter.

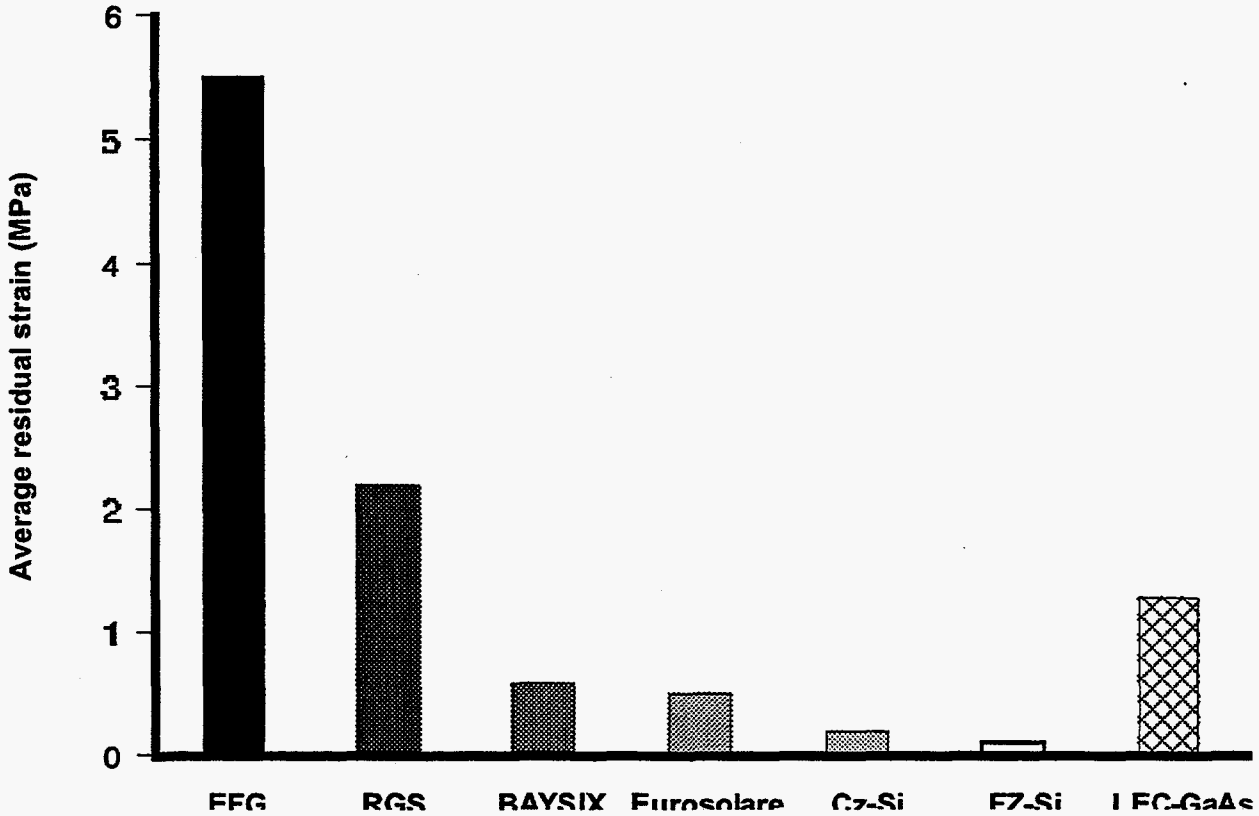

Fig. 2: Comparison of the residual strains of different materials used for solar cell fabrication. The represented values are average values obtained from several single measurements.

Improvement of Material Parameters of Silicon by Gettering

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ABSTRACT: This article gives a review of major gettering techniques. An extensive database of references to specific gettering techniques and their applications for gettering of specific metals is included. A special emphasis is put on gettering techniques which are applicable for photovoltaic industry. Current trends in the development of gettering and possible directions of future development are discussed.

1 Introduction.

It is well established that contamination of silicon wafers with transition metals can reduce device yield even if the concentration of metals is below 10^{12} cm^{-3}. Transition metals are generally fast diffusers with high solubilities at high temperatures[1] and can easily be incorporated into the bulk of silicon ingots during crystal growth, or contaminate the wafer surface during wafer sawing, surface texturing treatments, screen printing or other processing steps, and then diffuse into the bulk during subsequent high temperature heat treatments. Numerous techniques were developed to keep unintentionally introduced metals away from the device regions in the I.C. industry or out of the whole bulk of the silicon wafers in solar cells industry. These techniques are generally referred to as gettering techniques. Gettering is the process whereby impurity concentrations are reduced in the device region of the wafer by localizing them in separate pre-defined regions of the wafer[2,3]. In general, gettering can be considered a three-step process[4]. The impurity must be (1) released from its original and undesirable state to then (2) diffuse through the crystal from device region to the gettering sites, and be (3) captured at the gettering site. It is well established that for the slower diffusing initially dissolved transition metals, such as iron or gold, diffusion to the gettering site is typically the rate-limiting step[5,6]. Thus, in the I.C. industry, where the device region is the near-surface layer, it is highly desirable to bring the gettering region closer to the device region. Gettering techniques which utilize gettering regions within 10 μm of the device region are known as proximity gettering techniques and hold promise to perform well even with the lower thermal budgets. In the PV industry, the only option is to reduce the wafer thickness. Just such a trend is taking place in the PV industry, but for other considerations such as efficiency and silicon consumption.

There are two general classes of gettering, defined by the capture mechanisms, segregation and relaxation. Some authors have proposed gettering assisted by self-interstitial injection as the third mechanism[7-9]. In this review, we will describe the injection-assisted gettering within the segregation gettering section. Sometimes, gettering techniques are classified as internal and external, depending on how the gettering sites were introduced in the wafer (See, e.g., Ref. [10]). Internal gettering does not require any extra treatment (except for annealings) to achieve a gettering effect since the gettering sites are already present in as-grown material or they are produced and activated by an annealing treatment. External gettering typically requires an external treatment such as dopant diffusion, mechanical damage or ion implantation to form a precipitation/segregation region in the wafer. Sometimes, gettering techniques are also classified as intrinsic and extrinsic, depending whether the gettering region is located inside of the wafer or at the wafer surfaces.

2 Gettering mechanisms: relaxation and segregation gettering.

Relaxation gettering techniques require heterogeneous precipitation sites to be intentionally formed in regions away from the device region. The gettering process requires an impurity supersaturation, which typically occurs during a cool down from high temperatures. Any mobile and supersaturated impurity will quickly precipitate in regions of the silicon wafer with high concentrations of precipitation sites. In these regions, the dissolved impurity concentration remains close to the thermodynamic equilibrium solubility. In neighboring regions, such as the device region with low nucleation site densities, supersaturated impurities will not precipitate quickly, and thus impurity concentrations may significantly exceed the thermodynamic equilibrium concentrations during a cool down. This difference in precipitation rates creates a dissolved impurity concentration gradient. In this manner, supersaturated impurities diffuse away from the surface/device region and into the bulk during a cool down. This process is often referred to as relaxation gettering since it requires the supersaturation of impurities to 'relax' to equilibrium concentrations during a cooling step.

The most widely used relaxation gettering technique in the I.C. industry is internal gettering, which utilizes oxygen precipitates and the associated structural defects (punched out dislocation loops and stacking faults), which are inherent in CZ wafers, as heterogeneous nucleation sites for any supersaturated transition metals. Another example of relaxation gettering is backside damage gettering, which introduces gettering sites by damaging the backside of the wafer or by depositing a layer of polysilicon, which contains heterogeneous nucleation sites such as dislocations and grain boundaries. Unfortunately, relaxation gettering is not widely used in the PV industry. Most PV substrates have a high concentration of heterogeneous precipitation sites [11] and are therefore difficult to getter using this method.

Segregation gettering is driven by a gradient or a discontinuity in the impurity solubility. A region of higher solubility acts as a sink for impurities from the lower solubility region. The advantage of the segregation gettering is that no supersaturation of impurities is required. Thus, gettering occurs at elevated temperatures where the impurities diffuse quickly. The segregation effect can result from **(a)** a difference in phase, e.g., between crystalline and liquid silicon during crystal growth, **(b)** a difference in material, e.g., aluminum which has a greater solubility for metal impurities than silicon[12], **(c)** the Fermi level effect on solubility of metals[4,13-18], e.g., *Au* in phosphorus doped silicon[16,17,19,20], **(d)** ion pairs, e.g., *Fe-B* pairs[21], **(e)** strain which may increase or decrease the solubility of metal impurities and has been demonstrated to either directly getter metals[22], or influence metal gettering at defects[23].

For photovoltaic silicon substrates, the most common segregation gettering techniques are aluminum and phosphorus gettering. These techniques can be easily incorporated into solar cell production and getter impurities out of the entire active device region, i.e., the entire thickness of the material. Other segregation techniques, which are more suitable for the I.C. rather than for the PV industry, are gettering by heavily-doped substrates (e.g., epitaxial p-films on p^{++} substrates) or implantation proximity gettering.

3 Gettering techniques.

3.1 Internal Gettering

Internal gettering, as practiced in the I.C. industry, uses oxygen precipitates as gettering sites[24]. Oxygen is incorporated into the bulk silicon crystal during Czochralski-type crystal growth primarily from the SiO_2 crucible in concentrations of about 10^{17} to 10^{18} cm^{-3}. This concentration exceeds oxygen equilibrium solubility at temperatures used in device processing and results in precipitation of the supersaturated oxygen. Studies made by Gilles *et al.*[5], Aoki *et al.*[25,26] and Hieslmair *et al.*[27] confirmed

that iron precipitates at oxygen precipitates-related defects and proved that internal gettering is a relaxation-type gettering.

An advantage of internal gettering for the I.C. industry is that no special gettering step is needed since the gettering occurs during cooling from high temperatures during integrated circuit manufacturing. Internal gettering was shown to be effective for removal of all major metal impurities from the active device layer (see Table 1 in Section 4), which is explained by variety of gettering sites introduced by oxygen precipitates, and by the proximity of the gettering region to the device-active layer. However, internal gettering is poorly suited for PV applications. Typically, regions in the bulk PV grade silicon contain high concentrations of defects (relative to I.C. grade silicon) and thus will serve as heterogeneous precipitation sites themselves. Bulk defects which become decorated with metals and metal precipitates are highly recombination active [28,29] and will degrade PV performace.

3.2 External Gettering.

3.2.1 Phosphorus Diffusion Gettering

Phosphorus diffusion gettering is a type of gettering which occurs during in-diffusion of phosphorus through one of the wafer surfaces. It can be accomplished using the carrier gases $POCl_3$, PBr_3 (Ref. [30,31]), P_2O_5 (Ref. [32-35]), or a spin-on source[4,32]. A phosphosilicate glass (PSG) can form on the silicon surface when an oxidizing atmosphere is present. This glass then acts as the doping source for the phosphorus in-diffusion. Phosphorus gettering has been used to improve the purity of both I.C. grade silicon, which resulted in improvements in diode quality[32,36-39] and minority carrier diffusion length[40-42], and PV grade silicon which improved solar cell performance[43-50]. For polycrystalline silicon solar cells, the response of the material to the phosphorus gettering treatment depends on the concentration of structural defects[47,50,51] as well as oxygen and carbon concentrations[45,49,50]. As shown in Table 1, phosphorus diffusion has been successfully applied for gettering of almost all transition metals.

Observations from experimental studies of phosphorus diffusion gettering can be summarized as follows: **(1)** the impurity distribution follows the phosphorus in-diffused profile[20,52,53]; **(2)** dislocations form with extremely high phosphorus concentrations[52,54]; **(3)** little or no metal impurity gettering occurs in the glass layer used for phosphorus in-diffusions[30,31,35]; **(4)** a relationship exists between the carrier gas used for glass formation[30], the growth speed of the glass layer[55], and the amount of impurities gettered; **(5)** impurities precipitate in the phosphorus doped layer[30,34]; **(6)** *SiP* precipitates can form in the near surface region of the phosphorus doped region[34,55,56] and **(7)** a high concentration of *substitutional Co* and *Mn* is observed in heavily phosphorus doped regions[17,57]. Based on these observations, at least four potential mechanisms for gettering were suggested: solubility enhancement by the Fermi level effect, ion pairing, gettering to dislocations, and silicon self-interstitial injection assisted gettering. The first two mechanisms are well understood theoretically. The Fermi level effect[13,58-60] increases the solubility of positively or negatively charged impurities in p^{++} or n^{++} substrates, respectively, without changing the solubility of neutral impurities, thus the total impurity solubility (neutral plus charged) is increased. Ion pairing primarily occurs by Coulombic attraction between the impurity and a charged ion, usually a dopant atom. The exact solubility enhancement generated by ion pairing is difficult to estimate since few studies have been performed on metal impurity pairing with phosphorus atoms, with no studies performed at elevated temperatures. However, the results of Hall and Racette[16] strongly suggest some degree of ion pairing may be occurring in addition to the Fermi level effect. Calculation of the enhancement via ion pairing is possible with the use of a number of simplifications as outlined by Reiss *et al.*[59] Chou and Gibbons[15] have performed calculations for *Au-P* pairs where they note at most a factor of four enhancement via ion pairing.

The last two mechanisms which have been intensively discussed in the recent years are gettering by dislocations, which are formed during phosphorus diffusion and can augment the gettering process via precipitation of the impurities (relaxation gettering)[30,52,54,61,62], and gettering via silicon self-interstitial injection. The injection of self-interstitials can enhance the diffusion of some metal impurity species, e.g., *Au* and *Pt*, via the kick-out mechanism[63], which accelerates the kinetics of the gettering process[8,42,53]. However, the accelerated diffusion does not explain the increase in the total amount of gettered impurities. In addition to this diffusion enhancement, researchers[8,9,34,55,64,65] have provided a theoretical model which suggests phosphorus in-diffusion produces a flux of self-interstitials towards the phosphosilicate glass (PSG)/silicon interface. This flux is speculated to enhance the concentration of interstitial metal impurities above their solubility, thus driving precipitation of the impurities. This precipitation increases the amount of impurities gettered to the phosphorus-doped layer.

Phosphorus gettering was shown to be very effective in removal of all major metal impurities (see Table 1). Some further benefits are realized when phosphorus gettering is combined with another gettering technique. A combination of phosphorus and aluminum gettering has been shown to greatly improve material performance beyond the use of one gettering technique[40,46,49], suggesting a synergistic effect occurs with combined phosphorus and aluminum gettering[66]. Phosphorus gettering has also been successfully combined with *HCl* gettering. This is accomplished by adding trichloroacetic acid into the phosphorus annealing gas. Improvements have been realized for solar cells[51] and CMOS integrated circuit devices[67].

3.2.2 Aluminum Gettering

Aluminum gettering is accomplished by the deposition and subsequent heating of a thin *Al* or *2% Si-Al* film on the backside of a silicon substrate. *Al* gettering has been shown to improve material properties in polycrystalline silicon used for solar cells in thick silicon substrates[50,68-72], and thin film silicon[73] as well as I.C. grade single crystal silicon[50,74-78]. Minority carrier diffusion lengths in these materials can be increased by 100-200 μm while overall solar cell efficiencies have been shown to increase by as much as 0.5-1% (Ref. [79]). The primary mechanism for *Al* gettering is segregation of the impurities from the silicon to the *Al-Si* liquid layer. Most metal impurities, including *Fe*, *Cu* and *Ni*, have a solubility of 1 to 10 atomic percent in *Al* over a wide temperature range[80,81]. Since metal impurity solubilities in silicon are significantly lower, a segregation coefficient of 10^3 to 10^9 is expected, depending on the metal impurity and temperature. Additionally, pitting or damage at the *Si/Al-Si* interface may act as precipitation sites for relaxation gettering of metal impurities[72], although this mechanism has not been directly proven. Furthermore, the annealing of *Al* forms a p^+ layer, which can be used to reflect electrons and avoid recombination at the back surface of silicon solar cells where carrier recombination is unwanted. The reflection process is known as the back surface field (BSF) effect[82,83]. Overall, *Al* gettering is extremely useful and practical in gettering impurities from solar cell silicon, since impurities must be removed from the entire thickness of the material and an *Al* layer is already used as a backside contact. However, *Al* gettering impurities from I.C. device regions is less reasonable due to *Al* junction spiking and the relatively high vapor pressure of *Al*, which can evaporate from the back surface and contaminate the front surface.

Direct measurements of the *Al* segregation coefficient have been made by Apel *et al.*[12] for *Co* in silicon and Hieslmair *et al.*[75] for *Fe* in silicon. Apel *et al.*[12] found 10^3 as a lower bound for the segregation coefficient of *Co* between silicon and an *Al* layer at 820°C. Hieslmair *et al.*[75] found, as a lower bound, segregation coefficients of 10^5 - 10^6 for *Fe* between silicon and an *Al* layer at temperatures from 750 to 950°C.

The efficiency at which *Al* gettering improves material quality is comparable to phosphorus diffusion gettering[46,84,85] as well as gettering to implantation induced cavities[78]. Material properties, such

as minority carrier diffusion length, have been shown to greatly improve for co-gettering with *P* and *Al* (Ref. [40,46,49,86,87]). A synergistic effect has been measured experimentally[49,86] and explained theoretically[66]. It was suggested that the synergistic effect originates from the silicon self-interstitial injection by the phosphorus in-diffusion, which accelerates the gettering process by increasing both the dissolution of metal precipitates and the diffusivity of some impurities. Furthermore, the gettering ability of the *Al* layer is significantly more stable than the *P* layer, due to continued *P* in-diffusion and a decrease in the peak phosphorus concentration. Therefore, when both mechanisms are combined, the gettering action is enhanced.

3.2.3 Backside Damage (BSD) and Poly-Backside Seal (PBS) Gettering

Backside damage and polysilicon backside gettering utilizes gettering sites introduced at the backside of the wafer by mechanical damage of silicon (sandblasting, lapping, etc.)[38,88-90], by laser damage[91,92], by deposition of a polysilicon layer[93-95], or a Si_3N_4 film[95,96]. Gettering by a layer of porous silicon[97], by deposition of germanium[6] or by defects created using impact sound stressing[98] have also been reported. TEM studies[95,99], X-ray topography[92,96,100] and selective etching of the samples[89,101,102] revealed that the damaged layer consists of complicated networks of dislocations, intrinsic stacking faults and regions with intensive lattice strain. Since the structure of the damaged layer was shown to depend significantly on the type and intensity of the damage[90,101] and could vary with high-temperature annealing[96,102], it is very difficult to characterize backside damage gettering mechanism in general or compare different types of damage. Likewise, the physical model of backside damage gettering remains controversial. Currently, there are three models for backside gettering, which most probably all contribute to the actual gettering mechanism to various extents: **(a)** Backside damage gettering is relaxation gettering since backside damage provides an abundance of heterogeneous nucleation sites for precipitation of supersaturated metal impurities[94,100,103-105]; **(b)** Backside gettering is segregation gettering, in which metals are trapped at defects by strain fields or enhanced solubility in the vicinity of structural defects[22,38,93,101,102,106-109]; **(c)** Backside treatments enhance internal gettering[95,110,111] via acceleration of oxygen precipitate growth by absorption of silicon self-interstitials in the damaged layer[112-114]. This last model is still under discussion since some authors argue that mechanically damaged layers inject self-interstitials[111,115].

3.2.4 Chemical Gettering

Chemical gettering consists of high-temperature oxidation anneal (usually between 1000°C and 1100°C) in dry oxygen with small amounts (usually less than 1%) of chlorine-bearing species (Cl_2, HCl, C_2HCl_3, or trichlorethylene). The gettering effect is due to the chlorine in the oxidizing atmosphere which prevents positive alkaline ions from being introduced into the growing oxide through the formation of volatile chloride compounds. Oxidation in the presence of chlorine species was shown to decrease the density of surface states at the Si/SiO_2 interface[116] and to improve breakdown characteristics of MOS capacitors[117]. However, the chemical gettering could only moderately decrease the bulk concentration of metals. Robinson *et al.*[118], Engel *et al.*[119] and Jastrzebski *et al.*[48] studied influence of chemical gettering on minority carrier lifetime and found only small improvements. This was understood after experiments of Baginski *et al.*[120], Ohsawa *et al.*[121] and Honda *et al.*[122], who studied effect of chemical gettering on intentionally contaminated wafers. They found that *Cu* could be easily gettered from the wafers by the addition of *HCl* to the oxidizing ambient, whereas *Au*, *Fe* and *Cr* were not affected.

3.3 Proximity Gettering.

3.3.1 Implantation-Induced Gettering

Metal impurities in silicon can be gettered to regions of implantation, where either the implanted atoms or the implantation damage getters the impurities. Metal impurities are gettered to implanted regions by either a relaxation or segregation type mechanism. Relaxation occurs either at implantation-induced damage or at clusters/precipitates of the implanted species. Segregation can occur to a separate phase formed by a high dose implant, or via the Fermi level effect or metal ion pairing with the implant species, e.g., boron, arsenic or phosphorus implants, or via chemisorption to internal surfaces of cavities formed by implantation with helium or hydrogen.

Gettering has been observed for implantation with silicon[123-129], phosphorus[62,124], carbon[130-135], oxygen[125,134,136-143], helium[134,141,144-149], argon[119,125,136,150-154], neon[152,155], krypton[150], xenon[125,150], hydrogen[127,143,156], boron[126,135,150,157,158], germanium[159,160], chlorine[136], aluminum and chromium[161]. Implant energies range from 50 keV to 10 MeV with implant doses ranging from 10^{13} to 10^{17} atoms/cm^2. The implant atoms usually are light elements in order to avoid amorphization of the near surface region. Although implantation gettering have been shown to be very successful in gettering of all common metal impurities, such as *Cu, Fe, Au, Cr, Ni* and *Pt*, a major drawback to implantation gettering is the required high implant doses, which correspond to undesirably long implantation times and acceptably high price of the gettering treatments, especially for terrestrial solar cells. This can be overcome by development of prospective gettering techniques. For instance, plasma immersion ion implantation allows for rapid implantation of many species, e.g., an implantation of $2x10^{17}$ *H* atoms/cm^2 takes on the order of 2 minutes[141,162].

3.3.2 Gettering by Heavily Doped Substrates

Effective gettering of metal impurities can be achieved with heavily doped substrates. Epitaxial layers $\approx$ 10 μm thick with low to moderate doping are deposited on the heavily doped substrates in order to provide an active region for Integrated Circuit (I.C.) devices. The substrates are typically doped with boron, phosphorus or arsenic depending on the device application. The heavy doping additionally acts as a sink for stray currents between I.C. devices, thus retarding latch-up problems[163]. The substrates possess a higher solubility for metal impurities than the epitaxial layers. The difference in solubility drives segregation of the impurities from the epi-layer into the substrate. Heavily doped substrates effectively getter even with low thermal budgets because the substrates are located in the close proximity to the device region and the substrates act as a continuous sink for impurities.

Heavily doped substrates getter primarily by the Fermi level effect and ion pairing, which increase the solubility of the impurity in the substrate relative to the low or moderately doped epitaxial layer. The Fermi level effect[13,16,17,19,20,58-60,164] increases the solubility of positively or negatively charged impurities in p^{++} or n^{++} substrates, respectively, without changing the solubility of neutral impurities, thus the total impurity solubility is increased. Ion pairing occurs primarily by Coulombic attraction between the impurity and a charged ion, usually a dopant atom. Dislocation formation at the epi-substrate interface[54,165-167] as well as accelerated oxygen precipitation in the substrate[168,169] may enhance the gettering effect even further.

In comparison to other gettering techniques, heavily doped substrates are one of the most effective means to getter impurities in the I.C. industry and were shown to be superior in gettering efficiency as compared to the internal gettering[67,170,171]. These results provide a clear example of the advantages of segregation gettering over relaxation gettering.

3.3.3 Gettering by Si/SiO_2 interface and wafer bonding interface.

During the last few years, silicon wafer bonding has become more and more interesting as a basic technology for silicon-on-insulator (SOI) devices and power electronics[172]. Yang *et al.*[173,174] have shown that the bonded interface of directly bonded FZ silicon wafers is an effective gettering site for gold and copper. However, Kissenger *et al.*[175] showed that internal gettering is significantly more effective than that of the bonded interface. It was speculated[174] that the mechanism of gettering by the bonding interface is essentially the same as gettering by free silicon surface. Surface gettering effects were observed in the literature and were explained by a combination of the following factors: **(a)** the surface acts as a strain free site for the growth of metal-silicides with large volume expansions **(b)** the surface is a sink for silicon self-interstitials, such that metals which need interstitials for diffusion via the kick-out mechanism (like gold or platinum) are trapped, **(c)** near-surface defects (dislocations, oxidation-induced stacking faults, surface contamination by other elements) may serve as nucleation sites for metal precipitation, **(d)** some metals may become trapped in silicon oxide as the oxide grows, and **(e)** segregation to the surface, i.e., surface chemisorption. Yang *et al.*[174] suggested to use this gettering mechanism for proximity gettering. However, one can expect that its efficiency will be rather low since the fabricated IC devices themselves will be competitive gettering sites for the impurities. Furthermore, unlike *Cu, Ni, Cr* and *Pd* (Refs.[176-183]), iron[184] and titanium[185] did not aggregate at the surface in the absence of extended defects.

4 Current State of Understanding of Gettering and Future Trends

Over the last decade, a greater appreciation and study of transition metal gettering has been motivated by **(a)** a deeper understanding of electrical properties and precipitation behavior of transition metals in silicon, gained in the last years **(b)** a continuing reduction of allowable metal concentrations **(c)** an escalation of the I.C. production costs, and **(d)** development of the PV industry which requires low-cost gettering of polycrystalline wafers with high grown-in metal concentrations. Numerous gettering techniques have been studied with respect to the reduction of intentionally introduced metals and to the effect on device yields. Table 1 summarizes the studies in terms of specific metals used and gettering techniques. Almost all techniques have been studied for fast diffusing metals such as *Fe, Cu, Ni, Co*, and *Au*. However, such metals as *V, Ti, Mn, Mo* and *Ag*, have been studied only occasionally. Until recently, the majority of data on gettering had been qualitative in nature. Research efforts have now been shifting towards understanding the physical mechanisms of gettering, obtaining a quantitative description of gettering, and simulating gettering in order to predict metal concentrations. Additionally, it is important both for the PV and I.C. industry not only to develop gettering techniques which work well for a particular metal, but to find techniques or combination of techniques which are capable of gettering nearly all commonly introduced metal impurities.

Since process yield experiments, particularly in the I.C. industry, will become prohibitively expensive in the near future, computer simulations of gettering processes are becoming an important tool for process development and yield optimization. Simulations of the gettering process are achieved within a finite differences diffusion algorithm (see for example Refs.[186-189]) by including equations which describe precipitation and/or segregation of impurities in the gettering region. Diffusion of impurities toward gettering region is described by Fick's diffusion equation. Most approaches[107,190-195] to modeling precipitation in relaxation gettering are based on Ham's fixed radius solution[196] for impurity precipitation. Equations for modeling segregation were suggested by Tan *et al.*[194,197] and Antoniadis *et al.*[198]. Further discussion of mathematical modelling of various gettering techniques can be found in Refs. [8,9,66,115,199-201]. The major difficulty with predictive gettering simulations are to accurately obtain the material parameters such as effective density of precipitation sites n, average radius of the precipitation sites r_0, the segregation coefficient, and sometimes even the impurity diffusivity[202]. Apparently,

determination of the material parameters will become the main target of quantitative studies of gettering in the near future. Additionally, the existing simple models need to be further developed to take into account the complex gettering behaviors of different transition metals and interaction between various defects.

The I.C. industry has in the past relied primarily on internal and backside relaxation gettering to reduce metal impurities in the device region. Future gettering techniques will likely include some type of segregation gettering as well, especially proximity gettering techniques, since it is believed that relaxation gettering alone may not achieve the necessary reduction in metal concentrations with the lower thermal budgets required for very shallow junction formation. The most promising segregation gettering for the I.C. industry is p/p^{++} gettering. The p/p^{++} structure is already necessary to prevent latch-up in certain applications, i.e., CMOS devices, and thus p/p^{++} does not incur extra cost. For other applications, the extra cost of the p/p^{++} structure may be justified if yield is significantly enhanced and/or costly preventative measures can be reduced.

PV industry uses the whole wafer as a device-active region and requires that the transition metals be removed from the whole thickness of the wafer. Thus, segregation gettering techniques such as aluminum gettering or phosphorus diffusion gettering, are very compatible with the solar cell production and have been used in PV industry for a long time. Segregation techniques appear to be the only techniques suitable for polycrystalline silicon materials.

It is now well established that the lifetime in polycrystalline solar cells is limited by intragranular microdefects, which serve as precipitation sites of transition metals or eventually even may consist of transition metals[11,203-205]. Simulations of relaxation gettering showed that an important factor which determines which fraction of transition metals will be removed from the gettering region is the ratio of density of precipitation sites in the gettering and gettered regions[191]. A high density of intragranular microdefects, dislocations and grain boundaries creates competitive precipitation sites in the gettering region and makes relaxation gettering ineffective. On the contrary, segregation gettering does not require impurity supersaturation and relaxation-driven precipitation at the intragranular defects does not occur. Thus, the use of segregation gettering for improvement of solar cells is not only highly compatible with the technological process, but is also physically justified. Aluminum and phosphorus diffusion gettering in PV silicon, currently used by the industry, yields a substantial (up to 1%) improvement is efficiency[51,70,79,206]. However, this obviously does not yet exhaust the potential of gettering in photovoltaics. Further research must be done to understand the first step in gettering of this material, that is, the release and dissolution of impurities from structural defects in the bulk of multicrystalline silicon[207,208]. It was reported that even segregation gettering can not improve the diffusion length in the "bad grains" with low initial diffusion length and high density of intragranular microdefects to the same extent as it improves "good grains"[209]. This implies that either the metals which had precipitated at the microdefects can not be dissolved at the gettering temperature, or there is a competitive segregation of metals to the microdefects, which may be caused, e.g., by their strong strain fields[209]. Understanding of these phenomena and optimization of gettering in the PV industry requires a good deal of fundamental physical understanding of the ongoing processes, which includes understanding of the microscopic origin of the intragranular microdefects[210] and their interaction with the impurities during crystal growth and gettering treatments. Finally, since segregation coefficient is a strong function of temperature, then impurities, trapped in the gettering layer at the optimized gettering temperature, may be partly released during the following heat treatments. Thus, the stability of the gettering sites is an important issue for the studies of gettering.

An emerging trend in the development of gettering is a combination of several gettering techniques. In some cases (as it was discussed above) such combinations have synergetic effect, i.e., the total gettering effect is larger than just a sum of the two treatments alone.

Table 1. Database of references on gettering of transition metals in silicon, classified according to the gettering techniques (columns) and gettered metals (rows).

Metal	Intrinsic gettering	Phosphorus-diffusion gettering	Substrate gettering (e.g., P/P^{++}, N/N^{++})	*Si* surface and Si/SiO_2 gettering, including wafer bonding
Fe	5,23,25-27,111,148,211-224	36,225	17,164,171,226-231	48,179,184
Cu	99,146,213,220,223,232-242	16,30,32,33,36,225	16	97,173,175,178,179,183,232,233,243,244
Ni	8,213,216,221,223,224,236-238,240,245	34,225		179,243,244
Co	223,245	8,35,57,65,246	17	35,65,244
Au	247	8,9,30,31,33,36,37,52,53,62,115,124,151,200,201,248-255	19,20	127,173,174
Cr	211,256,257	258		48,179
Pt		42,252,259-261		262
Pd	214,223,240			244
Ti		185,258,263		185
Ag	264			
Mn	265		17	
Mo		263	230	
V		258		
Device yield	24,39,266-272	32,36-51,206,263,268,273-280	67,170	119

Table 1 (continued).

Metal	Implantation gettering	Backside damage gettering	Chemical gettering	Al-backside gettering
Fe	123,126,128,129,133-135,140-142,147,148,157 ,158,281-285	93,94,111,216,231,286	121,122	75
Cu	123,126,129,134,137-141,143-147,158,160,281,284,287-292	93,97,99	120,121	70,293
Ni	123,139,281,284,294	216		70
Co	123,147,281,282,284,295-298			12
Au	62,95,115,123,124,127,136,141,149,151,152,154,155,243,281,291,292,299-301	113,247,302	120	70,293
Cr	137,139		121	
Pt	144,154,303-306			
Pd				
Ti				
Ag	306			293
Mn				
V				
Device yield	119,125,132,136,150,153,274,307-310	38,70,89,91,92,95,96,101,102,216,268		50,68-70,72-78,311-313

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Minority Carrier Lifetime Determination on As-Sawn Ingot Surfaces of Cz-Si

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ABSTRACT: For lifetime characterization of Czochralski-grown silicon material for photovoltaic use in an early processing stage, an "ingot-lifetime tool" has been designed and built by T.Wang and T. Cizek at NREL [1]. The tool measures lifetimes at the as-sawn ingot surface by a two-contact photoconductivity decay (PCD) method. It is to be shown that this method allows a repeatable measurement and a correlation to the actual bulk lifetime despite poor surface quality. To be fully utilized it must be shown that a lifetime reading prior to cell processing can be related to final cell performance to a degree that a cutoff value for low performance material can be determined. This paper summarizes preliminary results of an ongoing study on the implementation of the ingot lifetime tool in Siemens Solar Industries' Vancouver Washington crystal growing plant.

INTRODUCTION

A key factor for profitable mass production of conventional mono-crystalline Silicon cells is the continuous supply of electronically and economically acceptable feedstock materials. Variation in supply and multiple factors during crystal growth cause variation in grown ingots that may impact the performance of the solar cells. Finding an effective way to identify ingots that will produce low performance cells prior to processing will save manufacturing cost and may allow recycling of the defective material.

We propose to characterize the ingots by the minority carrier lifetime (τ), which is an important parameter of silicon used for photovoltaic purposes. The minority carrier lifetime is limited by impurities and other defects in the crystal and can be significantly altered during the high temperature steps used in cell processing as various studies have shown in recent years [2, 3].

The above mentioned tool measures minority carrier lifetime at the as-sawn ingot surface using a two-contact photoconductivity decay (PCD) method. Early results of the ongoing study on the performance of this tool are reflected in this paper. The second step to be taken for implementation as a quality control tool is to further study the factors causing changes of lifetimes with the cell processes, in order to use lifetimes as a predictor for cell performance.

METHOD

The ingot lifetime tool uses two probes contacting the as-cropped face of an ingot section, ingot tail or ingot neck. A constant current is applied and a voltage change detected. A light pulse shining between the probes generates additional carriers Δn. With the decay of the carriers, the conductivity σ decreases, which is detected as a voltage change ΔV near the probes. ΔV is assumed to be proportional to $\Delta\sigma$ and Δn, the voltage decay profile is then used to calculate the lifetime of the excess carriers. The light source is a 940nm diode laser, pulsed with a sharp signal of 100 µs and a drop-off <100ns. It has a penetration depth of about 0.1mm.

After cropping the ingots, readings are taken at the tails, crowns or the cropped ingot faces. Wiping with IPA is the only standard surface preparation. It is attempted to be shown that the lifetime is not dominated by surface recombination, even though rough surfaces are used. In that case bulk information can be gained if a constant surface condition keeps the influence of surface recombination constant.

RESULTS

(a) Repeatability

A reproducibility study in the form of a balanced Analysis of Variances (ANOVA, see [4]) has shown that the tool was capable of detecting the difference between a) front and back of the ingots and b) between the locations on the face of the ingot. In both cases repeated measurement at the same location is not a significant source of variation. Table 1 shows the data; the P-value is the probability that the source factor is not significant.

Table 1: Repeatability, results of ANOVA

a) **Analysis of Variance for Lifetime. Ingot front and back.**

Source	DF	SS	MS	F	P
Ingot	8	10303.80	1287.97	22.24	**0.000**
Frt/Bck	1	1579.34	1579.34	27.27	**0.000**
ReptUp/Down	2	25.80	12.90	0.22	0.801
ReptOnly	1	15.56	15.56	0.27	0.605
Error	95	5501.38	57.91		
Total	107	17425.88			

b) **Analysis of Variance for Lifetime. Location.**

Source	DF	SS	MS	F	P
Location	3	470.792	156.931	23.67	**0.000**
ReptUp/Down	2	6.750	3.375	0.51	0.610
ReptOnly	1	3.375	3.375	0.51	0.485
Error	17	112.708	6.630		
total	23	593.625			

(b) Separation by material

The tails of over four hundred ingots grown from Remelt, Virgin and Potscrap material blends have been investigated with the lifetime tool. The various materials are used separately in blends. They are typical starting materials for photovoltaic manufacturers. Remelt is scrap material from Cz ingots including tops and tails, Virgin is material that has never been used to grow a Cz ingot. Potscrap is residual melt left in the crucible from previous growth runs. Figure 1 shows the data

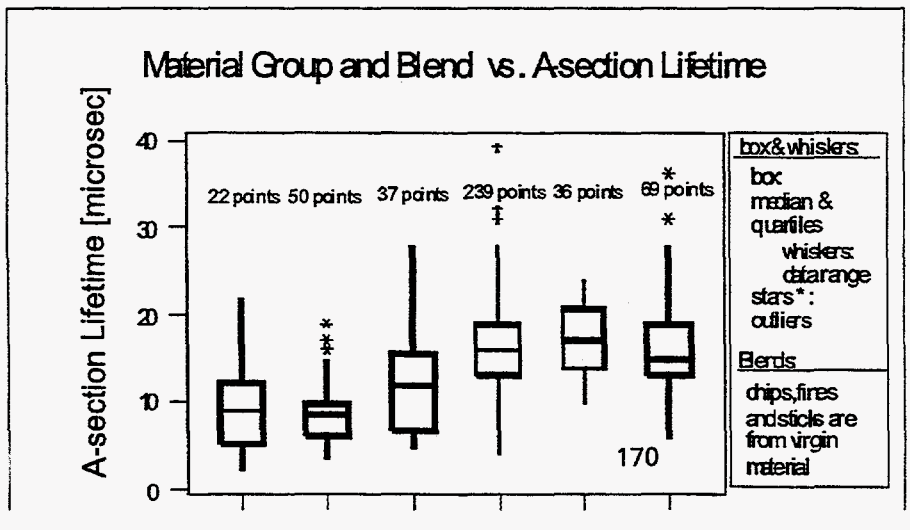


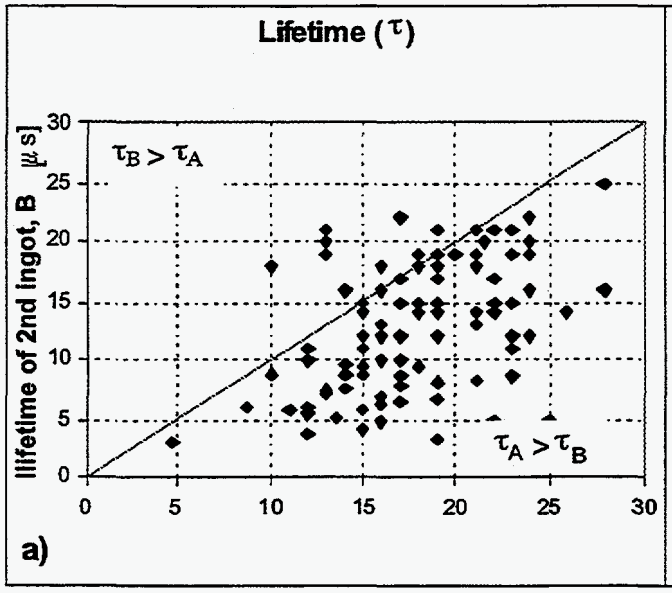
Figure 1: Box-plot for lifetime values taken with the ingot lifetime tool on different material types. Shown are median and quartile data as well as highest and lowest value. There is a significant difference between Potscrap and the other material types.

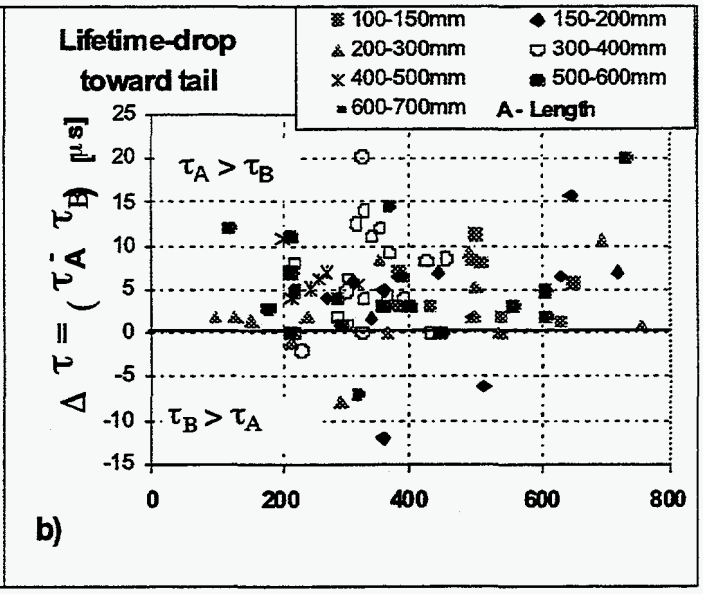
per material. Approximately 60% of the values range from 10μs to 20μs, 2% are 25μs and above

or 5μs and below. Mixtures with Potscrap had lower lifetime values than mixtures with Remelt or Virgin, especially Potscrap mixed with Virgin chips. This difference for Potscrap is statistically significant (at 95% confidence interval for mean, based on pooled Standard Deviation). The tool is therefore capable of detecting differences between some material groups.

(c) Separation by growth direction

During Cz-crystal growth, crystals occasionally lose structure. At that point the ingot (here called ingot A) is tailed and another ingot (ingot B) is grown from the remaining Silicon charge. The tails of more than a hundred of these A and B ingots have been checked for lifetime. The lengths of the B ingots indicate the distance between the measured points and vary between 100 and 800mm. Figure 2 shows this data. The B ingot reading is lower than the A-ingot reading in 90% of the cases, it's average is 4.8μs lower. This may be explained by a lower minority carrier lifetime due to higher impurity levels. Since most impurities have a higher solubility in liquid than in the solid phase, they accumulate in the melt during growth. It is therefore reasonable that ingot B starts out with higher impurity levels than the ingot A. Nevertheless, the lifetime may not always be dominated by point defects (all A-ingots had lost structure, this suggests the presence of other defects at the tail end), which can cause a different behavior, possibly as well a surface condition change. If a systematic error of surface condition caused by material parameters is excluded, the statistically significant shift in distribution indicates that the lifetime reading is





partly reflecting bulk information.

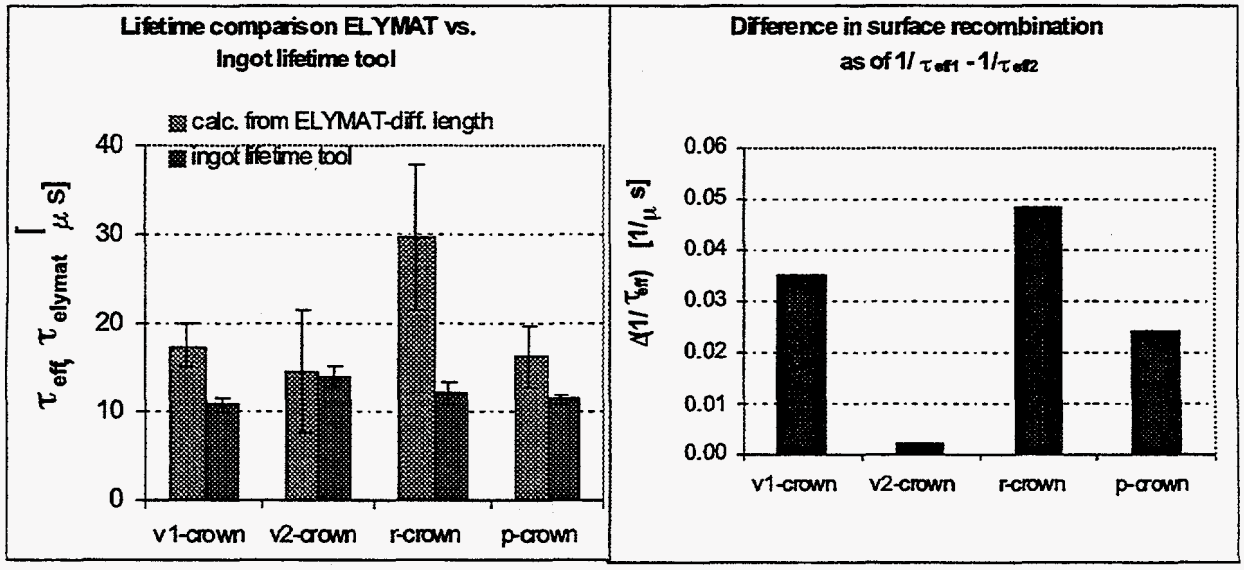
Figure 2a: Lifetime of tail of 1st run vs 2nd run ingots.

Figure 2b: Δτ vs. length of ingots A and B

(d) Correlation with other methods

Due to the poor surface finish for measurement, the readouts of the ingot lifetime tool are likely not to be pure bulk lifetimes. A study is underway to compare lifetimes taken with the ingot tool

to those from surface passivated wafers located adjacent to the ingot ends using RF-PCD and ELYMAT [5] studies. Figure 3 shows preliminary results: Diffusion Length (L_D) data have been taken with the ELYMAT system in HF on wafers located near the crown of four ingots. Lifetimes



have been calculated from L_D and charted against those taken by the ingot tester.

Figure 3a: Lifetime data calculated from Elymat diffusion length are higher than ingot-lifetime-tool measurements.

Figure 3b: Surface recombination difference of the two methods.

The diffusion length maps taken by ELYMAT reveal substantial variation of signal by surface location for the crowns. The averages and distribution (one sigma) are shown as bars in Figure 3a. The ingot-lifetime readings are overall lower than the wafer lifetimes, probably due to surface recombination. Figure 3b estimates the difference in surface recombination of the two methods for each sample, expressed by $\Delta(1/\tau_{eff}) = 1/\tau_{ingot} - 1/\tau_{elymat}$. It has been assumed that the ingot lifetime readings represent a spatial average and surface recombination is the only cause for a difference in reading of the two methods.

CONCLUSION

A reproducibility and repeatability study of the "ingot-lifetime-tool" has shown the system is capable of detecting differences between location on the ingot. The PCD lifetime results taken with this tool on as-cropped ingot surfaces are not completely dominated by surface recombination or variation of surface condition, but contain information of the bulk properties. This is suggested by the capability of the method to quantify differences in lifetime induced by different starting material quality, under the assumption that the crystal quality has no effect on the surface condition. However, the degree of correlation to bulk lifetime needs further study.

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EMISSIVITY MEASUREMENTS AND MODELING - A SUMMARY

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Abstract

A summary of the emissivity measurements and modeling in silicon related materials and structures is presented in this study. The experimental measurements have been performed using a spectral emissometer operating in the wavelength range of 1 - 20 μm and temperature range of room to 1000°C. The influence of (a) dopants (b) roughness (c) overlayers on the emissivity of silicon is discussed. The models available for calculation of emissivity from first principles of optics are described.

Introduction

The current trend in silicon device manufacturing has been to focus on single wafer based manufacturing tools. This is because of a continued decrease in feature size and increase in wafer dimensions. Manufacturing fabs devoted to 300 mm diameter silicon wafers are in fashion today. This coupled with growing interest in large area devices such as solar cells and displays has formed the basis for significant interest in novel process technologies. One such process technique is rapid thermal processing (RTP).

For RTP, pyrometers are the standard sensors of choice for non-contact, real-time process monitoring and control. Pyrometers require knowledge of the emissivity of the material being processed in order to determine the process temperature. Emissivity is a complicated function of wavelength and temperature. It is sensitive to material properties such as resistivity, doping type, surface morphology and presence of overlayers.

Experimental Details

The spectral emissometer, utilized in this study, has been described in detail in several recent papers [1-3]. The schematic of the emissometer is presented in Fig. 1. It consists of a hemi-ellipsoidal mirror providing two foci, one for the exciting source in the form of a diffuse radiating near-blackbody source and the other for the sample under investigation. A microprocessor controlled motorized chopper facilitates in simultaneous measurement of sample spectral properties such as radiance, reflectance and transmittance. A carefully adjusted set of five mirrors provides the optical path for measurement of the optical properties. The source of heating of the samples is provided by an oxy-acetylene/propane torch. The sample size is typically in the range of 0.5 to 1 inch in diameter. The spot size for the optical signal collection from the sample is ~ 3

mm in diameter. The spectral emissometer consists of three GaAs lasers to facilitate in aligning the sample at the appropriate focus. A high resolution Bomem FTIR, consisting of Ge and HgCdTe detectors, interfaced with a Pentium processor, permits data acquisition of the measured optical properties. Further, this on-line computer enables the user to flip the mirrors to acquire transmission/reflection spectra via software configurations such as Spectra Calc and GRAMS.

Results and Discussion

The novelty of the spectral emissometer described in this study lies in its ability to measure simultaneously the sample transmittance, reflectance, emittance and temperature. The accuracy of its temperature measurement capability is limited by the operating temperature of the exciting source, i.e., the diffused blackbody source operating at 900°C, and the sensitivity of the Ge and HgCdTe detectors. The fundamentals of emissivity and the theory of operation of the emissometer have been explained in detail in several recent papers [1-5].

Results of measurements on silicon

The applications of spectral emissometry to obtain emissivity as function of wavelength and temperature are illustrated in the following section. While the measurements are being performed on a variety of samples, the results of emissivity measurements on p-type silicon, with front-side polished, as function of wavenumber for temperatures in the range of 58°C to 962°C, are presented in Fig. 2. These wafers have resistivities in the range of $1\text{-}2\text{x}10^{-2}$ Ω·cm and are 0.61-0.64 mm in thickness. The observed sharp features in the infrared spectra in the wavelength range of 1 μm (10000 cm^{-1}) to 20 μm (500 cm^{-1}) are due to the presence of the following infrared sensitive molecules: (a) C in Si - 607 cm^{-1}, (b) SiO_2 - 1110 cm^{-1} (c) interstitial oxygen in Si - 1130 cm^{-1}, (d) water - 1600 and 3500 cm^{-1}, (e) CO_2 - 2400 cm^{-1} (f) Si_3N_4 - 1206 cm^{-1}. The marrow-band features below 1000 cm^{-1} (10 μm) are due to lattice vibrations in silicon [6]. Spectrum (I), in Fig. 2, at 196°C was measured after heating the wafer to the maximum temperature of 962°C. Comparison of the emittance spectrum (I) to that in (b) indicates reversibility in emittance changes. A similar measurement on a double side polished, n-type lightly doped wafer exhibits interesting properties. As can be seen in Fig. 3, the emissivity of this wafer is negligible at room temperature, while at high temperatures, it approaches that of single side polished silicon. The most change in this measurement is the loss of transmissivity at elevated temperatures, due to increase in free carrier density, with increase in temperature.

In general, our results of the temperature and wavelength dependent emissivity of silicon and comparison with studies in the literature [7]-[15] lead to the following observations: The effect of doping, in general, is to reduce the transmittance. Thus, intrinsic Si exhibits high transmittance. As temperature increases, silicon becomes opaque. Double side polished and lightly doped silicon wafers are IR transparent and can

therefore serve as IR windows at room temperature. With increase in temperature, the transmittance decreases resulting in increased emissivity.

Effect of surface roughness

In Fig.4(a)-(f) the emissivity as measured from the polished side and the rough side of the silicon wafer as a function of wavelength at specific temperatures is shown. As can be seen in these figures the emissivity of the rough side is greater than that of the polished side. This remains the case until the sample becomes opaque to sub-bandgap radiation at temperatures above 700°C. In the range of temperatures investigated, the largest difference in emissivities is observed at 387°C.

Results of emissivity measurements on SiO_2 / Si

Examples of the results of the temperature-dependent emissivity for thin films of SiO_2 on Si in the thickness range of 65 to 500 nm, using spectral emissometry, are presented in Figs. 5-7. In Fig. 5, the measured reflectance, transmittance and emittance are plotted as function of wavenumber for four specific temperatures for SiO_2 / Si with the oxide thickness of 512.4 nm. The spectral features at ~ 1350 cm^{-1} are common to all the SiO_2 / Si samples. This corresponds to a spectral region for SiO_2 where $n \sim 1$ and $k << 1$ [16]. This condition is referred to as the Christiansen effect [17], which has been exploited in the fabrication of Christiansen filters [18]. The effect of oxide layer on silicon is to reduce the transmittance significantly. As the oxide thickness is increased, the transmittance decreases even further. Our results of correlating emissivity with temperature for SiO_2 / Si as function of oxide thickness are summarized for one particular wavelength of $\lambda = 1.53$ μm in Fig. 6. The emissivity of SiO_2 / Si is as shown in this figure. These results of emissivity are plotted as function of oxide thickness for four specific temperatures at $\lambda = 1.53$ μm in Fig. 7. As can be seen in this figure, the emissivity initially increases with oxide thickness and subsequently decreases. The oxide thickness corresponding to this emissivity maximum is independent of temperature for a specific wavelength. Our measurements at $\lambda = 2.5$ μm, on these multilayers, indicate that the oxide thickness corresponding to emissivity maxima shifts toward higher oxide thickness.

Emissivity models

In order to calculate the wavelength and temperature dependent emissivity, a data base of the fundamental optical constants is required. In the literature, there are three commonly used models available. These models are based on the Abeles' matrix method [19]. The MIT / SEMATECH Multi-Rad simulation program utilizes the Abeles' method and incorporates the temperature dependence of the carrier mobilities. Most available models are applicable to double side polished specimens because of the inherent limitations of the inability of accounting for scattering. The model due to Vandenabeele and Maex (VM) [7,20] approaches the spectral properties of single side polished silicon wafers by proposing an empirical effective attenuation factor that is linearly related to the

real transmissivity by a factor of F. The VM model has weaknesses that have been discussed in detail in a recent paper [21]. A model designed to deal with non-planar surfaces by utilizing the matrix theory, the bulk silicon optical constants n and k, and ray tracing techniques has been developed by Sopori [22].

Conclusions

A spectral emissometer operating in the wavelength range of 1 - 20 μm and temperature range of room to 1000°C has been utilized to perform emissivity measurements on silicon and SiO_2 / Si. A brief summary of the available models for calculation of emissivity from fundamental optical constants has been presented.

Acknowledgment

The authors would like to thank SEMATECH, DARPA and NREL for their support of this project.

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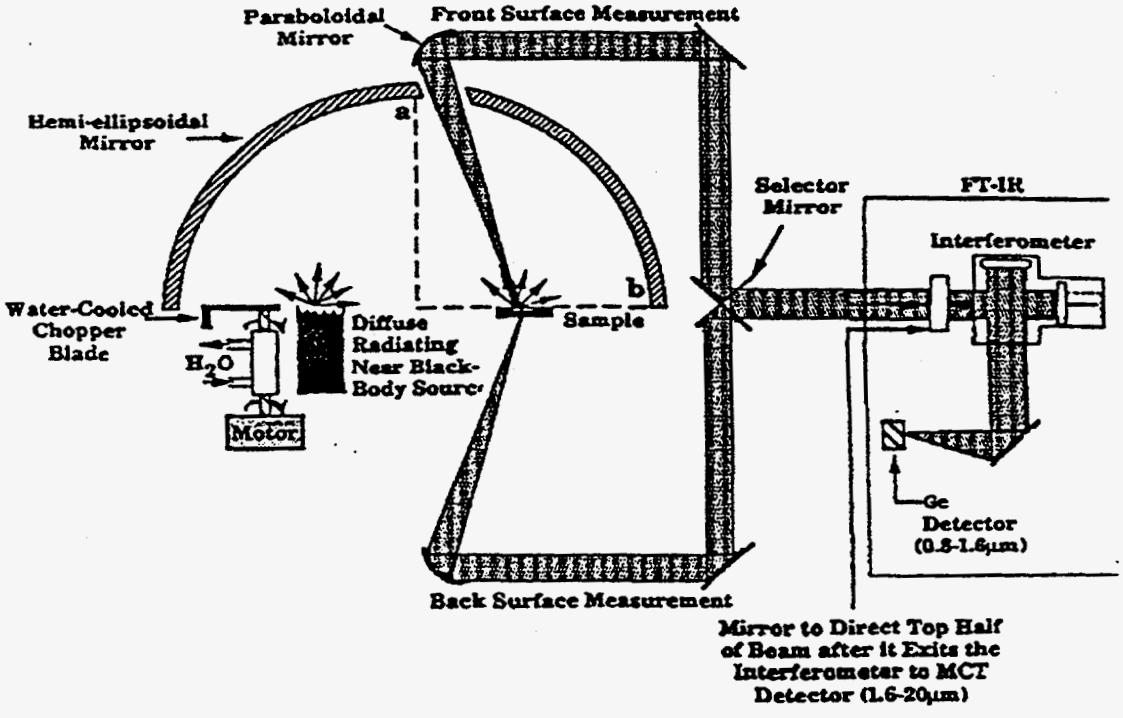

Fig.1 Schematic of bench top emissometer showing components and optical paths for radiance, reflectivity, and transmissivity.

Fig.2 Spectral emittance by closure ($\varepsilon_v = 1 - \rho_v - \tau_v$) for p-type silicon wafer with front side polished, measured in order at temperature up to 962°C. Wafer resistivity = 0.01-0.02 Ω·cm.

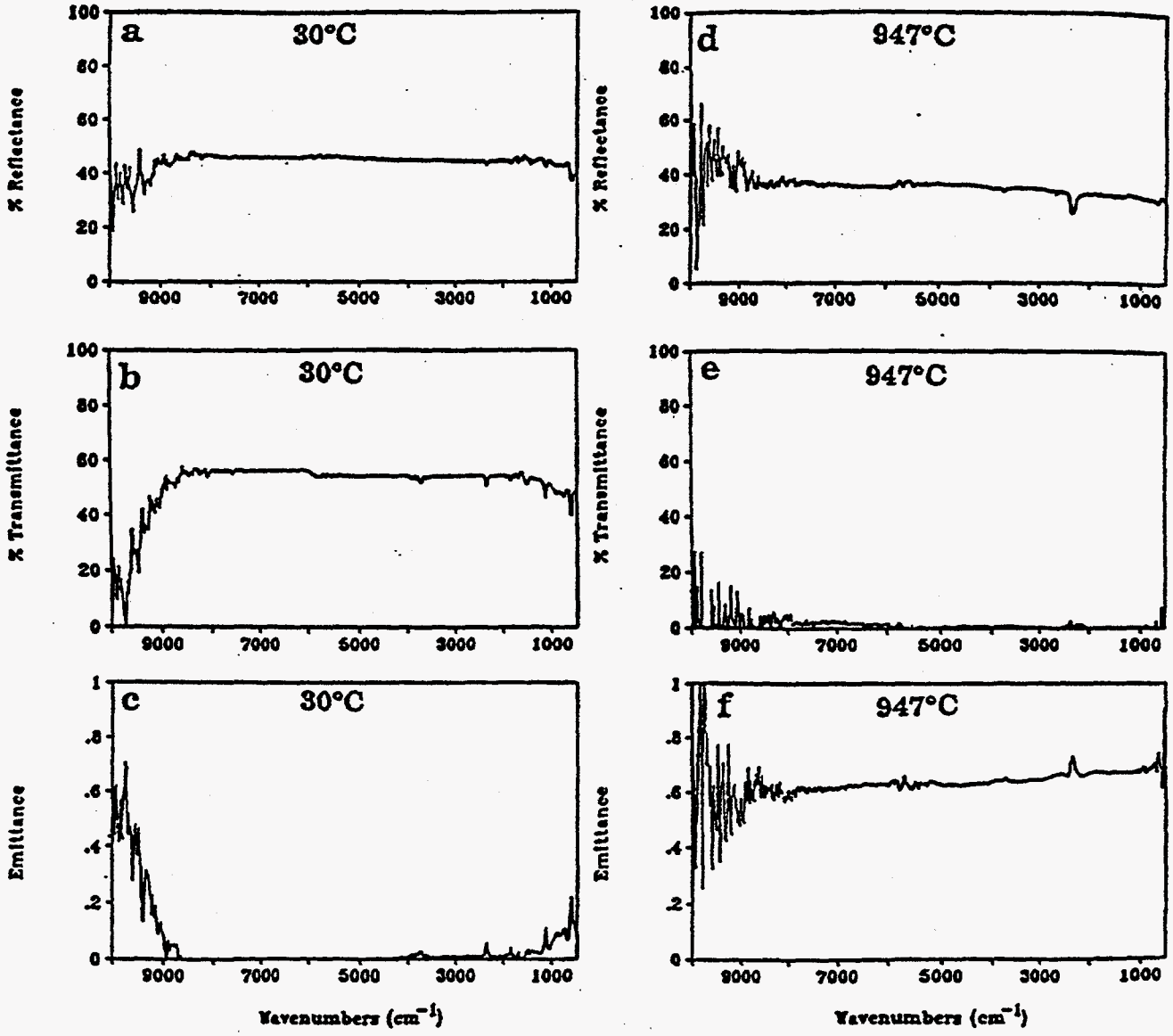

Fig.3 Comparison of measured R, T and ε of a lightly n-type doped silicon wafer (polished both sides) at 30°C (A, B, C) and 947°C (D, E, F).

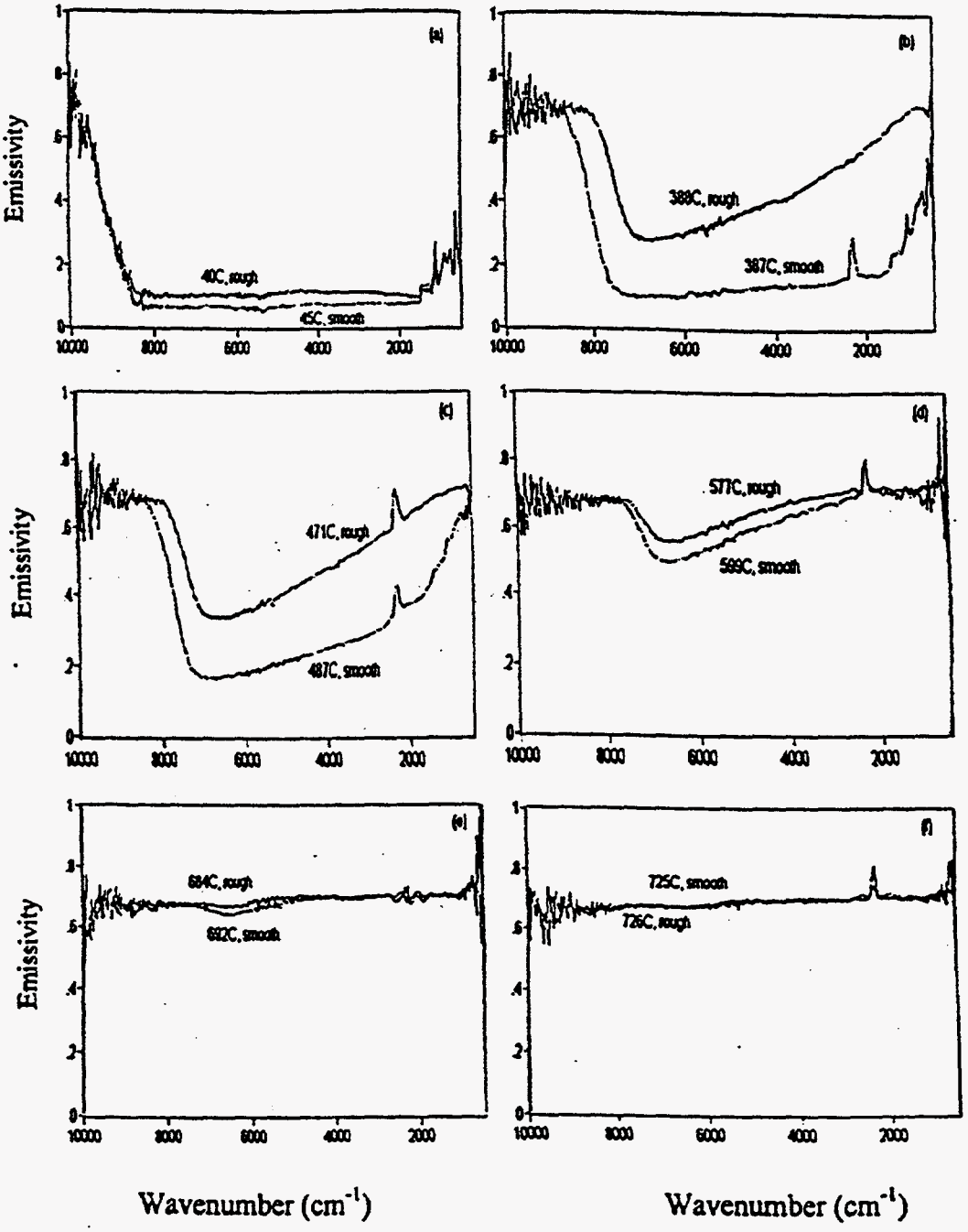

Fig.4 Emissivity of back-rough vs. front smooth sides of n-Si as function of wave-number for specific temperatures: (a) 40, 45°C (b) 388, 387°C (c) 471, 487°C (d) 577, 599°C (e) 684, 692°C and (f) 726, 725°C, respectively.

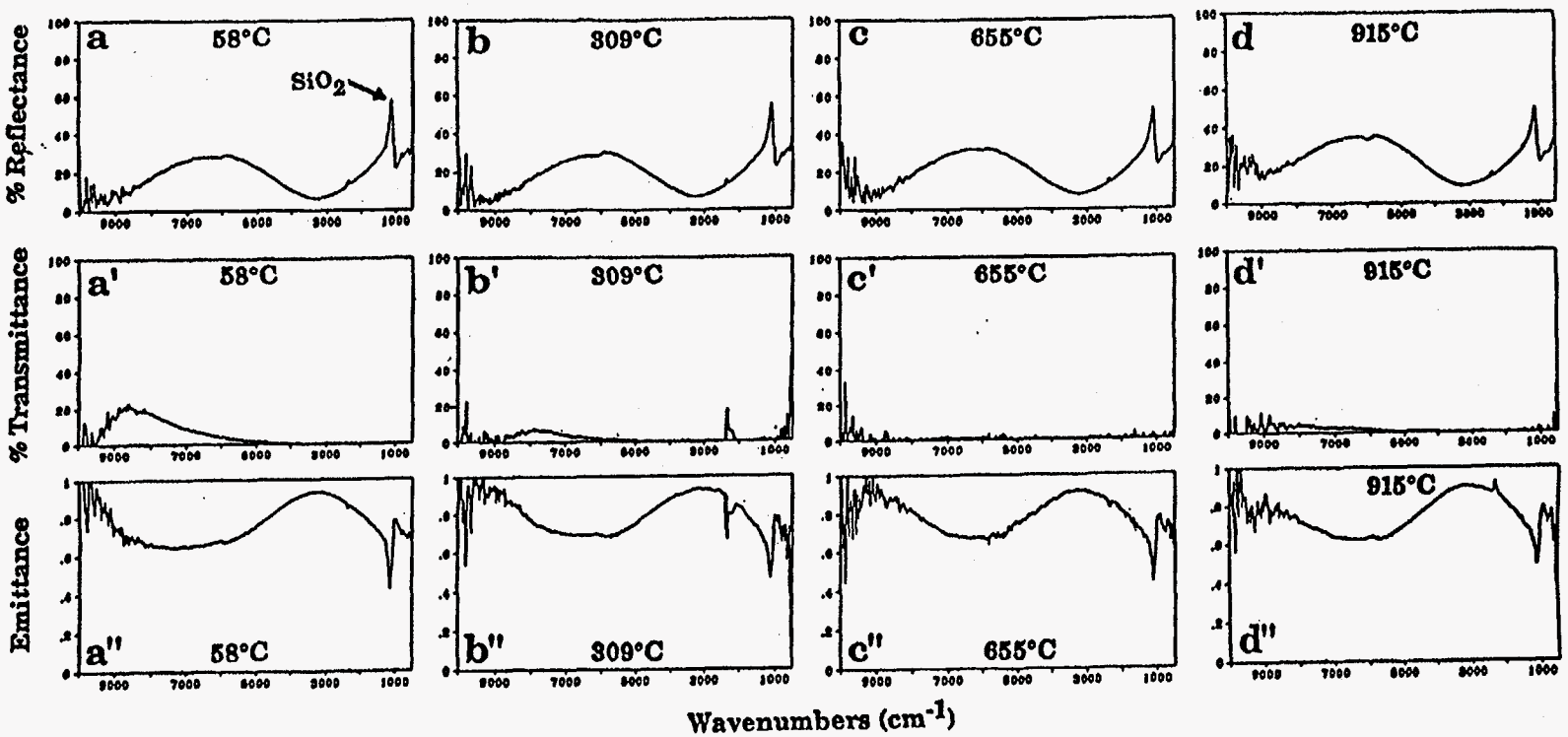

Fig.5 Infrared radiative properties of NJIT silicon wafer 10120B with an oxide thickness (SiO_2) of 5124 A at a's) 58°C, b's) 309°C, c's) 655°C, d's) 915°C,

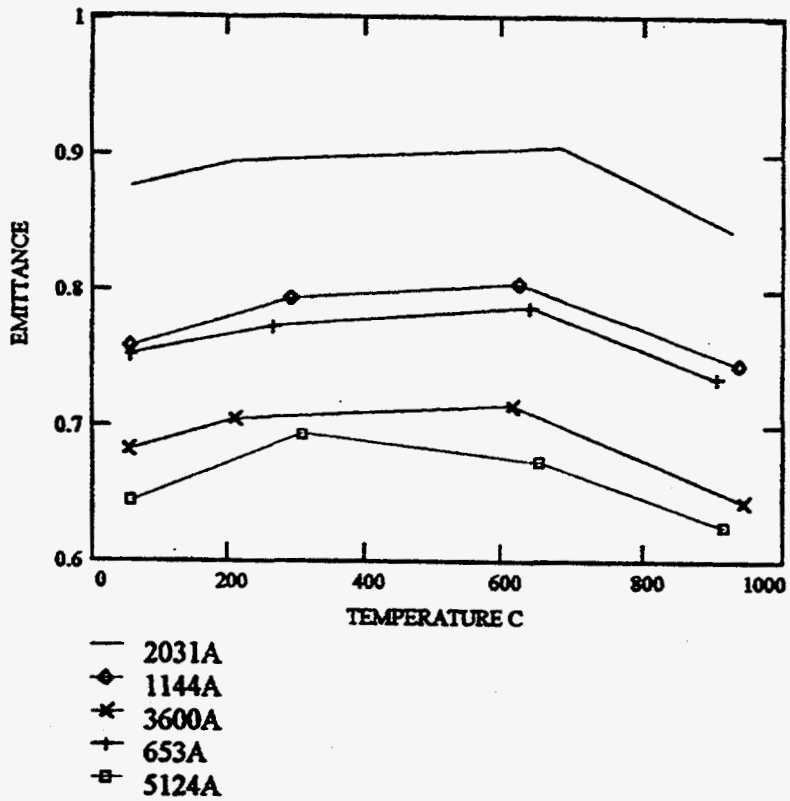

Fig.6 Measured emissivity as a function of temperature for samples with different thickness of SiO_2 coating on silicon at 1.53 μm.

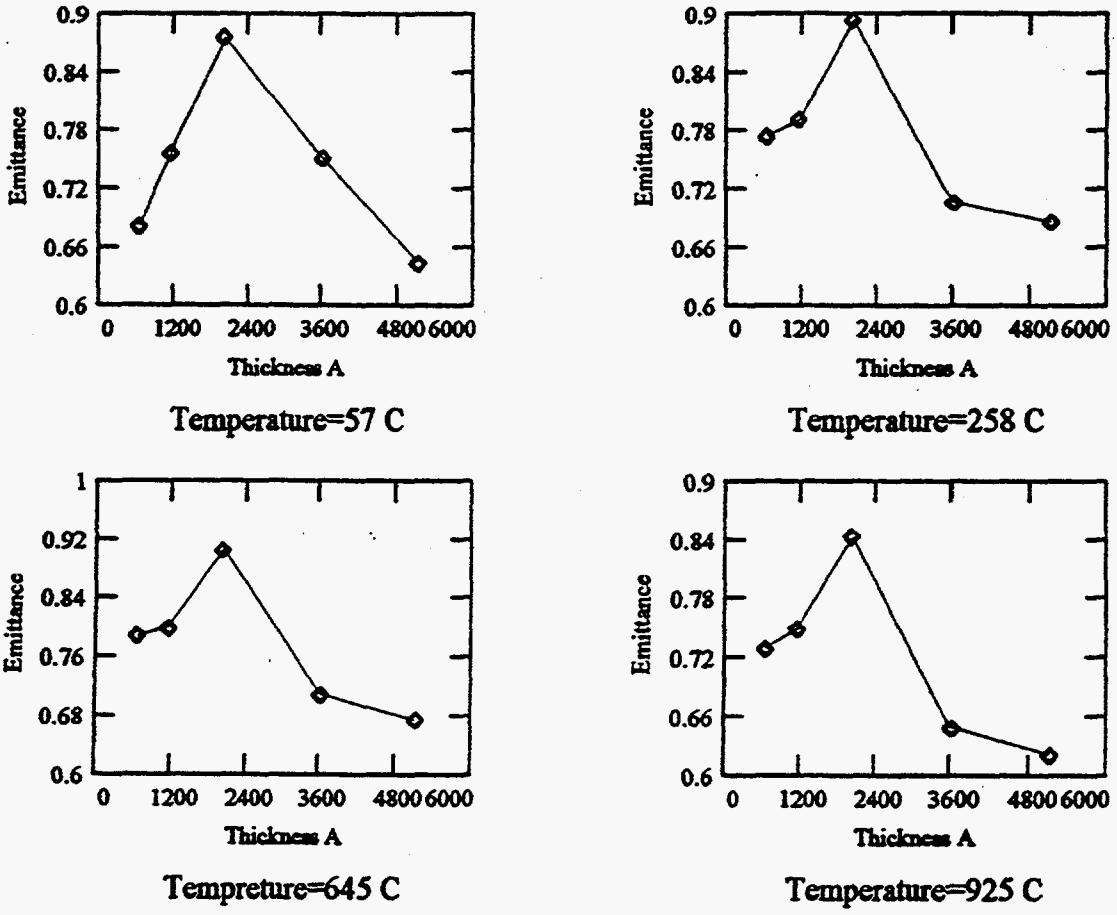

Fig.7 Emissivity versus oxide thickness for four specific temperatures at $\lambda = 1.53$ μm.

SILICIDE ASSISTED CRYSTALLIZATION OF THIN POLY-SI FILMS

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Poster Description:

The use of a thin, 5 nm thick, Ni layer on a-Si, to promote the formation of a lateral recyrstallization front was first reported in 1966 by Lee and Joo [1]

We measured the lateral recrystallization rate at 500 C, using furnace anneals [2] and found it to be 3.5 E-8 cm/sec; this value exceeds by two order of magnitude the solid state epitaxial regrowth rate of amorphous Si measured by Olson and Roth [3]. The activation energy was 0.3 eV [2], much lower than the value of 2.76 eV measured for epitaxial regrowth [3]. A model consistent with our observation is that Ni, at a very low concentration diffuses to the recrystallization front.

Poly-Si formed from a-Si through by induced lateral crystallization, MILC, tends to have a high electron mobility. We measured 87 cm^2/Vs in intrinsic Si. Hydrogenation improved this value to 170 cm^2/Vs [2].

We are currently investigating the MILC of CVD deposited a-Si using rapid thermal processing, RTP, using heat pulses at temperatures around 600 C.

Very preliminary measurements indicate that the activation energy under those conditions increased to about 1.7 eV, see Fig 1. Further measurements are needed to confirm this value. If true, possible reasons would include a change in mechanism, with a different mechanism operating at 600 C than at 500 C and/or photonic effects.

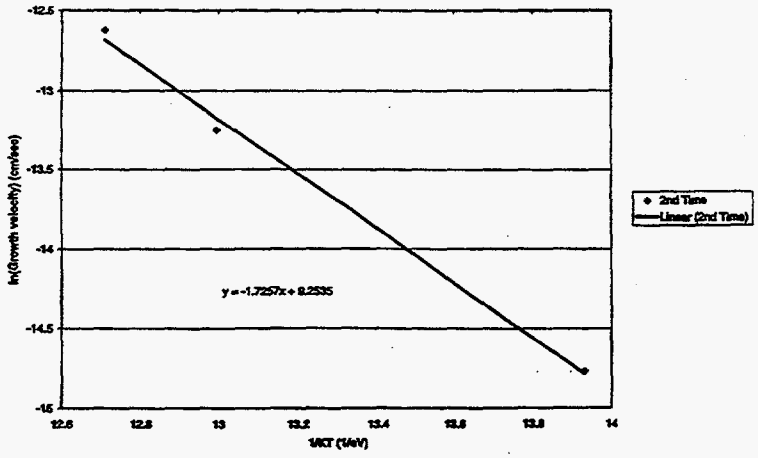

Figure 1. Lateral regrowth velocity of CVD deposited a-Si, as a function of inverse absolute temperature. The fit to the three data points is 1.72 eV. More data are being measured.

Poly-Si thin film transistors have been fabricated in the RTA recyrstallized material, see Fig 2, and are being analyzed. Results obtained will be presented at the poster session.

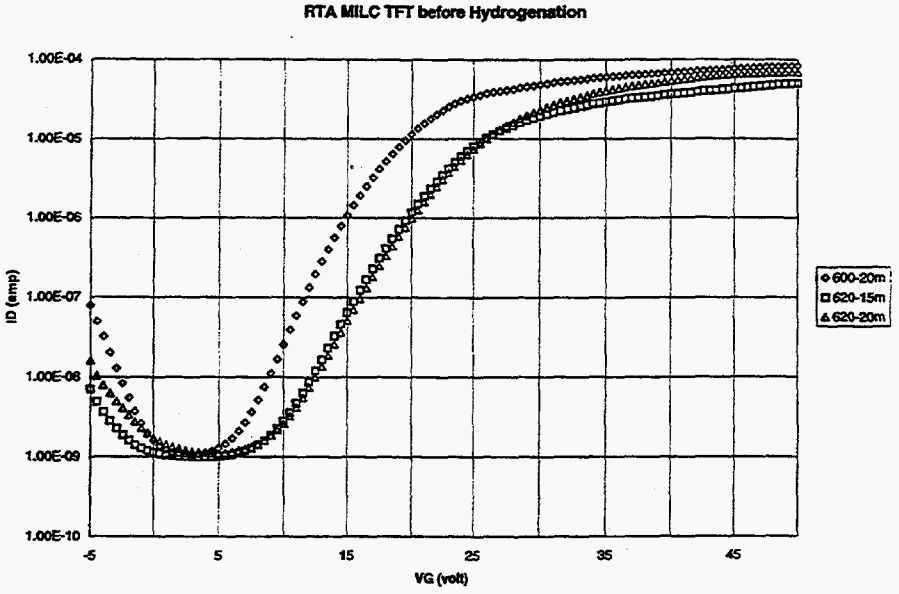

Fig.2 Source drain current of 15 x 15 μm fabricated in RTA, MILC poly-crystalline Si Film transistors as a function of gate voltage. The temperatures used varied between 600 and 620 C and the RTA annealing times between 15 and 20 minutes.

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Nanosized Al and Ag Particulate Contacts to Silicon: Materials Characterization and Preliminary Electrical Results

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Abstract

Our group has been investigating the use of nanoparticle Al and Ag as contacts in solar cell technologies. Toward this end, nanosized Al and Ag powders prepared by an electroexplosion process have been characterized by transmission electron microscopy (TEM), TEM elemental determination by x-ray spectroscopy (TEM-EDS) and TEM electron diffraction (TEM-ED). The Al sample had a bimodal distribution with a substantial oxygen impurity in the polycrystalline particles. The polycrystalline Ag sample was observed to contain no substantial oxygen impurity but had some particle necking. These Al and Ag particles were slurried and tested as contacts to p- and n-type silicon wafers, respectively, after annealing under inert atmosphere about 50 degrees above the respective eutectic temperatures. After mechanical removal of the residue and application of Ag paint, these contacts were characterized by standard I-V analysis. Linear behavior was observed for Ag on n-type Si indicative of an ohmic contact while the Al on p-type Si sample was non-ideal. A wet chemical surface treatment was performed on one nanoparticle Al sample and TEM-EDS indicated a substantial decrease in the O contaminant level. The etched nanoparticle Al on p-type Si films exhibited linear I-V characteristics when subjected to an annealing/contacting procedure.

Introduction

Aluminum to silicon contact metallizations via evaporation of Al or Al-glass screen printed pastes are well established. In certain configurations, these metallizations lead to shading losses that degrade efficiency. Toward this end, a reduction in the present lithographic limitations of screen printed conductors (i.e., line-width > 100 μm) [1] could serve to enhance overall solar cell performance.

The use of metallic inks that are comprised of nanosized particles could lead to smaller linewidths. This could be realized by tailoring the ink properties for screen printing with appropriate optimization of the lithography process. Given suitable characteristics of the nanoparticles, both physical (i.e., no particles > 0.5 μm in diameter) and chemical (i.e., appropriate reactivity), this approach also may be amenable to ink jet printing. We report in this paper our preliminary results of research aimed at the development of such metallic nanoparticle-based inks.

Experimental

Nanopowders of Al and Ag were obtained from Argonide Corp. after preparation by Russian scientists via the electroexplosion (i.e., exploding wire) process. The Al sample was shipped under kerosene while Ag was received as a dry powder. Samples were prepared for TEM by sonication of isopropanol slurries of dried powders. P-type Si (Wacker, 3.3 Ω•cm) and n-type Si (Wacker, 2.9 Ω•cm) were etched with 5% HF and rinsed with deionized water. The samples for annealing studies were prepared by dropping toluene slurries of the metallic nanoparticles onto the Si substrates using a modified disposable pipette in a He-filled glovebox. The nano-Al on p-type Si samples were annealed at 645-650 °C for 1 h under Ar while the nano-Ag on n-type Si samples were annealed at 882 °C for 1 h under Ar. After annealing, the deposits were crumbly and did not provide electrical contact. The residues were removed using an isopropanol-wetted cotton swab and Ag paint was applied to the alloyed areas and also to non-reacted areas on the Si to provide a control. Electrical testing of the areas showed activity in the areas where the nanoparticles had reacted but none in the control spots. IV characterization was performed using an Optical Radiation Corporation Solar Simulator 1000 and computer-controlled I-V instrumentation.

Results

The nano-Al was characterized by TEM with representative results shown in Figure 1. Two separate fractions were isolated by mixing the nano-Al in methanol and decanting the top fraction (fines) from the bottom fraction (coarse). The fines fraction (Fig. 1a) is characterized by a bimodal distribution with ~50% spheres 50-100 nm in diameter and ~50% non-spherical Al <10 nm in diameter. The coarse fraction (Fig. 1b) is composed of ~90% spheres and ~10% non-spherical Al 50-300 nm in diameter. TEM-ED indicated these particles are crystalline while TEM-EDS shows Al and a major O contaminant.

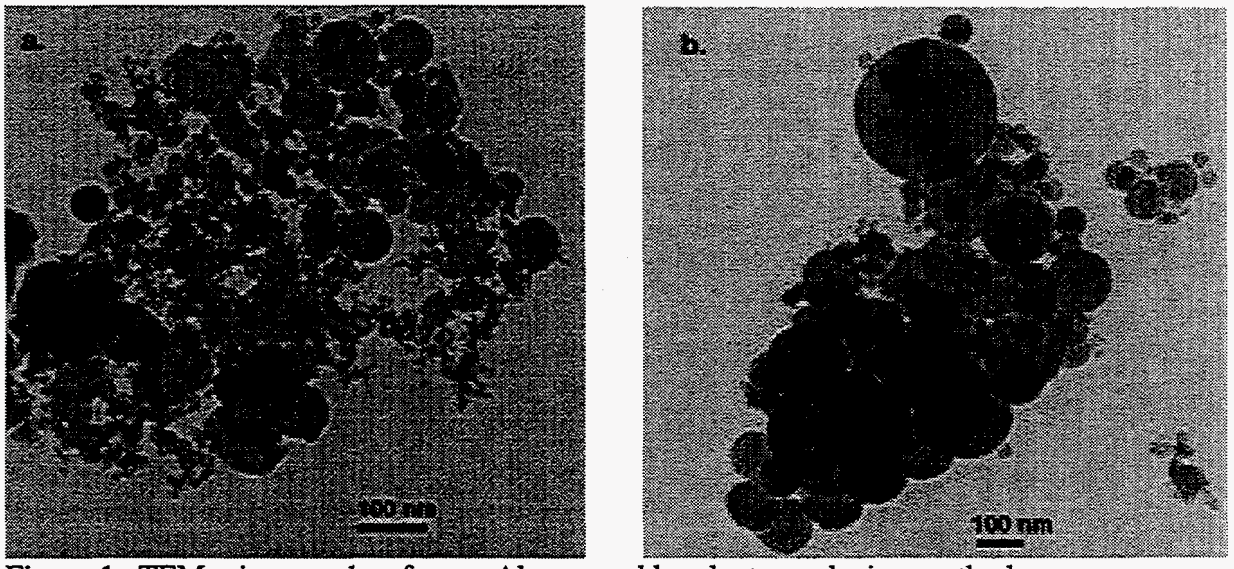

Figure 1. TEM micrographs of nano-Al prepared by electroexplosion method.

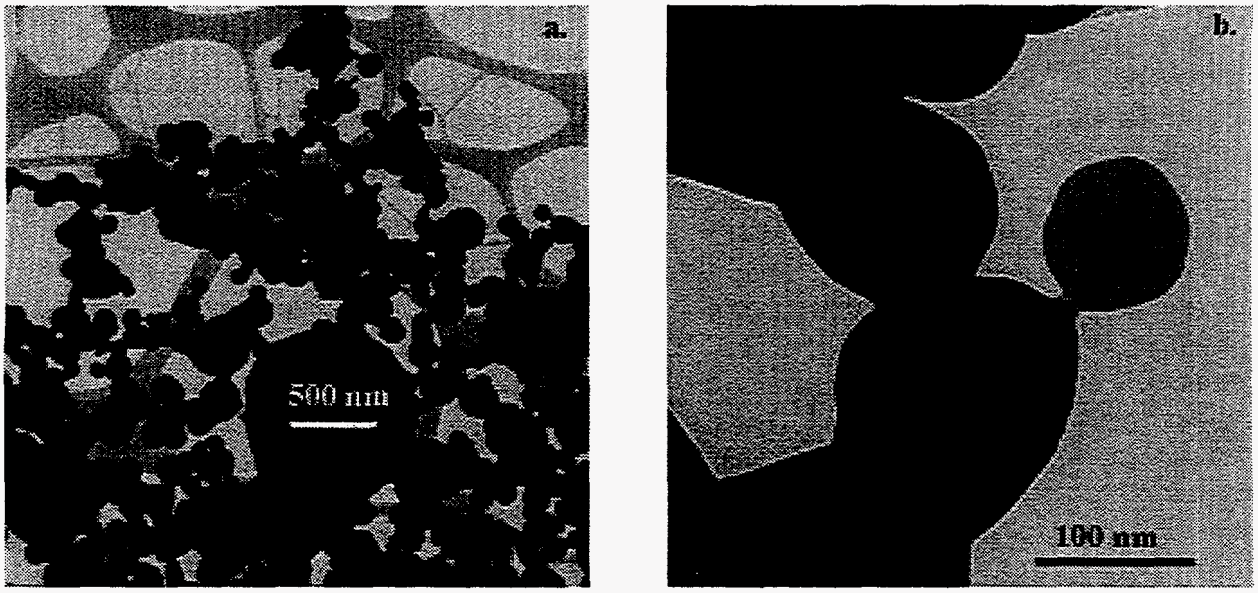

Figure 2. TEM micrographs of nano-Ag prepared by electroexplosion method.

The nano-Ag sample characterized by TEM consists of agglomerates mostly 100-300 nm in diameter with some particles > 500 nm (Fig 2a). Necking of the particles is observed (Fig. 2b) and the sample is crystalline by TEM-ED and contains no O impurity by TEM-EDS.

The nano-Al and nano-Ag were applied onto p- and n-type Si, respectively, and subjected to annealing (see above). Figure 3 shows IV characterization of these films after annealing. The nano-Al to p-Si sample (Fig. 3a) shows a slight deviation from linearity while the nano-Ag to n-Si sample (Fig. 3b) exhibits a linear response curve indicative of an ohmic contact.

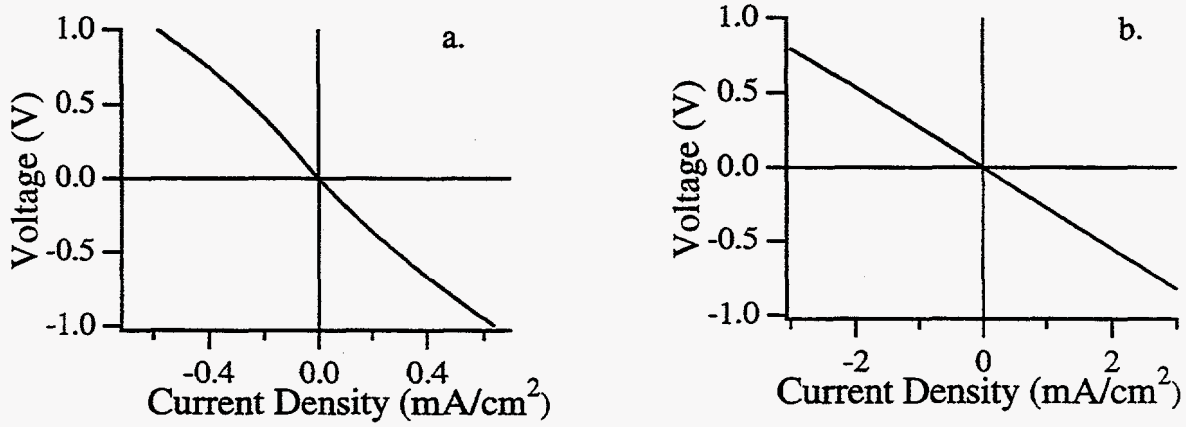

Figure 3. IV characterization of (a) nano-Al to p-type Si and (b) nano-Ag to n-type Si contacts.

In an effort to produce an ohmic contact to p-type Si using nano-Al, surface chemistry experiments were performed. After a proprietary wet chemical treatment, the nano-Al was observed to contain a much lower amount of O impurity by TEM-EDS. This treated nano-Al was next applied as a contact to p-type Si and annealed as above. IV characterization of this sample shows a marked improvement in the ohmic character of the treated nano-Al (Fig. 4) versus untreated nano-Al (Fig. 3a).

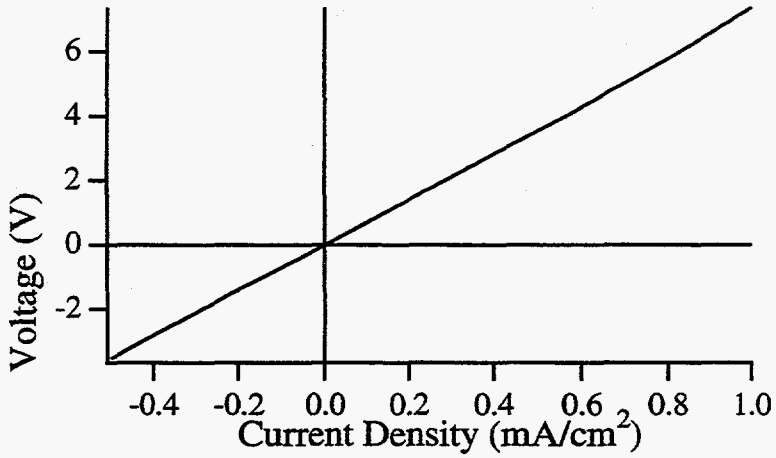

Figure 4. IV characterization of chemically-treated nano-Al to p-type Si contact.

Conclusions

Nanosized Al and Ag prepared by electroexplosion have been successfully applied as contacts to silicon. The degree of ohmicity of the contact appears to be related to the amount of oxide on the surface of the particles. A surface passivation treatment has been developed that removes the corrosion layer on nano-Al allowing ohmic contact to p-type Si. Further development of this technology could impact the solar cell industry through ink jet printing of contacting lines or through novel screen printing approaches.

Acknowledgments

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Some Thermochemical Calculations on the Purification of Silicon Melts

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INTRODUCTION

The availability of polysilicon feedstock has become a major issue for the photovoltaic (PV) industry in recent years. Most of the current polysilicon feedstock is derived from rejected material from the semiconductor industry. However, the reject material has become rare and more expensive during the recent major expansion in the integrated-circuit industry [1]. Although the economic downturn in the integrated-circuit industry may have increased the availability of the reject material to the PV industry in the past year, the continued rapid expansion of the PV crystalline-silicon industry will eventually require a dedicated supply of polysilicon feedstock.

The photovoltaic industry can accept a lower purity polysilicon feedstock ("solar-grade") compared to the semiconductor industry. The purity requirements and potential production techniques for solar-grade polysilicon have been reviewed [2]. Processes to purify metallurgical-grade silicon, which is very inexpensive but has very high concentrations of B, P, and metallic impurities, are of particular interest.

One interesting process from previous research involves reactive gas blowing of a molten silicon charge. Gas blowing refers to introduction of the gas into the melt through either an immersed injector or blowing gas over the surface of a rapidly stirred melt. Dosaj *et alia* reported a reduction of metal and boron impurities from silicon melts using reactive gas blowing with O_2 and Cl_2 [3]. The same authors later reassessed their data and the literature, and concluded that Cl_2 and O_2/Cl_2 gas blowing are only effective for removing Al, Ca, and Mg from the silicon melt [4]. Researchers from Kawasaki Steel Corp. reported removal of B and C from silicon melts using reactive gas blowing with an O_2/Ar plasma torch [5]. Processes that purify the silicon melt are believed to be potentially much lower cost compared to present production methods that purify gas species.

In this paper, we will report the results of some chemical equilibrium calculations relevant to the purification of silicon melts. The purpose of the calculations is to help guide the experimental investigations, and to understand the purification process. At this point, we have only examined C, B, and P removal.

DESCRIPTION OF THE CALCULATIONS

The equilibrium calculations were done using EQUIL [6], which is a CHEMKIN [7] implementation of STANJAN [8]. This code determines the equilibrium state by minimization of free energy, so the input is a list of chemical species and their thermochemical properties as a function of temperature rather than a list of reactions.

We investigated several gases (O_2, H_2O, HCl, and N_2) for removal of impurities from molten silicon by reactive gas blowing. These investigations required thermochemical data for as many chemical species composed of Si, B, P, C, H, O, Cl, and/or N as possible. Roughly 600 species were considered (Table 1). A species was considered if thermochemical data could be readily obtained either from standard sources such as the JANAF Tables [9], the CHEMKIN Thermodynamic Database [7], or from quantum chemistry calculations [10]. In general, carbon and silicon compounds are more thoroughly covered than boron and phosphorus compounds.

The calculations used a starting solid mixture of Si with 10^{-3} C(s) and 2.5×10^{-5} mole percent each of B(s) and P(s). Calculations were done for the above starting silicon mixture and with the following gases, where the gas concentration is in mole percent:

1. 0.05 O_2
2. 0.05 H_2O
3. 0.05 HCl
4. 0.04 N_2, 0.01 O_2, and 0.05 Ar
5. 0.05 N_2, 0.01 H_2O, and 0.05 Ar
6. 0.05 N_2 and 0.05 Ar

The calculations were performed over a range of temperatures (1700-2000K) and pressures (0.001-1.0 atm). For each gas mixture, a few calculations were performed at the extremes of temperature and pressure

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to determine which chemical species from Table 1 could be eliminated before running the complete set of calculations. A chemical species was eliminated if the species mole fraction at equilibrium was less than 10^{-5} of the relevant impurity starting mole fraction (i.e. equilibrium mole fractions of 10^{-10} for B and P species, and 10^{-8} for C species).

Although the code provides detailed information on the equilibrium composition by chemical species, we generally analyzed the results in terms of the fraction of each element in the gaseous, liquid or solid phase. Figure 2 shows an example of such an analysis for blowing-gas mixture 4.

RESULTS

Substantial differences in the distributions of B, P, and C among the phases were observed for the different reactive gas compositions, temperatures and pressures. Under the assumptions that the phases can be separated and that reactive-gas blowing system reaches chemical equilibrium, these calculations indicate the following.

Carbon: C tends to form solid SiC – particularly at higher pressures (1 atm). It should be noted that solid SiC might be difficult to separate from the silicon melt due to its similar density [11]. At lower pressures and in oxidizing ambients, the C was efficiently removed as gaseous CO.

Phosphorus: P may be removed at lower pressure and higher temperature through evaporation. It is not affected much by changes in blowing gas chemistry except in the presence of nitrogen, where some gaseous PN is formed at low pressures.

Boron: Removal of B exhibited very strong relationship to the gas ambient, temperature, and pressure. The oxidizing ambients were only moderately successful at reducing B concentrations (about 50% reduction) by formation of gaseous HBO and B(s). Ambients containing N_2 at 1 atm may be more successful, where the B concentration was reduced by over 90% by formation of BN(s).

SUMMARY

Thermochemical equilibrium calculations can be a helpful tool in developing strategies for using reactive gas blowing to remove impurities in polysilicon. Initial calculations predict that N_2 blowing will be more effective than oxidizing ambients in removing B from silicon melts. Future calculations may include metallic impurities like Fe.

We have also begun experiments examining reactive gas blowing of molten silicon. The experiments were performed in the Liquid Metals Processing Laboratory at Sandia National Laboratories. Experiments have consisted of melting the silicon in a vacuum induction furnace using a graphite crucible coated with yttria. Once the 45-kg sample charge is melted, gas is blown onto the surface using a tantalum lance. Initially, the lance was to use submerged injection, but the violence of the gas expansion at this temperature precluded this. Given the high level of stirring due to the inductive stirring, it was concluded that surface blowing would be sufficient to expose silicon surface area to the gas. To date, experiments have been conducted using argon, nitrogen, and air injection. Sample analyses have not yet been completed.

ACKNOWLEDGEMENTS

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11. C.P. Khattak, private communication.

Table 1. List of chemical species considered in the thermochemical equilibrium calculations.

Gas:

H H_2 O O_2 O_3 OH H_2O HO_2 H_2O_2
Cl Cl_2 HCl HOCl

Si Si_2 Si_3 SiH SiH_2 SiH_3 SiH_4
H_3SiSiH H_2SiSiH_2 H_3SiSiH_3
Si_2H_2 Si_2H_3 Si_2H_5 Si_3H_8

$SiClH_3$ $SiCl_3H$ $SiCl_2H_2$ HSiCl SiH_2Cl $SiHCl_2$
SiCl $SiCl_2$ $SiCl_3$ $SiCl_4$ Si_2Cl_5 Si_2Cl_5H Si_2Cl_6
$HCl_2SiSiCl_2H$ $Cl_2SiSiCl_2$ $Cl_3SiSiCl$ Cl_3SiSi
$Cl_2SiSiCl$ Cl_2SiSi ClSiSiCl ClSiSi HSiSiCl

C CH CH_2 CH_3 CH_4
C_2 C_2H C_2H_2 C_2H_3 C_2H_4 C_2H_5 C_2H_6
C_3 C_3H_2 C_3H_4 C_3H_6 C_3H_8
C_4 C_4H C_4H_2 C_4H_6 C_4H_8 C_4H_{10}
C_5 C_5H C_5H_2 C_5H_5 C_5H_6 C_5H_{12}
C_6H C_6H_2 C_6H_3 C_6H_4 C_6H_5 C_6H_6 C_6H_7
C_6H_{10} C_6H_{14} C_8H C_8H_2
CH_2CHCCH CH_2CHCCH_2 CH_2CHCH_2 $CH_2CHCHCH$
$CH_2CHCHCH_2$
CH_3CC CH_3CCCH_2 CH_3CCCH_3 CH_3CCH_2 CH_3CHCH H_2CCC
CH_3CH_2CCH $CH_3CH_2CH_2CH_3$
$H_2CCCCCH$ H_2CCCCH H_2CCCCH_2 H_2CCCH
HCCCHCCH HCCHCCH

CCl CCl_2 CCl_3 CCl_4 C_2Cl_3 C_2Cl_5 C_2Cl_6
CHCl $CHCl_2$ $CHCl_3$ CH_2Cl CH_2Cl_2 CH_3Cl
C_2HCl C_2HCl_5 CCl_2CH CCl_3CClH_2
CCl_3CH_2 CCl_3CHCl CH_2CCl CH_2CCl_2
CH_2CHCl CH_2ClCCl_2 CH_2ClCH_2 CH_2ClCH_2Cl
$CH_2ClCHCl$ $CH_2ClCHCl_2$ CH_3CCl CH_3CCl_2
CH_3CCl_3 CH_3CH_2Cl CH_3CHCl CH_3CHCl_2
$CHCl_2CCl_2$ $CHCl_2CH_2$ $CHCl_2CHCl$ $CHCl_2CHCl_2$
CHClCCl CHClCH CHClCHCl
Cl_2CCCl_2 Cl_2CCHCl ClCCCl HCCCl

CO CO_2 C_2O C_3O_2
HCO HCOOH $HOCH_2OH$ HOCO $OC(OH)_2$
CH_2O CH_2OH CH_3O CH_3OH
HCCO HCCOH OCHCHO CH_2CO CH_2HCO
H_2CCH_2OH H_2CCHO CH_3CH_2O CH_3CHOH
CH_3CO CH_3HCO CH_3OCH_3
H_2C_4O C_6H_5O C_6H_5OH

Cl_2CO Cl_2COH Cl_2HCO Cl_3CO Cl_3COH
ClCO ClCOH ClH_2CO ClHCO ClO ClOCl ClOO
CCl_2CClO CCl_2CClOH CCl_2HOO CCl_2OHCH_2
$Cl_2OHCHCl$ CCl_3CClO CCl_3CHO CCl_3OO
$CClH_2OO$ CH_2CClOH $CH_2ClCClO$ CH_2ClCHO
CH_2OHCCl_2 $CH_2OHCHCl$ $CH_3C(O)Cl$ CH_3CClO
CH_3OCl CHClCClOH CHClCHOH CHClOH
$CHClOHCH_2$ $CHClOHCHCl$ $CHCl_2CClO$
$CHOHClCCl_2$ Cl_3CCO ClCCO $ClCH_2OH$
H_2CCClO HClCCClO HClCCHO Cl_2CCHO
Cl_2CHOH

SiC SiC_2 SiCH $SiCH_2$ $SiCH_3$ Si_2C SiCCH
HSiC $HSiCH_2$ $HSiCH_3$
H_2SiC H_2SiCH H_2SiCH_2 H_2SiCH_3
H_3SiC H_3SiCH H_3SiCH_2 H_3SiCH_3
HSiCCH H_2SiCCH H_3SiCCH
H_2CCHSi $H_2CCHSiH$ $H_2CCHSiH_2$ $H_2CCHSiH_3$
$H(CH_3)SiCH_2$ $H_2Si(CH_3)_2$ $H_2Si(CH_3)CH_2$
$HSi(CH_3)_2$ $HSi(CH_3)_2CH_2$ $HSi(CH_3)_3$
$Si(CH_3)_2$ $Si(CH_3)_3$ $Si(CH_3)_3CH_2$ $Si(CH_3)_4$
$SiH_3SiH_2CH_3$ CH_3SiH_2SiH $CH_3SiH_2SiH_2CH_3$

CH_2SiCl CH_2SiCl_3 CH_2SiH_2Cl CH_2SiHCl_2
CH_3SiHCl_2 CH_3SiCl CHSiCl $CHSiCl_2$ $CHSiCl_3$
$CHSiH_2Cl$ CHSiHCl $CHSiHCl_2$ Cl_2SiCH_2
Cl_2SiCH_3 Cl_3SiCH_3 CSiCl $CSiCl_2$ $CSiCl_3$ $CSiH_2Cl$
CSiHCl $CSiHCl_2$ $H_2ClSiCH_3$ $H_2ClSiSiCl_3$
HCl_2SiCH_3 $HClSiCH_2$ $HClSiCH_3$
$Cl_2Si(CH_3)_2$ $Cl_2Si(CH_3)CH_2$ $Cl(CH_3)SiCH_2$
$ClSi(CH_3)_2$ $ClSi(CH_3)_2CH_2$ $ClSi(CH_3)_3$
$H_2CCH(SiCl_2H)$ $HClSi(CH_3)_2$ $HClSi(CH_3)CH_2$
$HCCSiCl_2H$ $SiCl_3CH_2CH$

SiO SiO_2 -SiOSiO- Si_3O_3 Si_4O_4
HOSi HSiOH HSi=O H_2SiO SiH_2OH H_3SiO
H_3SiOH SiH_2OH_2 $SiH(OH)_3$ $Si(OH)_4$
HOSi=O HSi(=O)O HSiOO SiOOH $HSiO_2$
$Si(OH)_2$ HSiOOH HSi(O)OH H_2SiO_2
H_2SiOOH $SiH(OH)_2$ SiH_3O_2 $SiH(OH)_2O$
$SiH_2(OH)O$ $SiH_2(OH)_2$ SiH_3OOH $HOSiO_2$
$O=Si(OH)_2$ $Si(OH)_3$ $Si(OH)_3O$ $H_2Si(O)_2SiH_2$
SiH_3OSiH_3 $-SiH_2OSiO-$ $(HSiO(OH))_2$

CH_3OSiO_2 CH_3OSiO CH_3OSi CH_3OSiOH
$CH_3OSi(OH)_3$ $CH_2OSi(OH)_3$ $CH_3OSi(OH)_2O$
$Si(OCH_3)_2(OH)_2$ $SiOH(OCH_3)_2$ $Si(OH)_2OCH_3$
$Si(OCH_3)_3OH$ $Si(OCH_3)_3O$ $Si(OCH_3)_3$ $Si(OCH_3)_2$
$Si(OCH_3)_4$ $(CH_3)_3SiOH$ $(CH_3)_3SiO$
$-Si(OH)_2OCH_2-$ $O=SiOHOCH_3$ $O=Si(OCH_3)_2$
$Si(OC_2H_5)_4$ $Si(OC_2H_5)_3OH$ $Si(OC_2H_5)_2(OH)_2$
$C_2H_5OSi(OH)_3$
$Si(OC_2H_5)_3H$ $C_2H_5OSiH_3$ $O=Si(OC_2H_5)_2$

N N_2 N_3 NH NH_2 NH_3 NNH N_2H_2 N_2H_3 N_2H_4 HN_3

CN CN_2 CNN C_2N C_2N_2 C_4N_2 HCN HCNH H_2CN

H_2CNH HNC HNCN HNCNH H_2CNCH_2 ClCN

NO NO_2 NO_3 N_2O N_2O_3 N_2O_4 N_3O_5
HNO HNO_2 HNO_3 HNOH HONO $HONO_2$ H_2NO
H_2NOH $HN(OH)_2$ H_2NNO HNNHO HNNO
HNNONO ONHNHO ONHNOH

CNO HCNO HNCO HOCN
CH_3NO CH_3NO_2 CH_3ONO CH_3ONO_2
H_2CNCH_2O H_2CNCHO H_2CNO H_2CNO_2
H_2CONO H_3CONHO
H_2CNNHO H_2CNNO H_2CNNO_2 OCHNNHO

SiN SiNH $SiNH_2$ Si_2N HSiN HSiNH $HSiNH_2$
H_2SiN H_2SiNH H_2SiNH_2 H_2SiNH_3 H_3SiN H_3SiNH
SiH_3NH_2 $H_2Si(NH_2)_2$ $HSi(NH_2)_3$ $Si(NH_2)_4$
$HSi(NH_2)_2$ $Si(NH_2)_3$ SiH_3NHSiH_3 SiH_3NSiH_3

B BC BO BO_2 B_2 B_2O B_2O_2 B_2O_3
BH HBO HOBO BH_2 HBOH H_2BO HOBOH BH_3
BH_2OH $HB(OH)_2$ $B(OH)_3$ $B_3O_3H_3$ $H_3B_3O_6$ $B_2H_4O_4$
BCl BCl_2 BCl_3 B_2Cl_4 HBCl $BHCl_2$ BH_2Cl
BOCl $B_3O_3Cl_3$

BN BNH BNH_2 HBN HBNH $HBNH_2$
H_2BN H_2BNH H_2BNH_2 H_3BNH_3
$B(NH_2)_2$ $B(NH_2)_3$ $HB(NH_2)_2$ $B_3H_6N_3$
ClBN ClBNH $ClBNH_2$ Cl_2BN Cl_2BNH Cl_3BNH_3
$HClBNH_2$ $BNCl_2$ BCl_2NH_2 $BCl(NH_2)_2$
$NH_2BCl_2NH_3$

H_3SiBH_2 H_2SiBH_2 $HSiBH_2$ H_3SiBH H_3SiB H_2SiBH

H_2SiB HSiBH $SiBH_2$ SiBH SiB
$HSi(H_2)BH_2$ $Si(H_2)BH_2$ $HSi(H)BH_2$ $Si(H_2)BH$
$Si(H_2)B$ $Si(H)BH_2$

$H_3SiSiH_2BH_2$ $HB(SiH_3)_2$ $H_2SiBHSiH_3$ $H_3SiBSiH_3$
$Si(H_2)BSiH_3$ $H_2SiBHSiH_2$ $Si(H)BHSiH_3$
$H_3SiSiBH_2$ $HSiBHSiH_3$ $H_3SiSiHBH$ $H_2SiBSiH_3$
$Si(H_2)BSiH_2$ $HSiBHSiH_2$ $Si(H_2)BHSiH$
HSi(H)BHSiH SiBHSiH$_2$ $Si(H_2)BSiH$ Si(H)BHSiH
$HSiBSiH_2$ HSiBHSiH $H_2Si(BH_2)_2$ $HSi(BH_2)_2$
$HBSiH_2BH_2$ -$H_2SiBHBH$- $Si(BH_2)_2$

$H_3SiBHCl$ $H_2ClSiBH_2$ $ClSi(H_2)BH_2$ $HSi(H_2)BHCl$
$HClSiBH_2$ $H_2SiBHCl$ $ClSi(H)BH_2$ $Si(H_2)BHCl$
H_3SiBCl $HSi(H)BHCl$ $H_2ClSiBH$ $Si(H_2)BCl$
$ClSiBH_2$ HSiBHCl H_2SiBCl HClSiBH $SiBCl_2$
ClSiBCl SiBHCl HSiBCl ClSiBH HClSiB
SiBCl ClSiB

P P_2 P_4 PH PH_2 PH_3 PCl PCl_3 PCl_5
PO PO_2 P_4O_6 P_4O_{10} $POCl_3$
CP CHP PN

Liquid:

Si(L) SiO_2(L)
B(L) B_2O_3(L) B_4C(L)
P(L)
N_2H_4(L)

Solid:

Si(S) SiO_2(S)
B(S) B_4C(S) B_2O_3(S) $B_3O_3H_3$(cr)
C(S) SiC(B)
P(cr) P_4O_{10}(S)
Si_3N_4(A)
BN(cr)

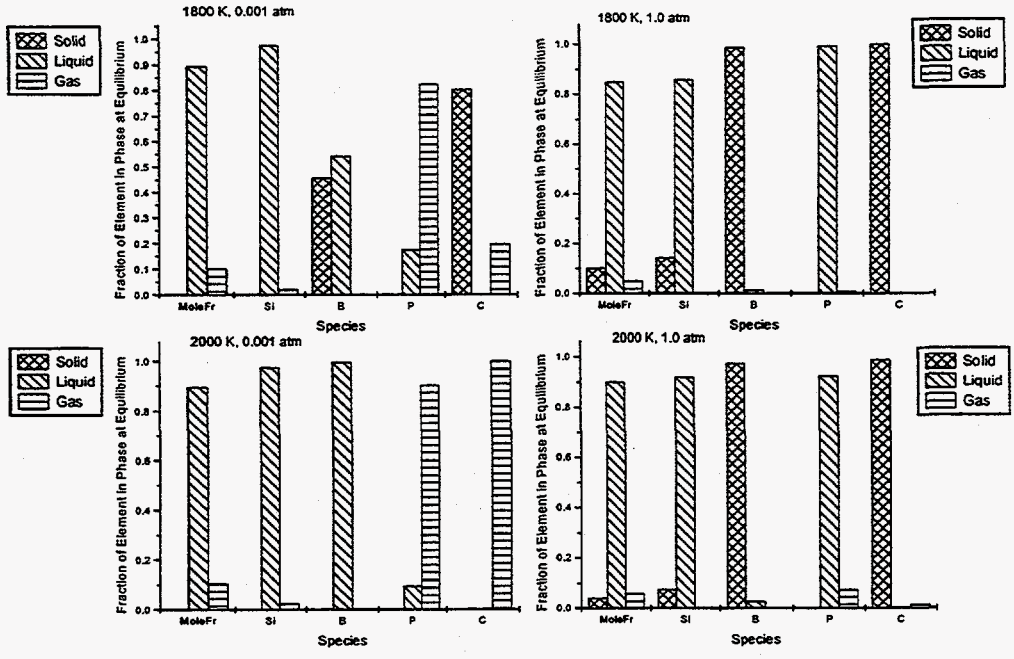

Figure 1. Results of thermochemical equilibrium calculations for mixture 4 by element.

Emission and Capture Trapping Lifetimes of the n-Type Silicon Wafers Evaluated Using Frequency Resolved Microwave Photoconductance Method

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The recombination properties of silicon e.i. surface recombination velocity, recombination and trapping lifetimes, exhibit high sensitivity to the presence of grown or wafer processing induced defects and impurities at levels which cannot be assessed by other non-electrical evaluation methods. The microwave photoconductance decay method (μ-PCD) is a common technique for lifetime evaluation. The extension of the μ-PCD technique based on frequency-resolved photoconductance (FR-PC) measurement is presented here. The microwave reflection coefficient is analyzed in the complex plain using Nyquist plots. The recombination process is described using a two level recombination/trapping model described in [1] and carrier kinetics characterized by surface recombination velocity v_s, bulk lifetime τ, emission τ_e, and capture τ_c lifetimes:

$$\frac{1}{\tau_c} = c_t N_t (1 - f_t), \quad \frac{1}{\tau_e} = c_t (n_{dc} + n_2) \tag{1}$$

where f_t is a trap filling factor and N_t, c_t are concentration and capture rate, respectively, n_2 is the characteristic electron concentration [2] and n_{dc} is DC excess minority carrier concentration. The microwave reflection coefficient in frequency domain can be expressed as:

$$R_{ac}(\omega) = q\left(\frac{\partial R}{\partial \sigma}\right)_o \mu_n \left(1 + \frac{\mu_p}{\mu_n}\frac{\tau^*}{\tau}\right) N(\omega) \tag{2}$$

where $N(\omega)$ represents the total excess carrier concentration generated by a modulated IR source of ω frequency The effective lifetime τ^* in (2) is given by [1]:

$$\tau^* = \tau\left(1 + \frac{\tau_e}{\tau_c}\frac{1}{1 + i\omega\tau_e}\right) \tag{3}$$

The four parameters, v_s, τ, τ_e, and τ_c, are determined from the phase shift function using nonlinear simplex method [1,3]. The frequency measurement range from 10 Hz to 100 kHz. A set of n-type silicon wafers doped with phosphor at concentration of 10^{15} cm^{-3} were cut from the same CZ ingot and measured using the FR-PC and SPV techniques. One group of these wafers was annealed in order to annihilate the thermal donors (TD) present in the material, while the second one was not annealed. It is expected that without TD annihilation the trapping center number is large. Fig.1 shows the measured data represented by Nyquist plots for the as-grown and TD annealed wafers measured at room temperature. The left part of the plot, for the as-grown wafer, is related to carrier

recombination and the right to trapping processes. Notice that the trapping related part disappears for the TD annealed wafer (open circles in Fig.1). It is seen that the detection limit of the used apparatus (Lifetech 88) is reached at the tail of the Nyquist plot, corresponding to the trapping region. As a result the signal is scattered. Fig. 2a and b show the qudrature (Y) and the in phase spectra (X) for both wafers. In both cases, the Lorentzian minima(shown by arrows in Fig. 2) are seen at a frequency of about 3 kHz for

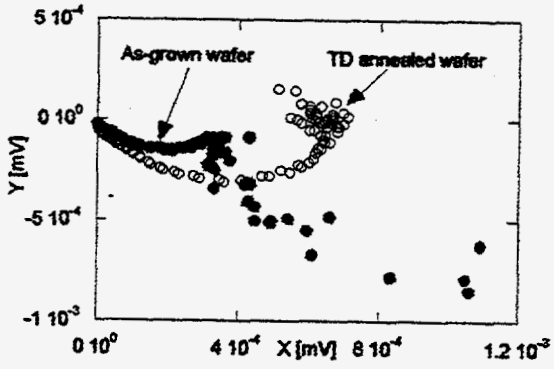

Fig. 1. Measured Nyquist plots for the as-grown and TD annealed n-type CZ wafers.

the Y spectra. The value of the Lorentzian frequency depends on the recombination lifetime [1]. For the as-grown wafer the low frequency quadrature signal decreases because of capturing of the free carriers at the traps. Four parameters, the recombination lifetimes τ, τ_e, τ_c, and surface recombination velocity v_s, have been evaluated by fitting the measured phase shift function $\Phi(\omega) = \tan^{-1}(Y/X)$ to the calculated phase function. For as-grown wafers a four parameter fitting vector $[v_s, \tau, \tau_e, \tau_c]$ has been used, because of the presence of the traps, while for the TD anneal wafer, the fitting vector is reduced to a two-dimensional $[v_s, \tau]$. Fig. 3a shows the experimental and the theoretical Nyquist plots for the following parameters: $v_s = 1289.7$ cm/s, $\tau = 359.7$ μs, $\tau_c = 239$ μs, and $\tau_e = 11$ ms. Both the Nyguist plot and the qudrature spectrum well match the experimental data. In the case of TD annealed wafers, we could not determine the "best" two parameter fitting

a) b)

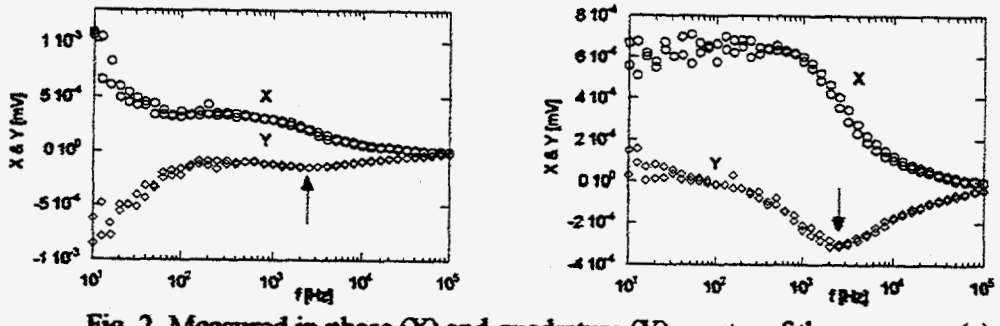

Fig. 2. Measured in phase (X) and quadrature (Y) spectra of the as-grown (a) and TD annealed (b) wafers (Lorentzian frequency is labeled by arrow).

vector [v_s, τ]. For example, Fig. 3b shows the experimental and the simulated data for v_s = 1370 cm/s and τ = 276 μs. The lack of the optimal solution of the nonlinear fitting procedure indicates that the recombination process of the TD annealed wafers can not be described by simple bulk and surface carrier recombination kinetics. The carrier transition should be characterized by the multilevel recombination centers.

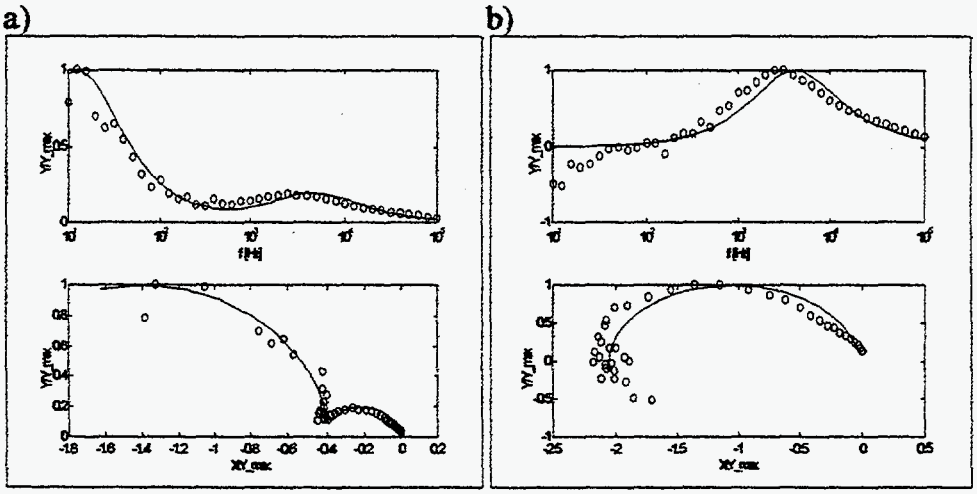

Fig. 3. Normalized experimental-theoretical Nyquist plots of the as-grown (a) and TD annealed (b) wafers.

The relation between the microwave reflection coefficient and the lifetime was determined in the frequency domain. Measured spectra, along with a nonlinear simplex fitting procedure, have been used to determine the recombination/trapping lifetime properties for CZ silicon. The traps associated with thermal donors were studied in as-grown and TD annealed n-type wafers. The trapping centers were found for as-grown wafers. They disappear after the annealing cycle, however carrier kinetics can not be fully described by simple surface/bulk recombination processes.

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Applications of PVSCAN5000 for Analysis of Wafer Defects and Solar Cell Performance

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Introduction

It is well established that crystal defects in the substrate of a silicon solar cell strongly affect the cell's performance. Dislocations are the dominant defect species in low-cost (single or multicrystalline) commercial photovoltaic silicon substrates. Recent studies have shown that not only the average defect density but also the distribution of defects play an important role in degrading the performance of solar cells [1]. Because crystal defects can interact with impurities, the influence of defects on the solar cell performance is strongly affected by the impurities present in the crystal during its growth. For example, it has been determined that defect clusters favor precipitation of metallic impurities that can cause "shunting" of the device and degrade its voltage-related parameters [2]. Thus, it is important to know the nature of the defects, their distribution, and how they influence the solar cell performance. We have developed a system, PVSCN5000, for defect characterization of large-area silicon wafers and for analyzing solar cells.

The PVSCAN5000 photovoltaics analyzer is an easy-to-use instrument that can be applied for both characterization of defects in the as-grown material and for mapping distribution of several key performance parameters of solar cells. PVSCAN5000 measures the dislocation density and the grain boundary distribution of the as-grown material. Because the distribution of defects is indicative of the nature of thermal stresses produced in the crystal growth process, these parameters provide information on the quality of the material and an insight for improving the material manufacturing process. The cell parameters that PVSCAN5000 can measure include reflectance and light beam induced current (LBIC) at two wavelengths of light excitation. These data can provide information on the uniformity of the cell, the quality of the fabrication processes, and the internal response of the cell. This instrument also provides a qualitative evaluation of the near-surface and the bulk recombination properties of minority carriers. This feature is made possible by measuring the internal photoresponse of the device at long- and short-wavelength excitation, and can be related to the junction and the bulk recombination characteristics, respectively. The long wavelength response data are used to output maps of the minority carrier diffusion length – a parameter used for device analysis, process monitoring, and device optimization.

The operating principle of PVSCAN

PVSCAN5000 uses the optical scattering from a defect-etched sample to statistically count the density of defects. It shines a laser beam on the surface of the defect-etched wafer and measures the (integrated) intensity of the reflected (scattered) light. It has been shown that the total integrated reflected light is proportional to the number of scattering centers [3]. Thus, in this system one obtains a signal that is proportional to the local dislocation density. By scanning

of the grain boundaries are much more pronounced in Figure2a, while Figure 2b shows intragrain dislocations, whose densities are represented by different colors (gray scale in this paper).

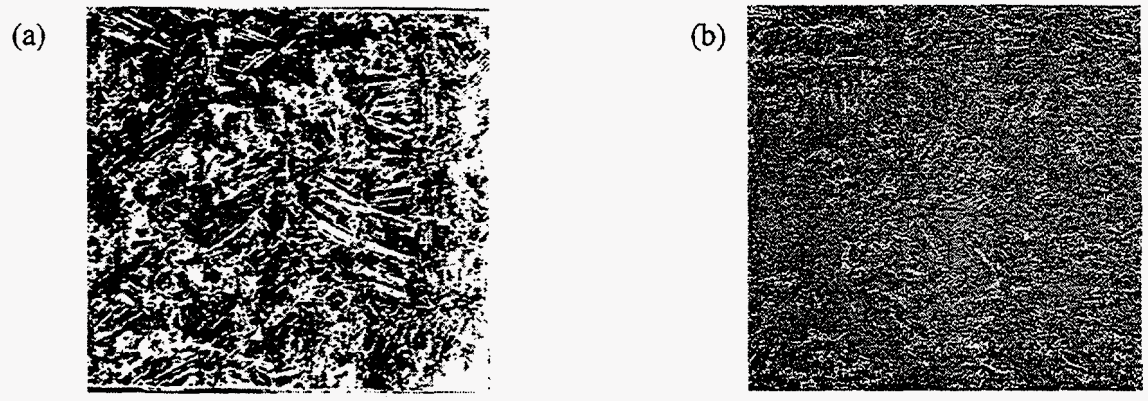

Figure 2. *(a) Grain boundary and (b) dislocation maps of a crystalline silicon wafer collected using PVSCAN*

Since high-defect-density regions have low minority carrier diffusion length (MCDL), defect maps show an excellent correlation with the MCDL maps. Hence, they can also indirectly provide MCDL information. Figure 3 illustrates these results. Figure 3a shows a MCDL map of the 5-cm x 5-cm poly-silicon sample, measured by the SPV technique, using a beam size of 3 mm. The defect map of the region, corresponding to the MCDL map in Figure 3a, is shown in Figure 3b. This figure was made by PVSCAN5000 with a beam size of about 300μm; here the darker regions have lower defect density. An excellent correlation is observed between the two images, but the defects map has much higher resolution.

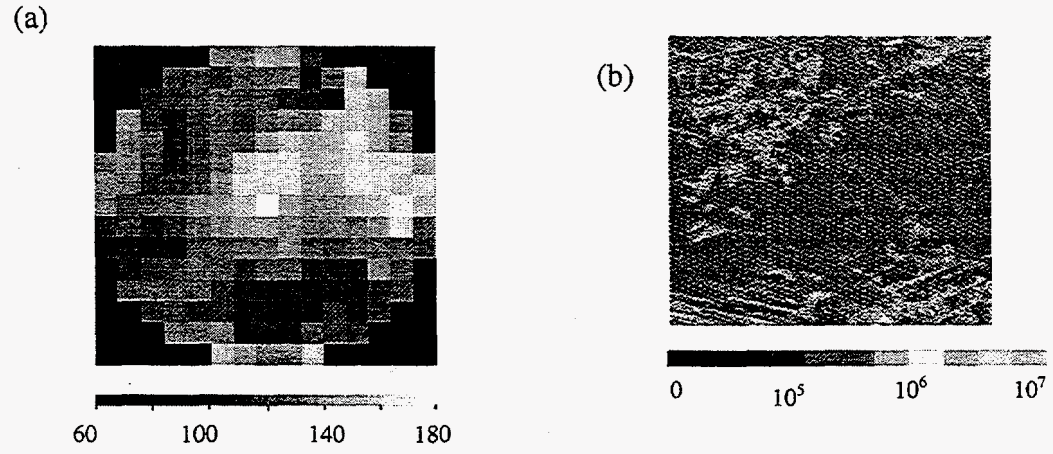

Figure 3: *(a) MCDL in μm, and (b) defect densit, in defects/cm^2, maps of a 5-cm x 5-cm silicon sample showing correlation between them {the circular shape of the map in (a) is because the instrument is designed for the measurement of circular wafers}.*

Although the material analysis data from PVSCAN can be used to deduce the properties of the devices, the more direct way to analyze a solar cell is to measure the photo response of the cell

itself. PVSCAN5000 can be used to map the LBIC of the device. Furthermore, by mapping reflectance and adjusting the external (direct) LBIC readings to consider the amount of light that never actually penetrates a solar cell, the PVSCAN can map the internal LBIC response that more accurately represents the capabilities of the cell measured by PVSCAN. Figure 4 shows the external LBIC and internal LBIC maps of a cell. Here the lighter color corresponds to higher photo response. Note that the response of internal LBIC map is generally higher and more uniform than that of external LBIC map. Weaker areas in the upper half of the figure are shown to be the result of (higher) reflectance (probably caused by grain orientation). Only one area in the upper middle part, caused by a dislocation cluster, remains substantially weak in the internal response map.

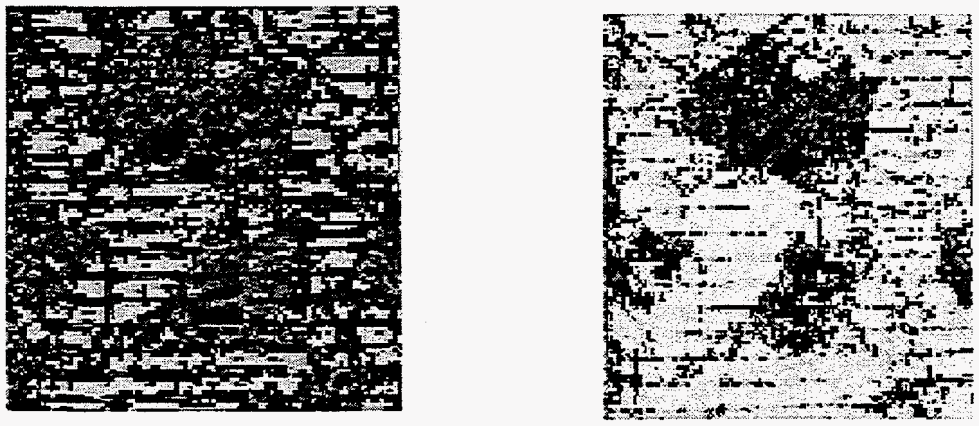

Figure 4. *"External" (left) and "internal" (right) LBIC photoresponse map of a solar cell made by PVSCAN.*

By analyzing the photo response of solar cells fabricated by different process sequences, one can also evaluate the effectiveness of these processes in improving the cell performance. Figure 5 shows the LBIC map of two cells made on two adjacent wafers in a silicon boule. The cell in figure 5b was gettered. Also shown in figure 5c is the defect map of the wafer. Note that while the gettered solar cell (figure 5b) performs significantly better than the un-gettered one (figure 5a), some poor-performing areas appear in both cells at the same positions. These regions are identified as defect clusters from a defect map shown in Figure 5c. This observation reveals a very important result in that gettering doesn't improve the properties of defect-cluster region. The frequently high concentrations of impurities in defect clusters and the ineffectiveness of gettering in removing them, underscores the need to ameliorate defects as a first step in solar cell processing.

Conclusions

The PVSCAN5000 photovoltaic analyzer maps several key performance parameters for completed solar cells and for the silicon wafers from which they are made. It can distinguish and map different kind of defects of the materials, map the PV response of the cells. It is a powerful analytic instrument of PV industry.

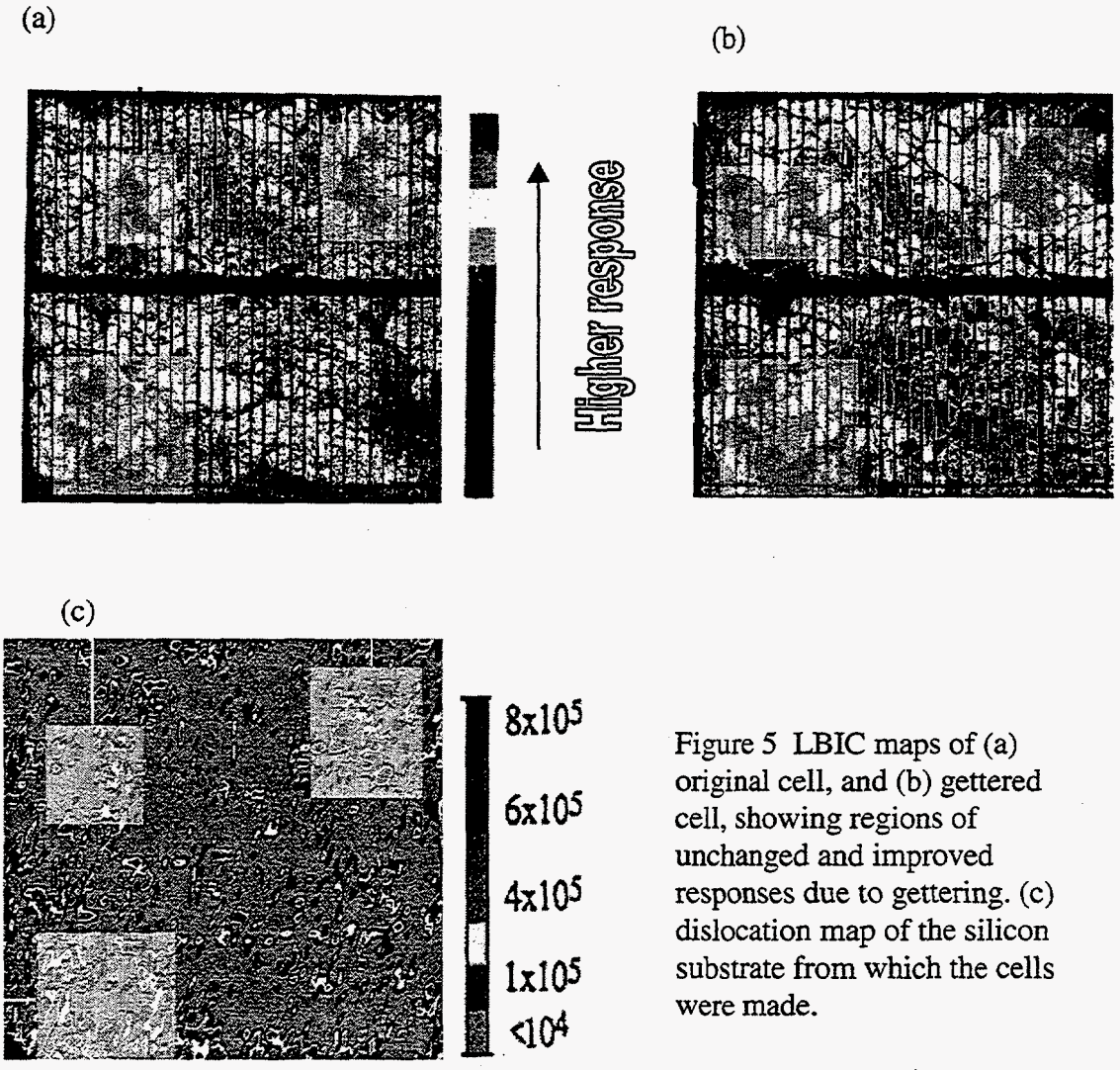

Figure 5 LBIC maps of (a) original cell, and (b) gettered cell, showing regions of unchanged and improved responses due to gettering. (c) dislocation map of the silicon substrate from which the cells were made.

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CHARACTERIZATION OF PHOSPHORUS GETTERING PROCESS FOR MULTICRYSTALLINE SILICON WAFERS BY SURFACE PHOTOVOLTAGE

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ABSTRACT

Phosphorus gettering of multicrystalline Si wafers fabricated by a drip-controlled method has been investigated by analyzing measured diffusion lengths and lifetimes of minority-carriers. The diffusion length and lifetime of as-received cast wafers were around 100μm and 30μs except for peripheral regions of the wafers. After phosphorus (P) -diffusion at 800℃, Fe concentration at the peripheral regions decreased drastically and lifetime values increased to the same values in high-quality bulk regions. Diffusion length did not vary with Fe concentrations in the case of those lower than $5\times10^{11}cm^{-3}$, because of the existence of other recombination centers of about $10^{12}cm^{-3}$. The other recombination centers seem to be crystal defects since the concentration of the other recombination centers does not change irrespective of annealing conditions.

INTRODUCTION

Multicrystalline Si solar cells have been fabricated at low cost using cast wafers produced by various techniques. A drip-controlled method (DCM), one of the casting method, was reported by Daido Hoxan to obtain lower cost Si ingot [1]. In the DCM, the injection of molten Si and the crystal growth were carried out simultaneously and the heat of molten Si was utilized actively as a heat source to control the crystal growth. Recent DCM advanced to produce a 170kg ingot with 43cm square, 40cm in height. Inhomogeneities of the DCM were investigated by comparison of lifetime maps with diffusion length maps [2].

In this study, diffusion length and lifetime maps were investigated using 10 cm × 10 cm square wafers sliced from a 22 cm × 22 cm square ingot. Fe concentration was calculated by analyzing the diffusion lengths measured using surface photovoltage (SPV) method. SPV mapping with a density of up to 6000 points/wafer is carried out with an Fe detection limit below 10^{10} atoms/cm^3 [3]. Detailed studies of quality improvement by P-gettering are performed as a function of P-diffusion temperature for DCM multicrystalline cast Si wafers.

EXPERIMENTAL

Sample preparation

Multicrystalline Si wafers were fabricated by a drip-controlled method (DCM). The DCM equipment consists of mold pre-heating, crystal growth and cooling zones separately on both sides of a molten Si injecting zone. Molten Si was fed drop-wise from the upper part to the crystallization zone to facilitate continuous casting. The cooling speed of the molten Si was controlled at less than 1mm/min. 10 cm × 10 cm square p-type multicrystalline Si wafers sliced from the DCM cast ingot were used for this study. Phosphorus was diffused into both sides of the wafers using $POCl_3$ at 800, 900 and 1000 ℃ for 30 min.

Characterization

The quality of the DCM wafers was characterized by combining lifetime, τ, and diffusion length, L, measurements. Minority carrier lifetime maps were measured using a microwave photoconductivity decay (m-PCD) method using a pulse laser of 904nm. A chemical passivation (CP) technique using I_2 in ethanol was applied for reducing surface recombination velocity at wafer surfaces to obtain bulk lifetimes [4]. The CP was very effective to eliminate surface contribution of carrier recombination and to obtain inherent bulk lifetimes for the multicrystalline wafers.

Minority carrier diffusion length maps for the same wafers were measured by the SPV method[3]. In SPV measurement, surface photovoltage was measured at different wavelengths without contact. Fe concentrations were calculated from the diffusion length changes before and after Fe-Boron dissociation by thermal activation at 200℃ for

3 min [5]. Principles ofthe SPV monitoring ofiron are that, when all irons are paired and L is its maximum, L_0; and when all pairs are dissociated and L is at its minimum L_1, Fe concentration, N_{Fe}, was calculated from the following equation.

$$N_{Fe}=(D/C_{Fe})(L_1^{-2}-L_0^{-2}).$$

Other recombination centers, N_R, were calculated from the following equation.

$$N_R=(D/C_R)(P-1)^{-1}(PL_0^{-2}-L_1^{-2}).$$

where D is the electron diffusion constant, C_{Fe} and C_R are the electron capture rates of the iron and other recombination centers, respectively. P is typically between 10 and 20, depending on the Fermi energy [3]. Beforethe measurement, the P-diffused n-layers were removed from both sides of the wafersby immersing the samples in an $HF:HNO_3$ (1:20) solution.

RESULTS AND DISCUSSION

Fe concentrations in DCM cast wafers

Using the SPV, a diffusion length and Fe concentration foran as-received waferwere obtained to be 110 μm and 2.2×10^{11} cm^{-3}. After P-diffusion at temperatures of 800 and 900℃, as shown in Fig. 1, the Fe concentrations decreased to about 1/4 and 1/2 of the as-received value in a whole region, respectively. This result shows that Fe concentration decreased due to the P-gettering effect. However, after 1000℃ P-diffusion, L decreased to 90 μm and Fe concentration increased to about 2.5 times higher than the as-received value.

Inhomogeneous distribution ofFe concentrations was observed in central and peripheral regions. The peripheral region was defined as a region, 1 cm apart from the mold. AfterP-diffusion at temperatures of800 and 900℃, as shown in Fig. 2, the Fe concentrations at peripheral regions decreased about 1/12 and 1/7 of the as-received value because of P-gettering effect. On the contrary, after1000℃ P-diffusion, Fe concentration increased to about 1.5 times higher than the as-received value, probably because of dissociation of gettered impurities at high temperatures.

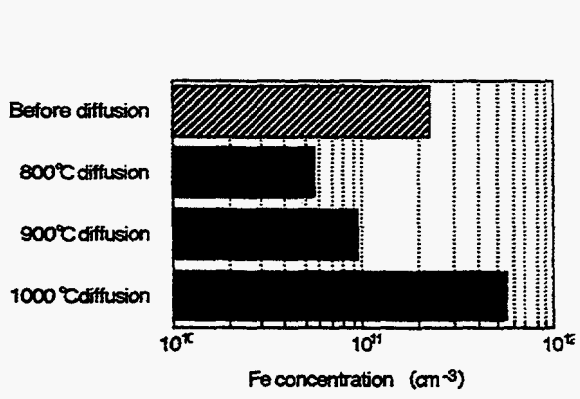

Fig. 1 Variation of averaged Fe concentrations in a whole region of DCM cast wafers with P-diffusion temperatures at 800, 900 and 1000℃.

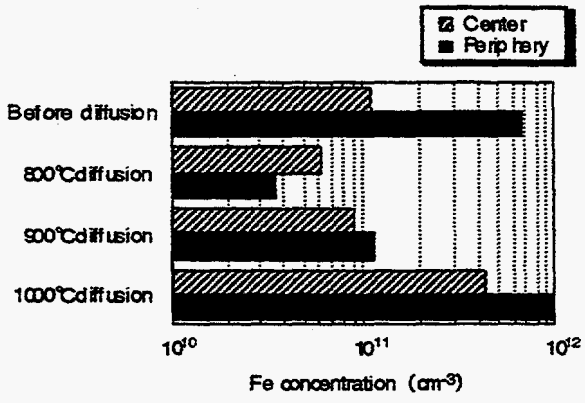

Fig. 2 Variation ofFe concentrations at central and peripheral regions ofP-diffused DCM cast wafers

Distribution of Fe concentrations and lifetimes

Fe concentration at the peripheral region was distributed about 7 times higher than the central region in the as-received wafer. The inhomogeneous featurewas clearly observed in the peripheral ofthe as-received wafer, as shown in Fig. 3 (a). This result shows that as-received wafer was contaminated by iron from the mold. After P-diffusion at 800℃, as shown in Fig. 3(b), the Fe concentrations at the peripheral and central regions decreased greatly to be the same values in the high-quality bulk regions. However, after 1000℃ P-diffusion, as shown in Fig. 3(c), Fe concentrations tend to increase, because of dissociation of gettered impurities at high temperature.

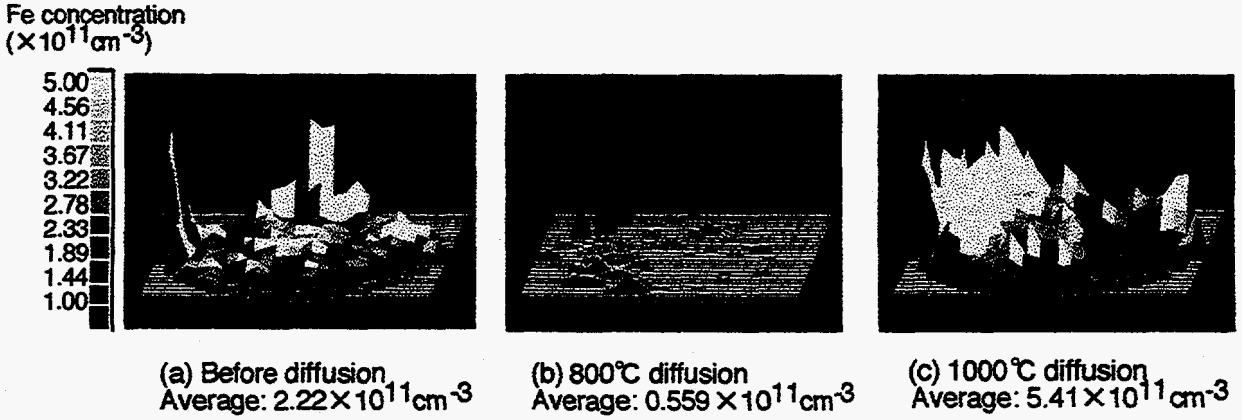

Fig. 3 Fe concentration maps of cast Si wafers before and after P-diffused at temperatures of 800 and 1000℃.

Using μ-PCD, an averaged lifetime for an as-received wafer was obtained 26 μs. At the peripheral region in the as-received wafer, the lifetime was very low about one fifth of the central region. This tendency corresponds to the distribution of Fe concentration. After P-diffusion at temperature of 800℃. The averaged lifetime increased about 1.6 times higher than the as-received value. Especially, at the peripheral region, lifetimes improved to 40 μs, 7 times higher than the as-received value of 6 μs. The inhomogeneous feature for an as-received wafer was changed to homogeneous after 800℃ P-diffusion. However, after 1000℃ P-diffusion, lifetime decreased to about half of the as-received value. Especially, at the periphery of the wafer, lifetime degraded, because of high temperature annealing. This tendency corresponds to distribution of Fe concentration. These results show that there is a relationship between Fe concentration and lifetime.

Effect of Fe concentrations and other recombination centers on diffusion length

Diffusion length was compared with concentrations of Fe impurity and other recombination centers for as-received and P-diffused wafers. As for the as-received wafer, as shown in Fig. 4(a), diffusion length depended on Fe concentration in the range of 5×10^{11} to 10^{13} cm^{-3}. The points of low diffusion lengths were plotted as 10^{12} to 10^{13} cm^{-3} of Fe concentration. After P-diffusion at temperature of 800℃, as shown in Fig. 4(b), Fe concentration decreased from 10^{12} to 10^{11} cm^{-3}. However, after 1000℃ P-diffusion, as shown in Fig. 4(c), Fe concentration was spread in 10^{11} to 3×10^{12} cm^{-3} as compared with the 800℃ P-diffusion.

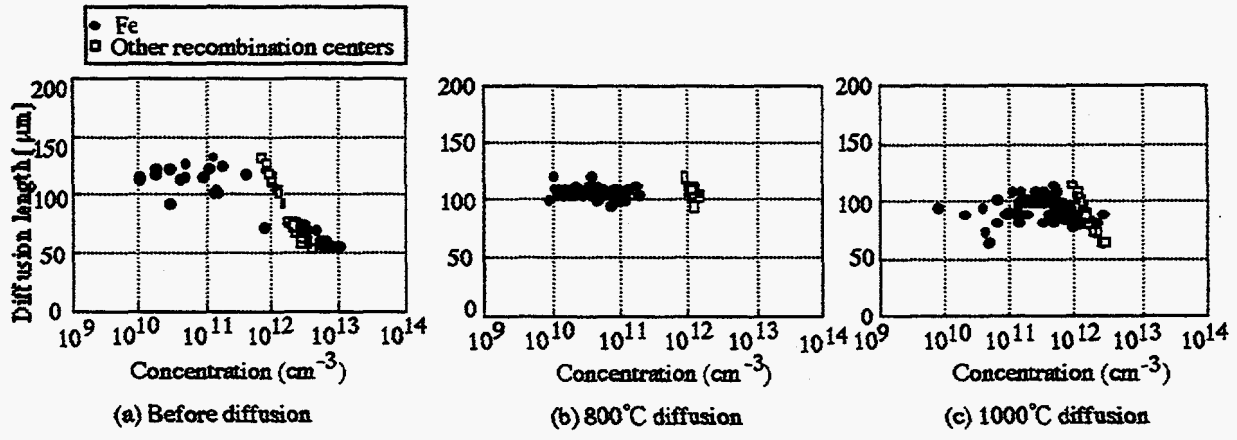

Fig. 4 The relations between minority-carrier diffusion length and concentrations of Fe and other recombination centers for as-received and annealed cast crystals

On the other hand, concentrations of other recombination centers of these wafers were about 10^{12} cm^{-3} and did not change with diffusion temperatures. This result shows that other recombination centers did not affect diffusion lengths greatly. The other recombination centers seem to be crystal defects since the concentration of the other recombination

centers did not change irrespective of annealing conditions.

An averaged concentration of other recombination centers for the as-received wafer was about 1.2×10^{12} cm^{-3}, as shown in a concentration map of Fig. 5(a). Concentrations of other recombination centers at 800 and 1000℃ P-diffusion were 1.3×10^{12} cm^{-3} and 1.7×10^{12} cm^{-3}. These values hardly changed with the diffusion temperature, as shown in Fig. 5(b), (c). At 1000℃ P-diffusion, another increase in Fe concentration appeared especially at the peripheral region corresponding to the degradation of minority-carrier diffusion lengths. This is probably due to the contamination of lifetime killer impurities from an ambient and/or the generation of crystal defects.

(a) As-received wafer Average: 1.2 x 10^{12} cm^{-3}

(b) P-diffused at 800 C average: 1.3 x 10^{12} cm^{-3}

(c) P-diffused at 1000 C average: 1.7 x 10^{12} cm^{-3}

Fig. 5 Concentration maps of other recombination centers for as-received and cast Si wafers P-diffused at temperatures of 800 and 1000℃

CONCLUSION

During P-diffusion at 800℃, minority carrier lifetimes of cast wafers improved drastically due to P-gettering of Fe impurities. The lifetime after 800℃ P-diffusion increased about 1.6 times higher than the as-received value. Especially, P-gettering effect at the peripheral region was very effective. This tendency corresponded to the distribution of Fe concentration. So, one of the lifetime killers for DCM cast Si wafer was probably iron. Concentrations of other recombination centers were about 10^{12} cm^{-3} and did not change with P-diffusion. Concentrations of other recombination centers did not affect diffusion length so much as compared with Fe concentrations. These results show that other recombination centers seem to be crystal defects.

ACKNOWLEDGMENTS

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Light Induced Defect Reactions in Boron-Doped Silicon: Cu versus Fe

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Impact of room temperature illumination on the minority carrier diffusion length and recombination centers is observed in Cu doped p-type Cz-Si using surface photovoltage and deep level transient spectroscopy. The light induced effects involving Cu are clearly distinguished from the light-triggered dissociation of FeB pairs and revealed as (i) irreversible degradation of the diffusion length down to ~10 microns, (ii) reduction of the Cu-related trap concentration, coupled with generation of new hole and electron trapping centers. In samples cross contaminated with Fe and Cu, we observed a retardation of the FeB => Fe+B light-triggered dissociation kinetics. This new effect is attributed to a competition of Cu-centers in recombination enhanced FeB dissociation.

Introduction. Control and reduction of heavy metal contamination is a primary concern in Cz-Si for microelectronics and PV crystalline Si. Solar cell processing, such as P-diffusion, hydrogenation, and Al-firing substantially reduce concentration of Fe and Cr increasing minority carrier diffusion length from 20-80μm in bare wafers to 200-300μm in final cells. In order to optimize cell processing, it is valuable to assess a level of contamination and identify impurities.

Optical dissociation of Fe-B pairs is employed for quantitative contamination control of p-type Si by using surface-photovoltage (SPV) technique [1]. The method is based on recombination-enhanced defect reaction FeB => Fe + B resulted in a decreasing of minority carrier diffusion length [2]. Two "fingerprints" for FeB pairs in the SPV method were suggested [3]. (i) The ratio of diffusion lengths before (L_0) and after pair dissociation (L_1) has to be close to 3 when FeB is a dominant recombination center, and (ii) Fe-B re-association kinetics is specified by the activation energy of 0.68eV. A simple equation was justified to extract the concentration of FeB pairs using only values of the diffusion length before and after pair dissociation:

$$[FeB]\ (cm^{-3}) = 1.05e16 \times (L_1^{-2} - L_0^{-2}) \qquad (1)$$

Validity of Eq. (1) critically depends on two assumptions: (a) no other recombination centers are affected by light, and (b) light intensity and exposure time are sufficient to dissociate all Fe-B pairs. If either (a) or/and (b) are violated then identification of FeB pairs and accuracy to measure their concentration appeared to be questionable. It has been recently reported that light activation degrades the L value in Cu-diffused boron-doped Cz-Si [4]. In this work we examined Si wafers contaminated with either Fe or Cu, and cross-contaminated with both impurities. We have observed not only a strong enhancement of the recombination activity of Cu-centers after optical activation, but also a noticeable retardation of the Fe-B pair dissociation kinetics due to light creation of Cu-related defects.

Experimental. Cz-Si wafers doped with boron at the concentration of $5x10^{14}cm^{-3}$ were intentionally contaminated with either Fe or Cu by ion implantation to a dose of 10^{12}, 10^{13} and 10^{14} cm^{-2}. Drive-in annealing was performed either in conventional furnace at 1000°C followed by rapid quench into liquid nitrogen, or by 1000°C RTA in nitrogen. The FeB concentration in as-received and Cu contaminated samples was below 10^{10} cm^{-3} as revealed by DLTS. Some of the Cu-samples were cross-contaminated with ~10^{11} Fe/cm^3.

SPV minority carrier diffusion length was used to quantify the light-induced defect reactions. Light activation was performed using 1500W quartz halogen lamp with the power density of $150mW/cm^2$. To avoid a sample heating, illumination cycles consisted of 15 second pulses separated by 15 second light-off intervals, thereby establishing maximum sample temperature of 30°C. To investigate iron- and copper-related electronic defects within the entire band gap of p-type Si, both the conventional and optical DLTS were applied to Al Schottky diodes.

Results and discussion.

(A). Diffusion length degradation due to Fe or Cu contamination. Table 1 summarizes the impact of Fe and Cu on the minority carrier diffusion length in B-doped Cz-Si as a function of impurity concentration and drive-in annealing procedure. For both impurities the SPV diffusion length is decreasing with the impurity concentration. It is noticed that at the low contamination level the impact of iron on L degradation is stronger than that of Cu, whereas at the 10^{14} Fe/cm^2 the diffusion length is saturated due to the Fe solid solubility limit at 1000°C. In contrast, the impact of Cu at this contamination level is much stronger. It is also seen that the annealing procedure does not affect the recombination activity of Fe, while the rapid quench creates more recombination centers in Cu-samples.

Table 1. SPV diffusion length degradation in Fe and Cu contaminated Si.

		L (μm)			
		Control	10^{12} cm^{-2}	10^{13} cm^{-2}	10^{14} cm^{-2}
Cu	RTA	600-700	400-600	200-350	20-30
	1000/Quench	600-700	200-350	50-180	15-20
Fe	RTA	600-700	150-200	70-80	60-90
	1000/Quench	600-700	150-200	60-80	60-80

(B) Optical activation and thermal recovery. A typical optical activation experiment on Fe- and Cu-sample is illustrated in Figure 1. Light exposure applied to Fe-samples reduced the diffusion length by a factor of 3. Subsequent annealing at 80°C for 15 min recovered L close to the initial value. These results indicate a reversible FeB⇔Fe+B reaction and are consistent with the Fe "fingerprints" [3]. In contrast, the Cu contaminated wafer revealed a strong, more than ten-fold L degradation after identical light exposure. It is important to note that annealing up to 120°C does not recover the reduced L in the Cu-sample.

In order to determine recombination centers responsible for such irreversible light induced L degradation in Cu contaminated samples, we performed DLTS measurements. As can be seen from Fig. 2, the DLTS spectrum measured before optical activation was similar to that described in Ref. 5 and consisted of four deep level traps. The dominant trap, Ev+0.095eV, was attributed to Cu-Cu pairs [6]. Though this level is very close to FeB pairs (Ev +0.1eV), it can be

distinguished by DLTS using low-temperature bias annealing [5]. Optical activation for 5 min strongly reduced the concentration of the Ev+0.095 eV trap and introduced new levels in the lower part (Fig. 2, dashed line) and the upper part (not shown) of the band gap. No further changes in the DLTS were observed after subsequent 120°C thermal annealing. Thus, the optical activation irreversible degrades the diffusion length, which is correlated to a decrease in the Ev+0.095 eV traps concentration and generation of new deep level centers.

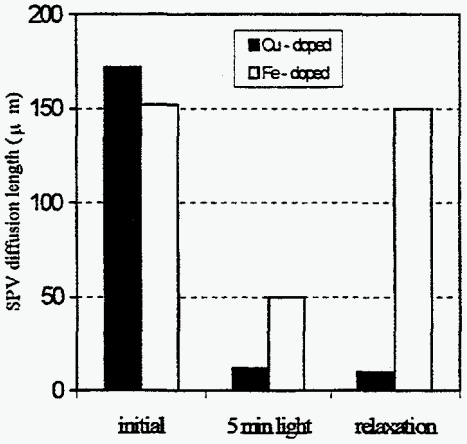

Fig.1 Light activation at room temperature reduces the diffusion length in both Fe- and Cu-doped Cz-Si. Follow-up relaxation (15min at 80C) completely recovers the L in Fe-sample and shows no in Cu-sample.

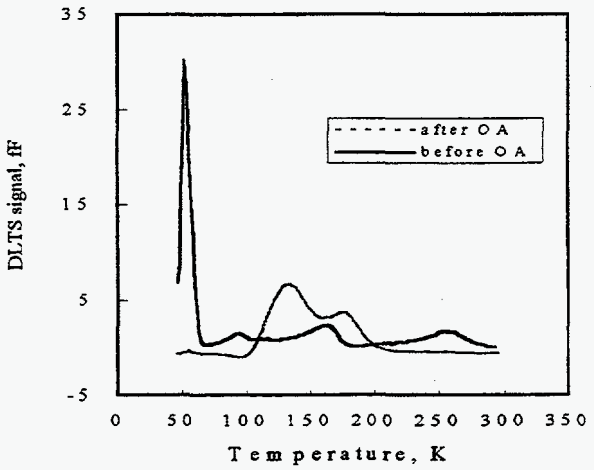

Fig. 2 DLTS spectra of Cu-related traps before and after optical activation. Details of the DLTS measurements can be found in Ref. 5.

C. *Light activation kinetics in Cu+Fe cross contaminated Si.* Figure 3 presents SPV data after several cycles of optical activation and thermal recovery. The following features were observed:

- The initial L value, L_0=312μm, was reduced after first light exposure to L_1=131μm. Long-term 5hour relaxation at 60°C resulted in a partial L recovery to L_2=264μm (saturated value). The difference between L_0 and L_2 indicates the irreversible contribution of the Cu-related defects to the L light-induced degradation.
- Consecutive cycles (2nd, 3rd and 4th) were practically reversible corresponding to the FeB concentration of ~ $5x10^{11}cm^{-3}$.
- Recovery time in every cycle (open dots) was 30 min in a reasonable agreement with calculated FeB pairing rate at 65°C and [B]=$5x10^{14}cm^{-3}$ [3].

Two processes revealed by the SPV study: reversible FeB⇔Fe+B reaction and irreversible light transformation of Cu-defects. The following question can be raised: whether or not the Fe_i released from dissolved FeB pairs contributed to the new Cu-related centers in the cross-contaminated samples? The fact that the total concentration of FeB pairs remains the same after each cycle (Fig.4) indicates that no gettering of Fe_i occurs during optical/thermal cycles. However, we noticed, that the rate of FeB light dissociation was gradually retarded in the cross-contaminated samples as compared to the Fe contaminated sample (Fig. 4). Initial time constant of 1.2 min at the 1st cycle was increased up to 2.8min at the 3rd cycle. We suggest, that the

slowing of FeB=>Fe+B reaction is due to electron capture by Cu-related centers ("Cu") created after optical activation (see insert in Fig.4). This competing process reduces the rate of recombination enhanced reaction of FeB dissociation. In turn, the presence of Fe drastically reduces the effect of light-induced L degradation due to Cu-related centers, compare Fig.1 and Fig. 3.

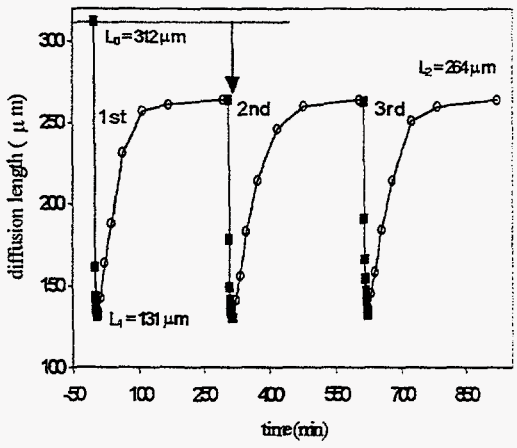

Fig.3 Cyclic light activation (squares) and thermal relaxation at 65°C (circles) in the sample cross contaminated with Cu and Fe. Permanent degradation of L is due to light transformation of Cu-traps with energy of Ev+0.095eV.

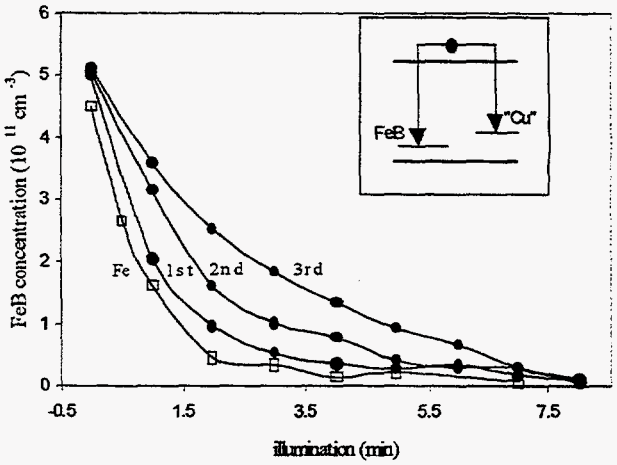

Fig.4 Cyclic light activation and relaxation of FeB pairs promote a gradual retardation of FeB=>Fe+B reaction in cross-contaminated sample with Cu and Fe. Insert: photo-excited electrons are captured at Fe-B pairs and also at the light created "Cu"-centers competing for minority carriers.

Conclusions. (1) Light induced degradation of minority carrier diffusion length is observed in Cu-contaminated Cz-Si. The transformation of Ev=0.095eV centers to new electron and hole trapping states is revealed by DLTS. (2) Kinetics of the FeB pair dissociation can be used as a sensitive method for Cu-monitoring in p-type Si including PV polycrystalline Si. (3) Measurements of FeB concentration using the method of light activation require special precautions in PV crystalline Si. Specifically, (a) total recovery of the initial diffusion length has to be justified, and (b) increased light exposition (intensity and time) is necessary due to high concentration of recombination centers competing for minority carriers.

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IMPROVEMENT OF CARRIER LIFETIME IN SILICON BY GETTERING OF PRECIPITATED IMPURITIES

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ABSTRACT

Numerical modeling of impurity gettering from multicrystalline Si for solar cell production has been carried out using Fe as a model impurity. Calculated nonradiative minority carrier lifetime change in the course of gettering is used as a tool in evaluating the gettering efficiency. Derivation of capture crosssection of impurity precipitates, as compared to single atom recombination centers, is presented. Low efficiency of conventional application of gettering process is explained by the modeling results. Variable temperature gettering process is modeled and predicted to provide high gettering efficiency and short needed gettering times.

Introduction

Gettering of impurities from silicon by an external aluminum or phosphorous layer has been shown to be an effective technique to increase minority carrier lifetimes in single crystal Czochralski Si wafers [1]. This process is especially useful for solar cell production, where obtaining high lifetimes and diffusion lengths of minority carriers throughout the wafer is crucial for the efficiency of the devices. However, this technique has been of a limited effectiveness for low-cost multicrystalline Si which contains higher concentration of impurities and crystal imperfections such as grain boundaries and dislocations. They significantly reduce minority carrier lifetime and, as a result, efficiency of solar cells. In multicrystalline Si, regions with high dislocation density show lower electrical response as well as lower gettering efficiency. Gettering of impurities from this kind of material is difficult because the impurities are largely trapped in precipitates formed at the crystal imperfections. In such cases, the process of gettering can be extremely slow because the precipitates are rich sources of metal atoms which are released to the Si matrix only slowly. The concentration of impurities can be significantly reduced only when the sources of impurities are exhausted, i.e. when all precipitates are dissolved. This process, however, is very slow at the lower temperatures typically used for gettering. Increasing the gettering temperature shortens the precipitate dissolution time. It is known that increasing the gettering temperature to above 950°C for short times can degrade solar cell performance, instead of improving it, especially in the regions with high concentration of extended defects [2]. This can be accounted for by dissolution of precipitates that occurs faster than gettering and thus, resulting in a net increase of impurity concentration and decrease of carrier lifetime. In this paper, we present modeling results which confirm this assessment. Since a shorter process is desirable for practical application, gettering at a high temperature may be needed [3]. However, even if high temperature gettering is carried out for a sufficiently long time, a significant decrease of the impurity concentration may not be achieved, because the impurity segregation coefficient between Si and the gettering material decreases when the temperature is increased. Thus, a compromise between the needed gettering time and residual concentration of impurities is inevitable in the conventional single temperature gettering process. In this paper, a variable temperature gettering process is modeled and compared to the single temperature processes. Calculations of relative changes of minority carrier lifetime which adequately take into account the influence of both dissolved and precipitated impurities are used as a criterion for evaluation of results of gettering.

Modeling of gettering process and carrier lifetime calculations

The process of precipitate dissolution and impurity gettering is modeled for the case of Fe, which is a typical interstitial impurity in Si. The approach described elsewhere [3] is used. It can be easily adopted for modeling of any other interstitial impurity. The modeling is carried out for the case of gettering by an aluminum layer deposited on the back side of a Si wafer. The thickness of the wafer was assumed to be 200 μm, the thickness of Al layer 2 μm, and Fe solubility limit in liquid Al 1 atomic percent. As initial condition, the concentration of dissolved Fe and the combined concentration of dissolved and precipitated Fe were taken equal to the thermal equilibrium concentration of Fe in Si at 700 and 900 °C, respectively, and the concentration of precipitates is 10^{11} cm^{-3}. As a result of modeling, time-dependent profiles of Fe concentration and precipitate sizes throughout the wafer were obtained.

The ultimate goal of impurity gettering from Si for solar cell applications is the improvement of solar cell efficiency by increasing minority carrier lifetime and diffusion length. These values can be measured experimentally for the carriers generated on one side of a wafer and diffused to the other side [1]. It is the lifetime of minority carriers passing through the whole thickness of a wafer that controls the efficiency of the solar cells. This lifetime is determined by carrier recombination rate, integrated over the thickness of the wafer, as

$$\tau = \frac{\delta n}{R}, \qquad (1)$$

where δn is the excess minority carrier concentration and R is the recombination rate. On the other hand,

$$\tau = \frac{1}{\sigma v_{th} C}, \qquad (2)$$

where σ is the recombination center capture cross-section, v_{th} is the thermal velocity of minority carriers, C is concentration of recombination centers. When there are more than one type of recombination centers present in the crystal, the respective recombination rates are additive. The impurities in multicrystalline Si can be in dissolved and precipitated forms. The capture crosssection of a dissolved impurity atom is close to the atomic size and can be written as

$$\sigma_{at} = \pi (\alpha r_{at})^2, \qquad (3)$$

where $\alpha \sim 1$. For a precipitate, the capture crosssection can be expected to be close to its size. However, the reaction of nonradiative electron-hole recombination is generally assumed to have a sufficiently high rate, so that the excessive concentration of carriers is zero or a negligibly small constant value at the surface of the recombination center [4,5]. Then the actual reaction rate is determined by the diffusion of the carriers to the recombination center. Recombination centers are surrounded by diffusion domains, which are free of other recombination centers. Assuming that they are distributed homogeneously, a diffusion domain can be approximated by a sphere of radius

$$r_{max} = \left(\frac{3}{4\pi C}\right)^{1/3}. \qquad (4)$$

At the outer boundary of the diffusion domain, there is no flux of carriers. In steady state, the carrier excessive concentration is described by a stationary diffusion equation. Its solution provides us with the concentration and flux of excess minority carriers at any point of the domain. The total flux of minority carriers through the surface of the recombination center is equal to the total recombination rate in the diffusion domain. A similar consideration can be applied to precipitates. The concentration of excess minority carriers can be assumed to be zero at the surface of the precipitate. Then, comparing recombination rates at the surface of the precipitate recombination center and single atom recombination center, one obtains that capture crosssection of a precipitate is related to that of a single atom as

$$\sigma_{prec} = \sigma_{at} \frac{r_{prec}}{\alpha r_{at}}. \qquad (5)$$

The fact that the capture crosssection increases as the linear size of the recombination center, rather than its second power, accounts for the fact that the recombination process is diffusion limited, rather than reaction limited. This dependence allows us to evaluate the recombination rate due to the presence of both dissolved and precipitated impurities.

Results of modeling

The modeling of the gettering process provides depth profiles of Fe concentration and radii of precipitates. This allows us to calculate the relative recombination rate for carriers diffusing from one surface of the wafer to the other by integrating the recombination rates over the thickness of the wafer, with those due to dissolved and precipitated impurities being additive. Relative lifetime is obtained as the reciprocal value of the recombination rate. Relative lifetime and recombination rate are calculated with respect to those at the beginning of the process, with the sample considered to have been quenched from the gettering temperature down to room temperature at the termination of the gettering process. This provides a way to compare measured and modeling results and predict the efficiency of a gettering process. It should be noted that the calculated lifetimes are those determined by the impurity only. There may be other recombination centers in the crystal that affect the lifetime.

Time dependencies of relative carrier lifetime in different processes are shown in the Fig. 1. They differ by the temperature regime. Light curves correspond to constant temperature processes. It can be seen that gettering at lower temperatures allows to obtain larger lifetime improvement, but at the expense of longer gettering times, mainly needed for dissolving the precipitates. In the process carried out at 700 °C, the temperature of precipitation is never exceeded and thus, the concentration of dissolved impurity does not exceed the initial value. As a result, the lifetime remains as large as, or larger than the original lifetime. In higher temperature processes, at the

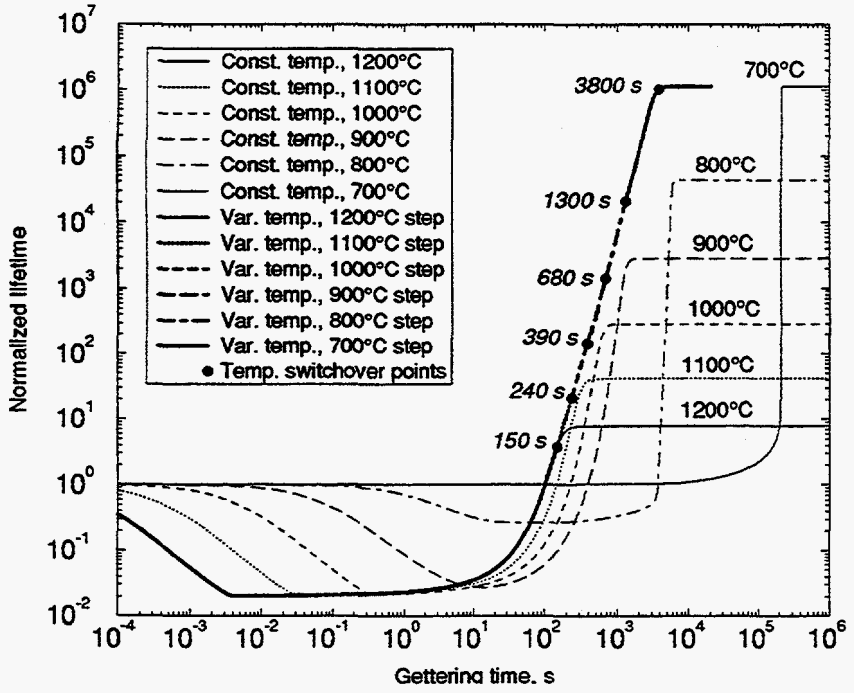

Fig. 1. Normalized carrier lifetime as function of gettering time. The light lines correspond to constant temperature processes. The heavy line corresponds to variable temperature process with temperature swithchover points shown. Normalization is done with respect to the lifetime at the beginning of the process.

earlier stage, dissolution of precipitates populates the Si matrix with more dissolved Fe atoms, since the outdiffusion rate of Fe atoms to the gettering Al layer is lower than the rate of Fe atom dissolution from the precipitates. Consequently, the lifetime can drop by orders of magnitude at higher temperatures. As soon as all the precipitates are dissolved, the lifetime starts to increase due to the outdiffusion of impurity. It may take as little as 100 s to restore the original level of lifetime at 1200 °C, and as much as 4000 s at 800 °C. This explains the fact that the carrier lifetime may drop as a result of impurity gettering in multicrystalline Si. Moreover, under certain conditions, the lifetime can decrease after gettering process, no matter for how long it is conducted. For instance, with initial Fe precipitate concentration of 10^{10} cm^{-3}, Fe saturation temperature 1000 °C, and precipitation temperature 600 °C, gettering at 1200 °C, conducted for sufficiently long, so that the equilibrium is achieved, results in lifetime decrease by a factor of 3. This can be understood considering the fact that although total concentration of Fe is much lower after gettering, before the gettering, most of the impurity is in precipitated state, and thus is electrically much less active.

We suggest a variable temperature process so as to take advantages of both the high and low temperature processes: short gettering duration and large lifetime. At the earlier, high temperature stage, dissolution of precipitates and prominent outdiffusion of dissolved impurities occur. At the later, low temperature stage, the concentration of Fe is brought down to a low value. In order to further shorten the gettering duration, a multi-stage process was considered (shown as bold curve in the diagram). For this case, the temperature is decreased by 100 °C at each step, from 1200 to 700 °C. As a result, a high lifetime increase proper to 700 °C process can be achieved in just about 1 hour as compared to 55 hours in a constant temperature process. Continuous temperature change could shorten the duration slightly more.

Conclusion

Calculations of minority carrier lifetime in the course of gettering using the derived expression for effective capture crosssection of precipitates provide a useful tool in evaluating the gettering efficiency. Numerical modeling of external aluminum layer gettering of impurities from multicrystalline Si for solar cell production has provided an explanation for the conventional application of this process which was found to be of a limited efficiency, and/or sometimes of a harmful effect. Variable temperature gettering process can significantly reduce the required duration of the gettering process without compromising the increase of carrier lifetime.

Acknowledgment

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Use of Design of Experiments and Balanced Analysis of Variance for Statistical Wet-Line Process Control

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Introduction

For solar cell production to mature, particularly in a climate where large profit margins on which to base development efforts are lacking, it is crucial that experimentation towards process control be pursued in as efficient a manner as possible. Toward this end, we present a case study for the use of classic *design and analysis of experiments* techniques to maximize the information content of a wet-line process control study. Careful attention is paid to extraneous sources of variation through balance and randomization. Having performed the experiment in this way, balanced analysis of variance can be used for statistical analysis and, in this case, was able to reveal a two-way interaction that was significant. We study the impact of four different wet-line process steps on cell electrical performance for various positions in bath life.

Experiment

Solar cells were processed at the Camarillo facility of Siemens Solar Industries under standard process conditions. The experiment was designed to examine the effect of position in bath life on electrical performance of four different process steps: a damage etch (DE) which removes wiresaw damage from the wafering process, a texture etch (TE) which textures wafers for antireflection, a neutralization bath (N), and a post diffusion etch (PDE) for removal of phosphor silicon glass (PSG). The three conditions of DE examined were immediately after changing (DE1), half way through the bath life (DE2), and just prior to changing (DE3). The four conditions of TE bath examined were just after changing the bath (TE1), immediately preceding a bath recharging step (TE2), immediately following the recharge (TE3) and just prior to bath change (TE4). The N and PDE baths were both examined for the cases of just after bath renewal (N1 and PDE1 respectively) and just prior to renewal (N2 and PDE2).

Experimental Design

The experimental design treatment structure consisted of three levels of DE within two levels of N and a further subdivision of the DE plots i.e. wafer groups into four sub-plots of TE. Consideration was also given to the PDE with its introduction as a two level unbalanced factor.[1] As the significant factors were found to be only DE and TE, the matrix collapses down into a balanced, two factor, mixed level design with DE at three levels (DE(3)) as the whole plot factor and TE(4) as the sub-plot factor.

Once the design has been formulated with respect to the variables to be systematically altered, design for control of unintentional variation in the process is needed. From the wet line to electrical test, a combination of holding variables constant, balancing with respect to, and randomizing against possible confounding proved to be effective. The error control strategy into the damage/texture etch system consisted of using wafer material from only one ingot and randomizing into sample groups with respect to ingot position. Factors held constant were plasma reactor, wet-line basket, and position with in the particular diffusion tube and oxidation tube used. Randomization was used to eliminate systematic variation during printing, firing and cell testing. Other sources of error were beyond systematic control and will show up in the random variation of the data during analysis. Sample size for each case was a boat of not less than twenty wafers per treatment combination with averages of the data being used to develop the effect estimates.

The experiment was followed as per the design and testing results were compiled for values of short circuit current (Isc), open circuit voltage (Voc), and fill factor (FF) for each cell. Pull strength of ribbon strips

soldered to cell contacts was measured on five cells per run and texture structure and quality were viewed via scanning electron microscopy (SEM) for one sample per run.

Results&Analysis

Since the TE and DE factors are balanced, cell data analysis can be performed by means of balanced Analysis of Variance (ANOVA)[1] demonstrating which trends are statistically relevant. The sampling scheme, error control strategy and treatment structure were sufficient to allow the estimation of a two-way, balanced ANOVA model of the damage/texture etch system into Isc and Voc. The ANOVA further revealed that pull strength is not significantly affected by the condition of the DE, TE, N or PDE. In the electrical performance metrics, variation in bath condition in N or PDE had no statistically significant impact. FF was additionally not significantly impacted by variation in DE or TE bath condition. Texture coverage correlates directly with values of Isc and Voc, however the variations in qualitative texture structure for the range of structure observed in this study is not correlated to electrical performance.

Figure 1 illustrates the two-way interaction of DE basket and TE basket on Isc. The figure demonstrates that for the DE1 and DE2, varying TE basket has no significant impact. In addition, having a fresh or recharged TE bath, TE1 and TE3 respectively, overcomes the significance of the final DE. It is only for the case of depleted DE bath (DE3) coupled with a depleted TE bath (TE2 and TE4) that we see a statistically significant variation in Isc.

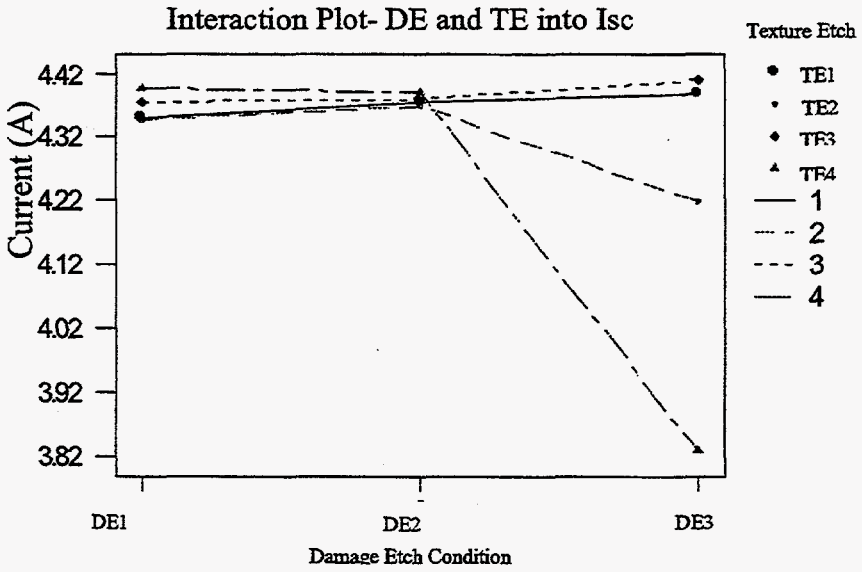

Figure 1. Two-way Interaction of DE and TE on Isc.

The associated ANOVA table follows in Table 1 (see ref. 1). These values allow for determination of statistical significance for the variation in mean values of treatment combination runs. Note the P value,

Analysis of Variance (Balanced Designs)

Factor	Type	Levels	Values			
DE	fixed	3	1	2	3	
TE	fixed	4	1	2	3	4

Analysis of Variance for Isc

Source	DF	SS	MS	F	P
DE	2	0.139525	0.069762	33.73	0.000
TE	3	0.122893	0.040964	19.81	0.000
DE*TE	6	0.314400	0.052400	25.34	0.000
Error	12	0.024818	0.002068		
Total	23	0.601635			

Table 1. ANOVA results for DE and TE into Isc

which represents the probability that the variation observed is due to some random influence rather than the factor of that row. P is very close to zero for this two-way interaction, indicating a high level of statistical significance for that factor. Similar analysis shows a similar effect on Voc under various conditions of the DE and the TE baths.

Qualitative groupings of run numbers were made on the basis of texture appearance as seen in the SEM micrographs. The main features of difference in appearance were the amount of coverage, size of the pyramids, and the distribution of the different size pyramids. On plotting Isc values by groupings based on similarity in texture coverage and microstructure (Figure 2), we see a significant dependence on the relative amount of texture coverage and no variation on the basis of texture structure otherwise.

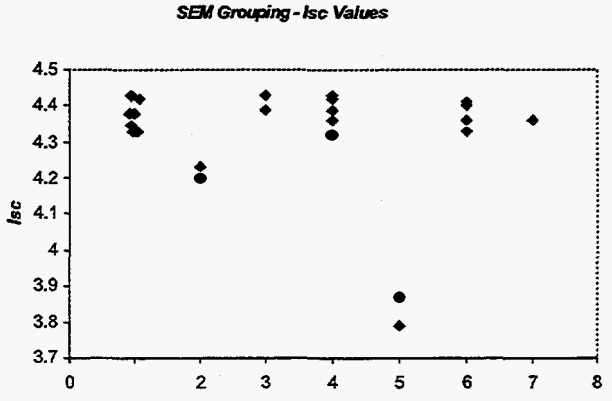

Figure 2. Chart of the run Isc values against qualitative groupings of texture quality based on SEM images.

The following figures show scanning electron microscope (SEM) images of the surfaces of sample runs. The magnification in each of these figures was 2,000x with an electron beam energy of 5 keV. The figures below show the condition of the texture under the two extreme conditions of DE and TE. Figure 3 is a SEM micrograph of a cell processed with a new DE and a new TE bath. This figure shows that the pyramids cover the entire surface uniformly.

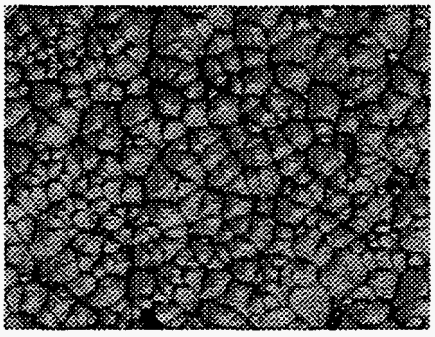

Figure 3. SEM image of the surface of a wafer in run with a new DE followed by a

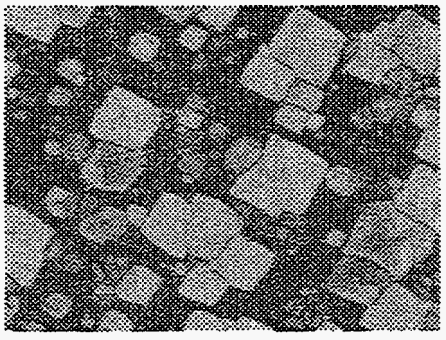

Figure 4. SEM image of the surface of a wafer in run with an old DE followed by an old TE.

Figure 4 is a SEM micrograph of a cell processed with an old DE and an old TE bath. Although the sizes of the pyramids are consistent, this micrograph shows significant surface area without any texturing.

The effect of recharging the TE bath is significant to the texture formation in the case where the wafers have been processed in an old DE bath. The following photographs reflect these differences. Figure 5 shows the areas on the cell surfaces (TE2) with gaps i.e. areas with no pyramids. Whereas wafers

processed under the same conditions in all previous steps but texture etched after TE recharging (TE3) show a uniform textured surface with considerably less gaps on the surface (Figure 6).

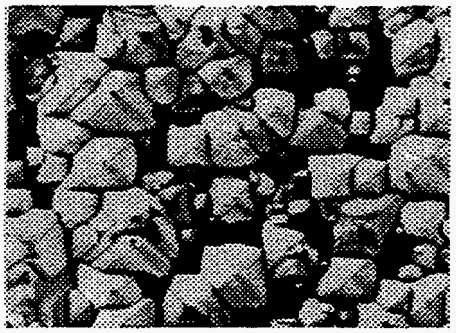

Figure 5. SEM image of the surface of a wafer in run with an old DE followed by a pre-recharged TE.

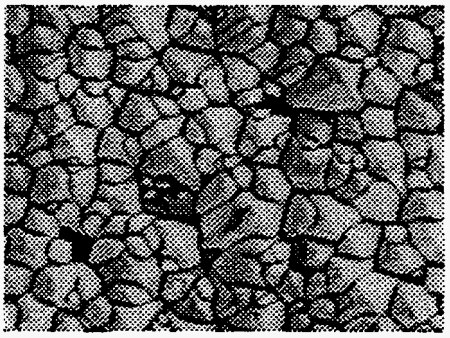

Figure 6. SEM image of the surface of a wafer in run with an old DE followed by a post-recharged TE.

These results clearly demonstrate the relationship between texture coverage and cell performance to the two-way interaction of DE condition and TE condition for the current process.

Conclusions

The Isc value of the cells in this experiment are in direct correlation with Voc values although the strength of the Voc dependence on DE and TE bath condition is weaker than for Isc as is to be expected from the logarithmic dependence of Voc on Isc. The ideal relationship is as follows:[2]

$$Voc = kT/q \ \ln(Isc/Io + 1)$$

where k is Boltzmann's constant, q is the charge on an electron, T is temperature in Kelvin and Io is the saturation or reverse bias current of the diode. Transforming the data to see the impact of DE and TE bath conditions on Io shows there is a statistically significant variation were Io increases for the combination of DE3 with either TE2 or TE4, however the dominant change in Voc is due to changes in Isc. Since texture is for the purpose of reducing reflection of incident light[3], it is understandable how reducing the texture coverage will reduce Isc. The structure of the texture, large uniform pyramids vs large pyramids interspersed with smaller pyramids, did not show a significant difference in performance. This indicates that either the texture structure has no significant impact on Isc and subsequently Voc or that the structure variation is masked by the random variation in our cell fabrication process. While there is correlation between texture coverage and Isc and texture coverage and Io, it cannot be quantitatively determined that other factors that are changing with bath condition are not also impacting these values.

In summary, the use of experimental design with careful consideration for error control and statistically relevant sampling has been used to analyze wet-line processes in a manufacturing environment. With these tools, conclusions can be drawn in spite of the vast amount of variation within and interconnections between the many processing steps in photovoltaic cell fabrication.

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Investigation of Post-Growth Treatments of Silicon-Film ™

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Abstract: Post-growth thermal treatments of Silicon-Film ™ polycrystalline silicon sheet materials are investigated with the aim of developing a manufacturing process that can improve minority carrier diffusion lengths during the solar cell fabrication. These treatments involve annealing and/or gettering over a wide range of processing variables (temperature, time, ambient, etc.). Long diffusion lengths are observed using a proper combination of thermal annealing and phosphorus gettering. Some unusual solid state phenomenon were also observed for certain Silicon-Film ™ materials. Efforts to characterize these phenomenon and deduce their underlying mechanisms are described.

Experimental: Gettering processes typically used with silicon solar cells are based on phosphorus diffusion or aluminum alloying, singularly or in combination. The gettering efficiency in polycrystalline silicon is usually limited by the defect density, specific defect structures, and impurity species. The response of polycrystalline silicon to high temperature treatments can be highly variable. The gettering process used for high efficiency Silicon-Film ™ solar cell processes features a "co-gettering" with phosphorus diffusion and aluminum alloying performed for extended duration [1]. In this work, we attempt to differentiate thermal effects from gettering effects due to post-growth processing. High-temperature annealing treatments were performed at temperatures ranging from 700°C to 1150°C in N_2 and H_2 ambients. Diffusion lengths in the treated materials are measured using spectral response data taken on semi-transparent Schottky diodes. The annealed Silicon-Film ™ materials were then subjected to phosphorus diffusion to examine the changes in carrier diffusion lengths. To simplify the gettering process and make it compatible with a continuous production process, a finite-source phosphorus gettering was implemented and evaluated at the optimal annealing temperature. Hall effect measurements show the effects of gettering treatments on majority carrier transport, and FTIR spectroscopy indicates the behavior of oxygen and carbon in the bulk Silicon-Film™ material during various stages of processing.

Results and Discussions: An annealing treatment that simulated the temperature schedule of the gettering process indicated that annealing has a profound effect on the efficacy of gettering Silicon-Film ™. Annealing treatments not only improve carrier diffusion lengths, but also enhance the effects of phosphorus diffusion gettering. A systematic optimization of the annealing treatment was undertaken. An optimal annealing temperature at around 900°C, where the Silicon-Film ™ is "activated", was deduced. This suggests the possibility of advantageously combining gettering with annealing using a finite source of gettering agents so that the gettering and annealing occur simultaneously. FTIR data taken on samples with different thermal treatments indicated that a reduction in interstitial oxygen contents from $10\times10^{17}cm^{-3}$ to

$3\times10^{17}cm^{-3}$ is mostly attributed to the high temperature annealing treatments. This reduction may be responsible for the observed increase in gettering efficiency.

In addition to changes in minority carrier diffusion lengths, high temperature treatments were found to increase the bulk resistivity of some Silicon-Film ™ materials. Doping behavior and/or majority carrier transport properties can be modified during high temperature treatments. Hall measurements indicate that resistivity increases are due to a reduction in Hall (majority carrier) mobility. Assuming that the minority carrier (electron) mobility is decreased due to the charged scattering centers, there are then two opposing effects on diffusion length during the gettering: a decrease in mobility and an increase in carrier lifetime. Depending upon which effect dominates, the gettering results (diffusion lengths) could be quite different, either beneficial or deleterious.

An unexpected phenomenon associated with post-growth Silicon-Film™ treatments is an unusual illumination-dependent bulk minority carrier recombination behavior. Specifically, the solar cell long-wavelength spectral response decreases as bias-light intensity increases [2] for some thermally-treated materials. Diffusion length measurements on Silicon-Film ™ samples that were gettered for different times indicated that, as the gettering time increases, the diffusion lengths measured under light bias increase, but the difference between dark and light-bias diffusion lengths also becomes more pronounced. The practically instantaneous transition in the diffusion length response between dark and light bias conditions leads us to speculate that the light-bias effect on diffusion length is due to localized space charge regions. During post-growth treatments, impurities may be segregating to defect regions such as dislocations and grain boundaries where the charge state at these regions as well as the filling state of trap levels can be changed. If defect regions, e.g., GBs, are depleted or inverted, the local recombination rate can be modified and the recombination rate would be inversely dependent on injection level. An effort to mediate this behavior employed additional aluminum treatments on the front side before emitter formation. Because the aluminum diffusion rate is quite high in defect regions and along grain boundaries, and since aluminum is a *p*-type dopant, this additional treatment should reduce the space-charge region effect surrounding defect regions and passivate deep-level traps/recombination centers with a consequent reduction of illumination dependence. A reduction in, and even a reversal of, illumination dependence has been observed in some samples, but an improvement over untreated cases in ultimate diffusion lengths under light-bias was not observed, suggesting different effects of annealing and gettering on bulk recombination.

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FILM SILICON SOLAR CELLS ON CERAMIC SUBSTRATES

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1. INTRODUCTION

In the Dutch project for film-Si solar cells on ceramic substrates, different techniques for the deposition of silicon for use in film-Si solar cell have been applied. Techniques for film-Si deposition in this project are thermal CVD [1], LPE [2] and hot-wire CVD [3]. The demands on the deposited film-Si layer are a compact and coherent morphology and a diffusion length of minority carriers in the order of the layer thickness, i.e. about 10-20 µm. It could be an advantage if the crystal grain sizes in such film-Si is in the same order of magnitude because of a potential negative influence of grain boundaries on the diffusion length of minority carriers. A higher film-Si quality is also a cost reducing factor because higher cell efficiency could reduce film-Si solar cell costs together with lower material costs from cheap ceramics. Therefore low cost silicon based ceramic substrates for use in Si-film devices have been produced by either the tape casting method or the atmospheric plasma spraying method APS and advanced film-deposition techniques have been applied to reach high quality films on top of the applied substrates 4. The thermal expansion coefficient of the ceramic substrates have been investigated as one main parameter to minimise mismatch problems in Si-film devices. The plasma sprayed silicon layers can be improved by a recrystallization process, i.e. larger grain sizes and lower porosity can be achieved. A standard liquid phase epitaxy LPE process and chemical vapour deposition CVD using a cold wall RF heated reactor have been applied for growing silicon layers on the low cost ceramic substrates. Compact and coherent Si-film layers have been achieved on different ceramic substrates by both deposition techniques. For those substrates for which a different thermal expansion coefficient to silicon have been measured, plastic deformation of the entire sample has been observed after deposition by CVD technique.

2. EXPERIMENTAL

2.1 Ceramic substrates

Ceramic substrates for use in film-Si solar cells have been made by two different techniques, i.e. atmospheric plasma spraying APS and tape casting [5]. The mullite and SiAlON substrates have been produced by the **tape casting** technique. For mullite the mixed oxide route starting with commercial Al_2O_3 and SiO_2 powders followed by a sinter/reaction process at 1600°C for 1h in air have been used. The nitride based ceramic SiAlON has been produced by tape casting starting with commercial SiAlON powder. Samples have been sintered at 1550 °C for 1h in Ar. For a modification of the SiAlON substrate 43 wt% Si-powder was added as a second phase to the slurry to reach better conductivity and more nucleation sites. This modified substrate will be called SiAlON-Si in the following. Samples have been sintered by using the same conditions as for SiAlON substrates. The **atmospheric plasma spraying technique (APS)** has been applied for fast deposition of Si-coating on SiAlON-Si substrates. The layer will be called APS-Si in the following. Coating of thin APS-Si layers on ceramic substrates gives additional nucleation and diffusion barrier layers for the deposition of Si-films by LPE or CVD processes. The used Si powder has a grain size of 25-75 µm. An Ar/H_2 plasma has been used as heating source. The thickness of the plasma sprayed APS-Si layers is 40-150 µm.

2.2 Techniques for recrystallization and film-Si deposition

To obtain larger grain size and a lower impurity concentration in the APS-Si layer, recrystallization experiments have been carried out with a zone melting heater **ZMH** constructed at ISE/Freiburg in

Germany [6] The used APS-Si layers on SiAlON-Si substrates were coated with a SiO_2 layer by plasma enhanced chemical vapour deposition (PECVD) at ISE in Freiburg/D in order to prevent the layer from oxidizing and cracking during the recrystallization process. For more details see [6]. At present the most common techniques for deposition of a thin Si-film on foreign ceramic substrates are liquid phase epitaxy LPE where the Si-film is deposited from an over-saturated solution and the CVD technique. A standard **LPE** process was used for growth of film-Si on different type of substrates. A more detailed description of the process is given in Ref. [2]. For application of the chemical vapour deposition CVD the Si-film is deposited from the gas phase after chemical decomposition of a precursor as for example dichlorosilane DCS. Conventional thermal **CVD** was used to deposit silicon on ceramic substrates. The reactor, which has been applied, is a cold wall type reactor. A more detailed description of the reactor and the morphology of deposited film-Si on thermally grown SiO_2 layers are described in Ref. [1].

3.RESULT AND DISCUSSION

3.1 Morphology of ceramic substrates

In Fig. 1 examples of the morphology of the used substrates are given. In Fig. 1a a mullite surface is presented which shows larger open pores at the surface. A porosity of 10-15% has been measured at the mullite surface. In Fig. 1b an example of a SiAlON substrate surface is presented at a higher magnification. The surface of the sample consists of smaller grains, 1-2 µm in diameter. The surface is macroscopically smooth and the observed porosity is about 3%. In Fig 1c an example is given of the modified SiAlON substrate surface, i.e. SiAlON-Si with 43 wt% Si-powder. Silicon crystallites with different sizes, about 1 to maximum 20 µm, are visible at the substrate surface. In Fig. 1d a cross section is given of a plasma sprayed APS-Si layer on top of a SiAlON-Si sample. The shown APS-Si layer is 150 µm thick. The layer can be described as compact and coherent to the substrate with a roughness of about 5 µm. The APS-Si layer is mechanically stable and nearly crack free. The porosity is high, 10-15%, which is typical for this deposition technique. The pores are irregularly distributed all over the layer. Additional *free standing* APS-Si bodies have been made with comparable morphology but 350µm thickness, excluding a additional substrate.

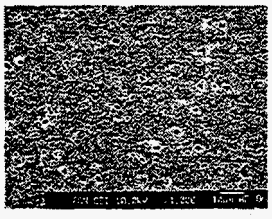

Fig. 1a: Mullite surface after reaction sintering at 1600°C for 1h in air

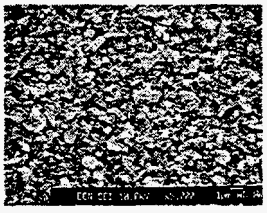

Fig.1b: SiAlON surface after sintering at 1550 °C for 1h in Ar at a higher magnification

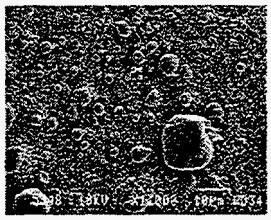

Fig. 1c: SiAlON-Si surface with 43wt% Si after sintering at 1550 °C for 1h in Ar

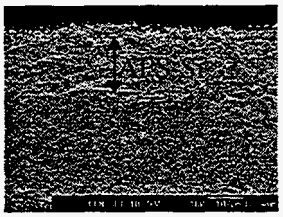

Fig.1d: Cross section of a APS-Si plasma sprayed silicon layer on top of a SiAlON-Si substrate

3.2 Material properties of selected ceramic substrates

In Table I material properties of the tape cast and plasma sprayed ceramics are given together with data for monocrystalline silicon for comparison purposes.

Table I: Material properties of selected ceramics; *Ra* Roughness, *E* elastic modulus, *R* resistivity and λ thermal expansion coefficient

substrates	*Ra (µm)*	*% porous*	*E (GPa)*	*R (Ω·cm)*	$\lambda\ (10^{-6}K^{-1})$
c-Si*	1		110	10^{-5}	5
mullite	1.0	80-85	140	10^{14}	4 - 7
SiAlON	3	98	290	1	4
APS-Si	5-6	80-85	<110	1	5

*data for a ⟨100⟩ monocrystalline silicon wafer for comparison

In Table I APS-Si and SiAlON have expansion coefficients which are comparable to silicon and thermal mismatch problems are therefore not expected. For the mullite substrate the situation seems is more complex, since the thermal expansion coefficient is strongly related to the SiO_2 concentration [7]. For processes including drastic temperature variations as for example APS or CVD, a sufficient thermal shock resistance of the applied substrate is of great interest. The thermal shock resistance of ceramic materials is directly related to the elastic modulus [8]. Therefore mullite substrates are less preferred then SiAlON substrates with a high thermal shock resistance. The electrical resistance for the oxides is typically high and backside contacting seems to be an option only for SiAlON, SiAlON-Si and APS-Si substrates. For the non conducting mullite ceramic a solar cell concept with a full front side-contacting scheme is preferred. The addition of silicon to SiAlON to form SiAlON-Si substrates affects the surface roughness. The roughness *Ra* changed from 3.2 to 4.5 µm for the Si rich ceramic. The higher value was effected by the observed Si particles on the SiAlON-Si substrate surface (see also Fig.). For the other oxide based ceramics in Table II a much smoother surface has been measured, similar to commercial mono Si-wafers.

3.3 Recrystallization of sprayed layers and film-Si deposition on ceramic substrates

To improve porosity, grain size and impurity concentration of the APS-Si layer a sample with SiAlON-Si as substrate and a 40 µm thick plasma sprayed APS-Si layer on top has been recrystallized at ISE/Freiburg in Germany. In Fig. 2a a cross-section is given after recrystallization. A grain is visible having dimensions of up to several hundreds of microns. The surface is nearly flat and no cracks can be observed. Deformation of samples or other effects from material property mismatches between Si-layer and substrate could not be detected. The adhesion of the recristallised APS-Si layer to the substrate is still excellent. In Fig. 2a it is also visible, that the Si particles in the SiAlON-Si substrate are recrystallized. Beside recrystallization tests, nucleation and growth of film-Si on the developed ceramic substrates have been performed. The solution growth or liquid phase epitaxy (LPE) is carried out at ECN and the thermal chemical vapour deposition CVD is carried out at DIMES at TU Delft. In Fig. 2 results are given for both deposition techniques. Fig.2b presents the cross section of a film-Si on SiAlON substrate which have been deposited by CVD technique. The film is dense and coherent to the SiAlON substrate. No sample deformation from material mismatch has been observed after deposition. In Fig.2c a cross section of a film-Si is shown which have been deposited by LPE technique on a APS-Si layer. Also here the film is dense and coherent to the APS-Si substrate without material mismatch problems.

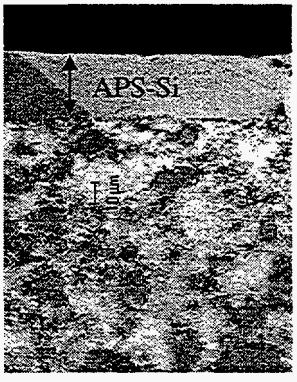

Fig.2a: Cross section of a APS-Si layer on top of a SiAlON-Si substrate after recrystallization at ISE in Freiburg/D

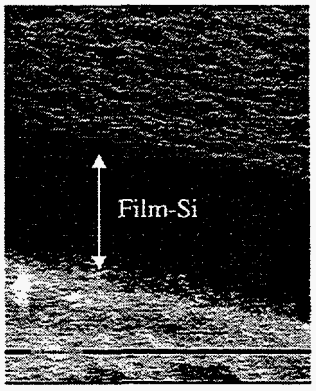

Fig2b: Cross section of CVD deposited film-Si on top of a SiAlON substrate performed at TU-Delft/DIMES (marker 5µm)

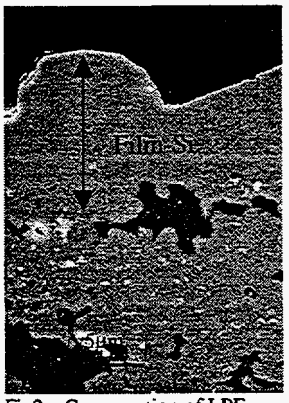

Fig2c: Cross section of LPE deposited film-Si on top of a APS-Si substrate performed at ECN

For summarising experimental results, in Table II a short overview is given for zone melting recrystallization ZMR and growth experiments using LPE and CVD technique. For further experimental details see also literature references [1][2][4][6].

Table II: Test results for zone melting recrystallization ZMR and growth experiments by LPE and CVD technique on various ceramic substrates

	APS-Si	*SiAlON*	*SiAlON-Si*	*mullite (higher expansion coefficient)*
LPE[1]	dense Si-film	not yet tested	dense Si-layer	not yet tested
CVD[2]	dense Si-film	dense Si-film	dense Si-film	dense Si-film, sample deformed
ZMR[3]	dense Si-layer			

On APS-Si type substrates dense a compact Si-layers by ZMR could be demonstrated. On this type of substrate (non recrystallized) and on SiAlON type, dense Si-films by LPE and CVD could be reached. Experiments of Si-film deposition on mullite substrates have shown deformation effects because of expansion mismatch problems. The entire sample has deformed due to thermal stresses. This indicates again the significance for an optimised expansion coefficient for substrate materials to be used for film-Si deposition.

4. CONCLUSIONS

For the present state of research it can be concluded that ceramic type substrates can be used in principle for Si-layer recrystallization and film-Si growth, but further optimisation in particular of the mullite ceramic has to be achieved, e.g. by optimisation of the SiO_2 content.

Tape casting and plasma spraying of ceramic powders can be used to produce ceramic type substrates on a larger scale for deposition of Si-film.

The thermal expansion coefficient of selected ceramics has to be close to Si to overcome thermal mismatch problems. Therefore mullite with lower SiO_2 content seems to be less qualified.

Recrystallization of APS-Si layers leads to larger grains and lower porosity. Deposition of film-Si has been demonstrated on non recrystallized APS-Si and on SiAlON type substrates. Dense and coherent to the substrate grown Si-films could be realised by LPE and CVD technique. It is very probable, that the growth results on APS-Si type substrates can be further improved if this layer is recrystallized before film-Si deposition.

ACKNOWLEDGMENT

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[3] performed by ISE/Freiburg/D

IMPROVED PERFORMANCE OF SELF-ALIGNED, SELECTIVE-EMITTER SILICON SOLAR CELLS

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ABSTRACT: We improved a self-aligned emitter etchback technique that requires only a single emitter diffusion and no alignments to form self-aligned, patterned-emitter profiles. Standard commercial screen-printed gridlines mask a plasma-etchback of the emitter. A subsequent PECVD-nitride deposition provides good surface and bulk passivation and an antireflection coating. We used full-size multicrystalline silicon (mc-Si) cells processed in a commercial production line and performed a statistically designed multiparameter experiment to optimize the use of a hydrogenation treatment to increase performance. We obtained an improvement of almost a full percentage point in cell efficiency when the self-aligned emitter etchback was combined with an optimized 3-step PECVD-nitride surface passivation and hydrogenation treatment. We also investigated the inclusion of a plasma-etching process that results in a low-reflectance, textured surface on multicrystalline silicon cells. Preliminary results indicate reflectance can be significantly reduced without etching away the emitter diffusion.
Keywords: Passivation – 1: Silicon-Nitride – 2: Texturisation - 3

1. INTRODUCTION

The purpose of our work is to improve the performance of standard commercial screen-printed solar cells by incorporating high-efficiency design features without incurring a disproportionate increase in process complexity or cost. Our approach uses plasma processing to replace the heavily doped homogenous emitter and non-passivating antireflection coating (ARC) with a high-performance selectively patterned diffusion covered with a passivating ARC. A slight variation of the plasma step can effectively texture even multicrystalline silicon (mc-Si) surfaces to significantly reduce front surface reflectance.

1.1 Passivated, Patterned Emitter

Plasma-enhanced chemical vapor deposition (PECVD) is now recognized as a performance-enhancing technique that can provide both surface passivation and an effective ARC layer [1]. For some solar-grade silicon materials, it has been observed that the PECVD process results in the improvement of bulk minority-carrier diffusion lengths as well, presumably due to bulk defect passivation [2].

In order to gain the full benefit from improved emitter surface passivation on cell performance, it is necessary to tailor the emitter doping profile so that the emitter is lightly doped between the gridlines, but heavily doped under them [3]. This is especially true for screen-printed gridlines, which require very heavy doping beneath them for acceptably low contact resistance. This selectively patterned emitter doping profile has historically been obtained by using expensive photolithographic or screen-printed alignment techniques and multiple high-temperature diffusion steps [3,4].

We have attempted to build on a self-aligned emitter etchback technique described by Spectrolab that requires only a single emitter diffusion and no alignments [5].

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Reactive ion etching (RIE) using SF_6 etches back the emitter but leaves the gridlines and emitter regions beneath them unetched. This removes the heavily diffused region and any gettered impurities between gridlines while leaving the heavily doped regions under the metal for reduced contact resistance and recombination. This leaves a low-recombination emitter between gridlines that requires good surface passivation for improved cell performance. Therefore, we follow the etchback with a surface-passivating PECVD-nitride layer. The nitride also provides a good ARC and can be combined with plasma-hydrogenation treatments for bulk defect passivation.

1.2 Textured, Low-Reflectance Emitter

Several groups have reported interest in plasma-etching techniques to texture mc-Si cells, because mc-Si cannot benefit sufficiently from the anisotropic etches typically used for single-crystal Si. In contrast to laser or mechanical texturing, plasma-etching textures the entire cell at once, which is necessary for high-throughput. Inomata et al. used Cl_2-based RIE on mc-Si to fabricate a 17.1% efficient cell, showing that plasma-texturing does not result in performance-limiting surface damage [6].

We developed a variation of the SF_6 emitter etchback process, which results in good surface texturing. Use of SF_6 keeps the process compatible with the metal gridlines. This allows the texturing to be done after the metallization step as part of the emitter-etchback process.

2. EXPERIMENTAL PROCEDURE

The textured, self-aligned selective-emitter (SASE) plasma-etchback and passivation process is shown in Figure 1. The SASE concept uses cells that have received standard production-line processing through the printing and firing of the gridlines. Then the cells undergo reactive ion etching (RIE) to first texture and etch away the most heavily-doped part of the emitters in the regions between

the gridlines, increasing the sheet resistance in these areas to 100 ohms/square.

For emitter etchback, we used a new PlasmaTherm 790 reactor. This is a commercial RF dual parallel-plate reactor operating at 13.56 MHz. This equipment is IC industry-standard, programmable, and capable of being configured in a cluster-tool arrangement for high-throughput. Wafers were etched in pure SF_6 at a powers between 15 and 45 W and pressures ranging from 100 to 150 mTorr. Gas flow rates were between 14 and 26 sccm.

For texturization, we performed room-temperature RIE in a Technics, PEII-A parallel-plate reactor. We used mixtures of SF_6 with varying amounts of O_2. RF power ranged from 50 to 300 W.

Wafers received a silicon-nitride deposition (PECVD-nitride), using conditions similar to those found to be effective for bulk and surface passivation in String Ribbon™ mc-Si [2]. The plasma-nitride depositions were performed using the PECVD chamber of the PlasmaTherm reactor. Reaction gases for nitride deposition were a 5% mixture of silane in helium, nitrogen, and anhydrous ammonia. The optional H-passivation treatment consists of an exposure to a pure ammonia plasma between 300-400C in the PECVD reactor. We found that less power is required to generate a NH_3-plasma than a H_2-plasma, resulting in less surface damage. Nitride-coated cells then receive a forming gas anneal (FGA) at 300C for 30 minutes. The cells at this point are returned to the production-line for final cell processing, if any.

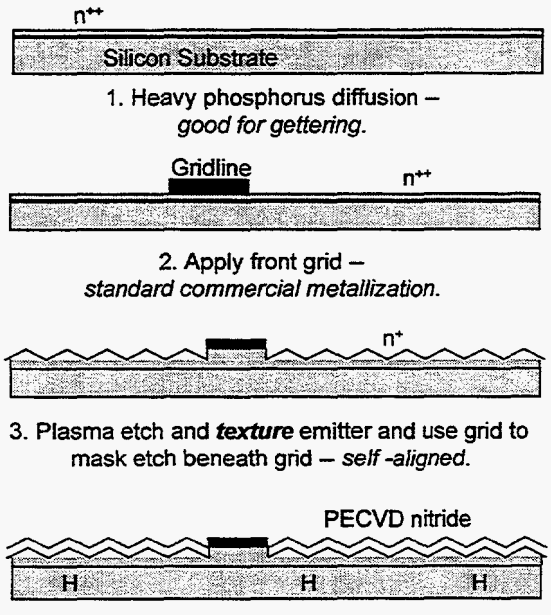

Figure 1. Process sequence for textured, self-aligned selective-emitter cells. The emitter etchback can be done after texturization to remove any surface damage the texturing may cause.

3. EXPERIMENTAL RESULTS

3.1 Emitter-Etchback Studies

The key to the success of the SASE process lies in finding an etching technique that results in uniform emitter etchback while avoiding both gridline and silicon surface damage. We investigated Si etch rates and uniformity for various RIE parameters using the PlasmaTherm reactor and compared them with those obtained using an older but similar Vacutec reactor, which produced SASE cells with half a percent higher efficiency than control cells [7]. Uniformity was monitored by measuring emitter sheet resistance over the full 130-cm^2 area of commercial wafers after the etchback. Surface damage was monitored by measuring the emitter saturation current density (J_{oe}) on high-resistivity float-zone wafers after passivation with a PECVD-nitride film [8].

We succeeded in finding a set of parameters for rf-power, flow rate, and pressure for the PlasmaTherm, which resulted in better uniformity and less surface damage than obtained with the Vacutec. The best result reduced uniformity variation from 10% to 2% and reduced J_{oe} from 270 to 225 fA/cm^2 on 100 Ω/sq. emitters.

3.2 Emitter-Passivation Studies

Our previous work with the Vacutec showed that we were able to obtain lower J_{oe} values and better surface passivation using a 3-step nitride deposition process compared to a single continuous deposition [7]. The 3-step process starts with deposition of a thin layer of nitride to protect the Si surface, followed by exposure to a NH_3-plasma, and finally the deposition of the remaining nitride required to attain the correct thickness for ARC purposes.

Comparison using the PlasmaTherm also showed better passivation using the 3-step process. We conducted a statistically designed multifactor experiment to find the 3-step parameters that would minimize J_{oe} on float zone wafers using our previous response surface methodology [7,8]. The results of a quadratic interaction experiment are shown in Fig. 2.

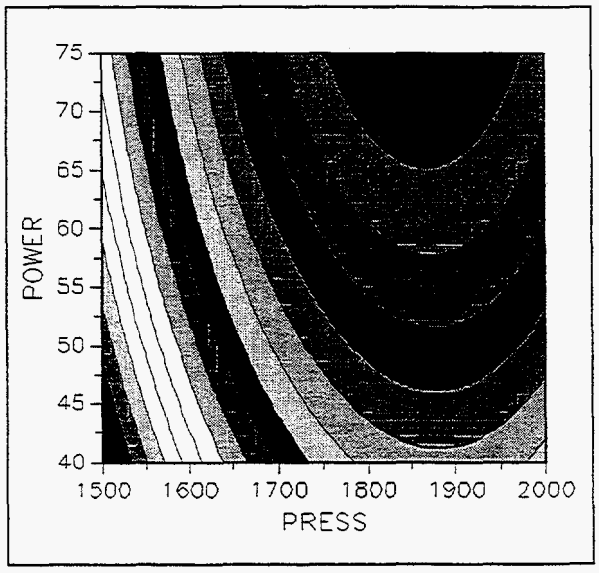

Figure 2. Contour plot showing response of J_{oe} to the power (W) and pressure (mT) during NH_3-treatment with a protective-nitride thickness of 10 nm. J_{oe} ranges from 216 in the lower left corner to a minimum of 161 fA/cm^2 near the upper right corner. The duration of the NH_3 hydrogenation was 20 minutes.

3.3 SASE cell processing

We used the parameters that produced minimum J_{oe} on 130-cm^2 cells processed up through gridline firing on the Solarex production line. We investigated whether shorter NH_3-treatments would retain the benefits of surface passivation. Results of IV testing are shown in Table. I.

Table. I: Six SASE sequences were applied to 12 Solarex mc-Si cells (2 cells/sequence) using matched material from the same ingot as the controls. Illuminated cell IV data ± standard deviation are shown normalized to a constant transmittance to account for the additional 1.1% spectral-weighted absorbtance in the nitride [11].

Eff. (%)	Jsc (mA/cm^2)	Voc (mV)	FF (%)
90 sec. RIE, **1-step** SiN, FGA			
12.3±0.4	30.5±.0.0	565±4	71.6±1.6
90 sec. RIE, **3-step** SiN, **5 min NH_3**, FGA			
12.9±0.1	30.6±.0.1	573±1	73.5±0.4
90 sec RIE, **3-step** SiN, **10 min NH_3**, FGA			
12.4±0.0	30.3±.0.0	570±0	72.0±0.0
150 sec RIE, **1-step** SiN, FGA			
12.1±0.5	30.1±.0.0	562±7	71.3±2.2
150 sec RIE, **3-step** SiN, **5 min NH_3**, FGA			
12.9±0.2	30.4±.0.3	576±4	73.5±1.4
150 sec RIE, **3-step** SiN, **10 min NH_3**, FGA			
13.0±0.2	30.4±.0.0	577±2	74.0±0.9
Control Cells: No emitter etchback, TiO_2 ARC			
12.6±0.0	30.2±.0.1	569±0	73.5±0.0

The first three groups of cells were not etched back sufficiently, because the etch duration did not account for etching through a thermal oxide that grew on the cells during gridline firing. These cells do not show consistent improvement over the controls.

The second three groups used a longer 150-second RIE-etch that removed the thermal oxide and then etched the emitters from their starting sheet resistance of 50 Ω/sq. to 100 Ω/sq.. The 1-step cells show a drop in performance compared to the controls, in agreement with our J_{oe} results that showed poorer passivation by a 1-step nitride. Once the emitter is etched back to 100 Ω/sq., it requires excellent surface passivation to avoid excess surface recombination.

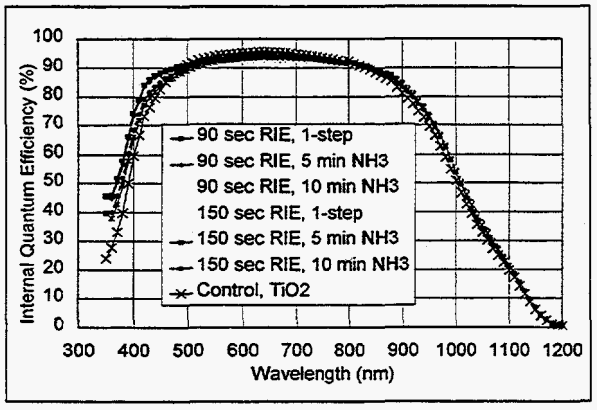

Figure 3. IQE for cells described in Table I.

The 3-step cells show significant improvements, especially in V_{OC}, suggesting longer diffusion lengths from bulk defect passivation. Internal quantum efficiency (IQE) of these cells, showing both improved red and blue response is shown in Figure 3.

All the nitride passivated cells show similar red and blue response, consistent with their similar J_{SC} values. The J_{SC} is no greater than that of the control cell because the increase in IQE is compensated by parasitic absorbtion in the nitride. This is due to the high refractive index of 2.2 used to minimize reflectance. Another series of SASE cells were processed using a lower refractive index of 2.12 to reduce the spectrally weighted absorbtance to 0.5%. Normalized IV data for these cells are shown in Table II.

Table. II: Three SASE sequences were applied to seven Solarex mc-Si cells using matched material from the same ingot as before. IV data are shown below normalized to the transmittance of the control cells.

Eff. (%)	Jsc (mA/cm^2)	Voc (mV)	FF (%)
140 sec RIE, **3-step** SiN, **5 min NH_3**, FGA			
12.9±0.2	31.1±.0.1	572±3	72.7±0.3
140 sec RIE, **3-step** SiN, **10 min NH_3**, FGA			
13.1±0.0	31.4±.0.1	574±0	73.0±0.1
140 sec RIE, **3-step** SiN, **20 min NH_3**, FGA			
12.2±0.4	31.2±.0.1	563±5	69.5±1.5
Control Cells: No emitter etchback, TiO_2 ARC			
12.3±0.1	30.8±.0.0	558±2	71.4±0.4

The SASE cells have consistently higher J_{SC} than the controls, because now the increased IQE due to passivation is not lost due to excessive parasitic absorbtion. The cells that received 10 minutes of NH_3-hydrogenation performed the best, exceeding the controls by almost a full percentage point due to the large improvement in V_{OC}. However, improvement in V_{OC} is reduced for the cells that received a 20-minute NH_3-exposure. These cells also suffered a loss in fill factor due to an increase in diode ideality factor.

3.4 RIE-textured cells

We developed an RIE process that uses SF_6/O_2 mixtures to produce a randomly textured surface on c-Si. Figure 4 shows an SEM of an RIE-textured sample with less than 0.5% spectral reflectance at all wavelengths.

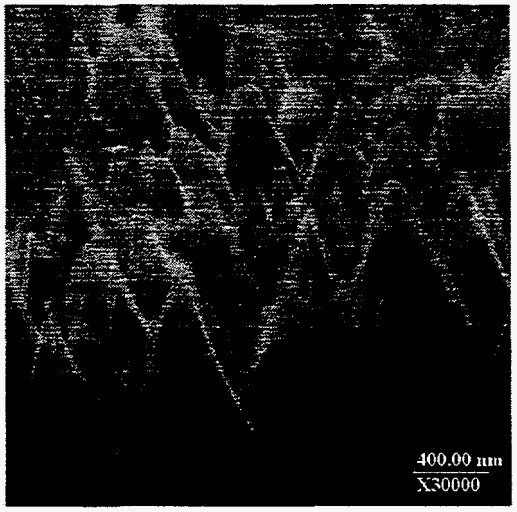

Figure 4. SEM of Si surface textured for 30 minutes.

About 6.0 μm of Si was removed from the surface shown in Fig. 4. This process could be applied to the wafers before emitter diffusion, when removal of a few micrometers of Si would not be an issue. The SASE process could then be applied after gridline firing as usual.

We developed a second process that could be applied after emitter diffusion since it removes only 0.1 μm from the surface, increasing the emitter sheet resistance to about 60 Ω/sq. This process requires the Si surface to be prepared in a simple manner using low-cost, low-temperature techniques. An SEM of such a textured surface prepared in this manner near a cleaved wafer edge is shown in Figure 5.

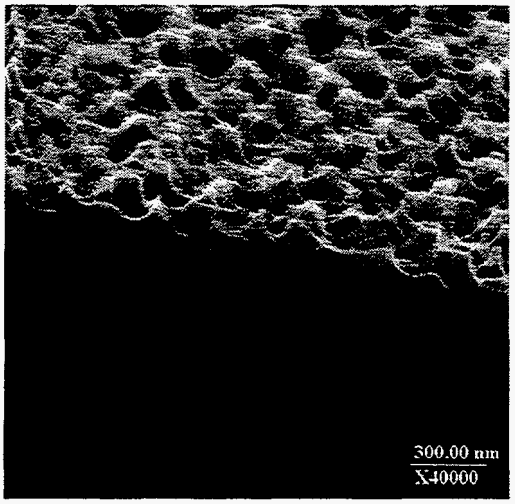

Figure 5: Textured Si surface with 0.1 μm feature sizes.

This second process was applied to single-crystal wafers with three different surface preparation conditions. Specular reflectance curves of the three resulting textures are compared to that of bare Si in Fig. 6.

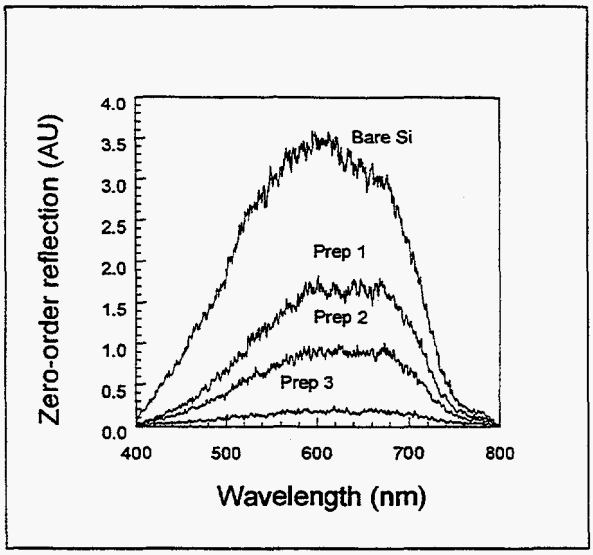

Figure 6: Specular reflectance of samples with three different surface preparation conditions. The reflectance of the textured samples has been reduced by a factor of 2.2, 4.4, and 24, respectively.

We applied this second process to full-size mc-Si wafers with gridlines using preparation conditions 1 and 2. These cells are currently in process at Solarex and could provide an increase of up to a full percentage point in efficiency due to reflectance reduction alone.

4. CONCLUSIONS

The SASE process has been improved using statistical experiments, more complete emitter etchback, and lower absorbtance nitride films to achieve nearly a full percentage point efficiency increase over the standard production line process. The use of an optimum-duration, ammonia-plasma hydrogenation treatment is crucial to the increased performance. In addition, plasma texturing has been shown to reduce reflectance significantly while removing only the heavily diffused portion of the emitter region. As a result, texturing could be included as part of the emitter etchback process.

5. ACKNOWLEDGMENTS

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Recent Advances in Silicon-Film™ Solar Cell Manufacturing Engineering

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The dimensions of Silicon-Film™ wafers and solar cells have increased from 10x10 cm to 15x15 cm during the AstroPower PVMaT-4 program. New solar cell processes for large-area junction diffusion and for AR coating were developed under the program. Solar cell fabrication processes are now being designed and developed within the AstroPower PVMaT-5 program to manufacture large-area Silicon-Film™ planks into solar cells.

I. Continuous Diffusion

Prior to the PVMaT-4 program, Silicon-Film™ wafer gettering and emitter junction diffusions were performed as a batch-type process using large, 8-inch bore diffusion tubes with $POCl_3$ as the dopant source. As the area of Silicon-Film™ wafers has increased, the effort and cost required to obtain high performance junctions in a tube furnace-based system also increased. We have engineered a new continuous "rapid thermal" process and manufacturing system for diffusing N-type junctions onto large-area Silicon-Film™ wafers and planks. The width of the diffusion furnace belt is 36 inches. At a belt speed of 18 inches per minute, the throughput of this system is 1000 Silicon-Film™ wafers per hour.

II. Contact Metallization

Contact metallization printing steps are performed using commercially-available semi-automatic printers; the printers are equipped with collocators to feed 36-inch wide infrared belt furnaces. Figure 1 shows one of two screen printer-collocator-furnace systems that are used for Silicon-Film™ solar cell production.

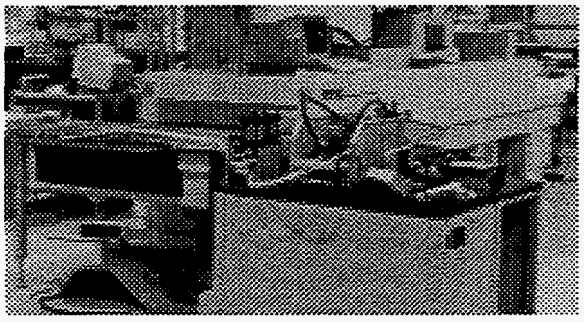

Figure 1. Silicon-Film contact metallization system. Consists of semi-automatic screen printer with 36-inch wide collocator and infrared firing belt furnace.

Based on the speed of the firing furnace belt, the potential throughput of the metallization process is more than 1500 Silicon-Film™ cells per hour. However, the actual throughput that has been realized is much lower; it is limited by the mechanisms that are used to load and unload wafers from the screen print nest, and to move wafers from the collocator belt to the furnace belt. This printing equipment is not capable of handling the large-area Silicon-Film™ planks. During the

PVMaT-5 program we will investigate alternative processes and equipment and will develop a continuous metallization printing process that matches the throughput of the firing furnaces and is capable of printing both large-area wafers and planks.

III. Large-Area AR Coating

Typical production-level AR coating systems are based on platen-type wafer heating which restricts the wafer size that can be processed and severely impacts coating uniformity, system throughput, and material usage. Waste AR coating overspray must be continuously cleaned from these systems to maintain the process.

Under the PVMaT-4 program, we investigated improved techniques to deposit uniform AR layers onto large-area Silicon-Film™ solar cells. We have combined spray pyrolysis deposition [1, 2] with infrared wafer heating and obtained dramatic improvements in throughput, spray area, material consumption and process stability.

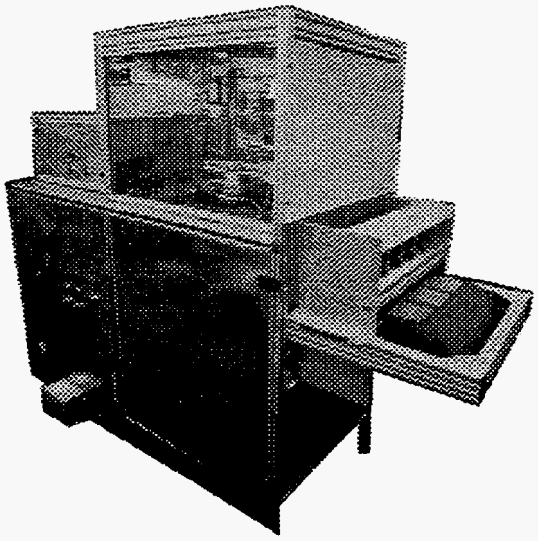

Figure 2. Continuous large-area Silicon-Film™ AR coating system.

Figure 2 shows a prototype-level infrared-heating AR coating system that is based on tubular halogen lamps. Since the wafer transport system uses an open belt it is capable of handling both large-area Silicon-Film™ cells and planks. The AR solution is deposited onto the heated wafers by a sprayhead that rasters across the belt. The infrared wafer heating system allows us to flexibly coat either wafers or planks up to 50-cm wide. This prototype coating system has a potential throughput of 900 Silicon-Film™ cells per hour.

IV. Wet Chemical Processing

Silicon solar cell wet chemical processing, such as surface damage, texturing and diffusion phosglass etches, has stubbornly remained an expensive batch-oriented sequence that severely restricts the area of the wafers that can be processed. During the PVMaT-4 program AstroPower began an investigation of in-line processes and wet chemical process equipment that will transform the standard cassette-based etch bath sequences into a continuous process that offers better control, greater safety, chemical recycle capabilities, and effluent stream reductions.

Under the PVMaT programs, we have begun to develop continuous wet chemical process sequences for diffusion phosglass etching and for hydroxide-based damage etching.

Conclusions

We have achieved significant progress in developing in-line, continuous processes and equipment to increase the manufacturing productivity of large-area Silicon-Film™ wafer cleaning, junction diffusion, contact metallization and AR coating processes. The improved processes and manufacturing equipment have been installed for Silicon-Film™ solar cell production on the new AstroPower production line that was commissioned this past Spring. Under the AstroPower PVMaT-5 program, we will develop new in-line continuous processes and production equipment for surface damage and diffusion phosglass etching, and for contact metallization to larger-area Silicon-Film™ wafers and planks.

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Effective surface and bulk defect passivation of low resistivity multi-crystalline silicon by annealed RTO/PECVD SiN Stack

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Abstract
Excellent surface and bulk defect passivation of low-resistivity p-type float zone and multi-crystalline (HEM) silicon is achieved using plasma silicon nitride (PECVD SiN) deposited on top of SiO_2 grown by rapid thermal processing. Very low effective surface recombination velocities (S_{eff}) of 8.5 cm/s and 23.4 cm/s, respectively, were obtained for float zone and the multi-crystalline silicon. The low S_{eff} is achieved after a 730°C/30 seconds anneal of the RTO/SiN stack. A corresponding bulk defect passivation of the HEM multi-crystalline material is seen with lifetime value improving from 8 μm to 35 μs. FTIR measurements show a reduction in the Si-H band concentration due to the anneal. This heat treatment enhances the release and delivery of the atomic hydrogen from the SiN film to the Si/RTO interface, thereby reducing the density of interface traps at the silicon surface. The improvement in the bulk lifetime is also attributed to the passivation of the dangling bonds or defects by the released hydrogen atoms from the SiN. This shows that HEM multi-crystalline material responds to hydrogenation without any prior gettering, which is not common for most multi-crystalline materials.

Introduction
Low surface recombination velocity (S) is a prerequisite for optimum performance of many semiconductor devices. For silicon solar cells, the recombination velocity at the front (S_f) and back surfaces (S_b) must be kept low to attain high efficiency. More importantly, the method of reducing the surface recombination velocity should be compatible with low-cost and high-throughput processing. For low-cost multi-crystalline materials, which are very good candidates for photovoltaic industry, the bulk recombination needs to be reduced. Thus a passivation scheme which can passivate both bulk and surface defects is highly desirable.

Thermally grown oxide at high temperatures of about 900 to 1100°C is generally used for good surface passivation of solar cells. However, such high temperature is known to degrade the base minority carrier lifetime in multi-crystalline materials. Silicon nitride (SiN) films deposited at low temperature by plasma enhanced vapor deposition (PECVD) have been found to provide good passivation of the low resistivity p-type Si surface [1]. In addition, the atomic hydrogen from the SiN is found to passivate bulk defects in some multi-crystalline materials. Since the application of the SiN film after front contact metallization can degrade the fill factor of silicon solar cells and ~ 1% absolute gain in efficiency is observed if applied before metallization [2], screen printed metallization is generally performed by punching through the deposited SiN. However, it is not known how PECVD SiN surface passivation responds to screen-printing firing.

The effectiveness of the PECVD SiN passivation varies greatly with deposition conditions, plasma reactor design, and post-deposition annealing. Some films show increase S after a low temperature post-deposition anneal in forming gas [3] and others [4] show an improvement in passivation quality after a similar treatment. Since the industrial solar cells undergo a moderate heat treatment for screen-

printed contacts (typically >700°C) it is necessary for any passivation scheme to be able to withstand and be compatible with this heat treatments.

The RTO (rapid thermal oxide) and PECVD SiN stack passivation has been found to be superior to any other passivation scheme used in silicon solar cell processing with an S value of about 10 cm/s on low resistivity p-type single crystal Si [5]. High temperature anneals of RTO/SiN stack (high temperatures applicable to screen printed solar cells) on 1.3 ohm-cm p-type has been shown to provide S value in the vicinity of 70 cm/s [6]. In this paper we report on the efficacy of annealed RTO/SiN stack to passivate the surface and bulk defect in HEM multi-crystalline material.

Experiment

The substrates used in this experiment include 1.3 Ω-cm., chemically polished p-type (100), FZ and 1.1 Ω-cm HEM multi-crystalline wafers. The substrates were cleaned in H_2SO_4 (1) + H_2O_2 (1) + DI H_2O (2) for 5 minutes followed by a 3 minute rinse in DI water. This was followed by a clean in HCL (1) + H_2O_2 (1) + DI H_2O (2) for 5 minutes and a 3 minute rinse in DI water. A final dip in 10% HF for 2 minutes was performed followed by 3 minutes DI water rinse. The thin oxides (100Å) were grown in RTP followed by PECVD SiN deposited at 300°C, 30-Watts power and 900 mTorr with SiH_4 and NH_3 flow of 320 and 1.55 sccm, respectively, to form the oxide/nitride stacks. After the SiN deposition samples were divided into five different groups to perform no anneal (NA), 730°C anneal (A730 A), 850°C anneal (A850 A), forming gas anneal (AFG A) at 400°C and all the three heat treatments cumulatively (AFA A).

The quality of the passivation scheme was assessed by determining surface recombination velocity (SRV) by the transient PCD technique. The effective lifetimes for samples covered with RTO/SiN were carried out for each sample before and immediately after each high temperature anneal. To measure the bulk lifetimes in each group, the RTO/SiN stack was removed in 20% HF and the samples were placed in 0.001M of I_2 (placed in sandwich zip lock bag) for the measurements.

The effective lifetime of the minority carriers (for FZ silicon) was converted to effective surface recombination velocity (S_{eff}) according to [7]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + D\beta^2 \qquad (1)$$

$$\tau_s = \frac{1}{\beta^2 D_n} = \left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_b}\right)^{-1} \qquad (2)$$

$$S_{eff} = \beta D_n \tan\left(\frac{\beta W}{2}\right) \qquad (3)$$

where τ_{eff} is the measured effective minority carrier lifetime, τ_s is the surface lifetime, τ_b is the measured bulk minority carrier lifetime, S_{eff} is the effective surface recombination velocity, D_n is the

electron diffusion constant and W is the wafer thickness. Since FZ wafers had bulk lifetime (τ_b) in excess of milliseconds, the value of S_{eff} in this study was determined by $\frac{1}{\tau_{eff}} = \frac{2S}{W}$, which is valid for very high or infinite carrier lifetime and good SRV. Thus S_{eff} values of FZ represent maximum or worse case scenario.

For the multi-crystalline silicon, since the bulk lifetime is not so high, the measured values of τ_{eff} and τ_b (measured in 0.001M iodine solution) are used in equation (2) to first determine τ_s which is then used to determine β and finally S_{eff} is determined from equation (3). All the effective and bulk minority carrier lifetimes were measured in the low level injection regime between $2e^{14}$ and $1e^{15}$.

Results and Discussion

Figure 1 shows the comparison of the effective surface passivation of low resistivity FZ and HEM multi-crystalline silicon. FZ substrate shows poorest surface passivation (S_{eff} = 394 cm/s) after the stack deposition without any anneal. After 730°C and 850°C anneals alone, the S_{eff} values decrease to 8.5 and 25 cm/s, respectively. After the three cumulative heat treatments (applicable to screen printed solar cell processing) the S_{eff} value of 56 cm/s is obtained, which is a very good value for a finished solar cell. The RTO/SiN stack surface passivation is most effective after the 730°C anneal for 30 seconds. This is believed to be due to the release and delivery of atomic hydrogen from the SiN to the Si/RTO interface, thereby reducing the density of interface traps at the silicon surface. Also, because the time is so short, only 30 seconds, the hydrogen atoms delivered to the interface of Si/SiO_2 are not driven out as suggested by the higher S_{eff} value for the 850°C anneal which is done for 2 minutes. The FGA anneal alone for 20 minutes at 400°C results in equally low S_{eff} because this temperature is not high enough to drive out the atomic hydrogen.

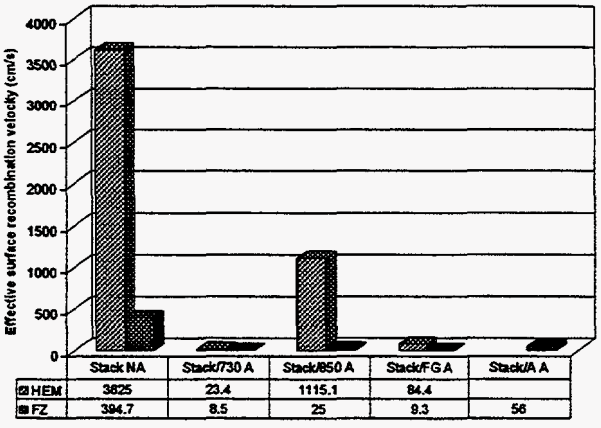

Fig.1: Effective surface passivation of low resistivity FZ and multi-crystalline silicon.

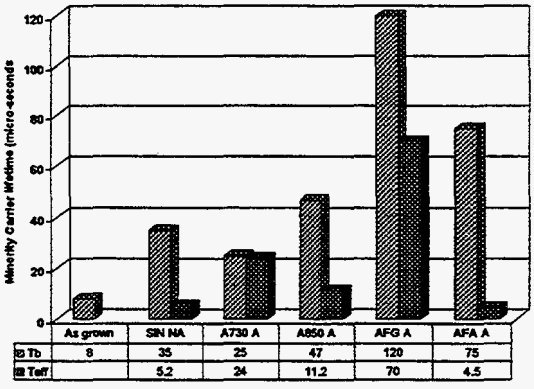

Fig.2: Effective surface and bulk defect passivation of multi-crystalline silicon by annealed RTO/SiN stack.

The surface passivation of the multi-crystalline silicon was also found to be poor (S_{eff} =3600 cm/s) directly after the RTO/SiN formation. However, after the 730°C anneal, S_{eff} reduced by a factor of 156 to a value of 23 cm/s. The passivation quality of the RTO/SiN stack deteriorated (S_{eff} = 1115 cm/s) after 850°C anneal. This high S_{eff} value may be attributed to the portion of the substrate used in this study or a more intense anneal could drive hydrogen faster through the grain boundaries into the bulk leaving the Si/RTO interface unpassivated. The passivation quality of the RTO/SiN after FGA for 20 minutes is quite good (S_{eff} = 84 cm/s). Again, longer time in hydrogen ambient helps in better

passivation of the Si/RTO interface. Unlike the single crystal Si, the passivation quality of the stack after all three anneals was quite low (S_{eff} = 5600 cm/s). This may be attributed to damage to the sample surface rather than a general trend. More work is underway to prove this point.

The bulk defect passivation of HEM multi-crystalline silicon by annealed RTO/SiN stack is shown in Figure 2. The bulk lifetime is found to improve from the as-grown value of 8 μs to 35 μs immediately after the stack formation. The as-grown lifetime increased to 25 and 47 μs after 730°C/30 seconds and 850°C/2 minutes, respectively. The highest improvement was recorded after annealing the sample (Si/RTO/SiN) in forming gas for 20 minutes at 400°C. After all the three anneals a lifetime of 75 μs was obtained, which is quite respectable for achieving high efficiency cells. In each case, the improvement in bulk lifetime is attributed to the defect passivation by atomic hydrogen released from the SiN during deposition and other high temperature anneals. It should be noted that the difference in the minority carrier lifetimes measured on different pieces after different anneals could be due to some inhomogeneity in multi-crystalline silicon pieces. The multi-crystalline used in this experiment did not undergo any prior gettering to remove the impurities that might be present in the bulk.

Conclusion

The annealed RTO/SiN stack is very effective for the passivation of both single and multi-crystalline silicon surfaces. The passivation quality of the stack is significantly enhanced when annealed at elevated temperature (~750°C) for a short time (30 seconds). This results in Seff of 8 cm/s and 23 cm/s on FZ and HEM surfaces, respectively. The forming gas anneal of the RTO/SiN stack also gives very low surface recombination velocity (9 cm/s for FZ and 84 cm/s for HEM). The release and delivery of the hydrogen from the SiN to the Si/RTO interface, reduces the density of interface traps at the silicon surface. The bulk passivation of the HEM multi-crystalline silicon by annealed RTO/SiN stack resulted in bulk minority carrier lifetime of 75-120 μs. The atomic hydrogen released from the SiN reaches the bulk via defects such as dislocations and grain boundaries, passivating the dangling bonds or lifetime limiting traps. The multi-crystalline material used in this work did not undergo any form of gettering before the passivation, yet very high lifetimes were attained in HEM material. This may not be true for all the multi-crystalline materials.

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A RAPID THERMAL OXIDE/PECVD SILICON NITRIDE STACK FOR EFFECTIVE PASSIVATION OF LOW RESISTIVITY SILICON AND PHOSPHORUS DIFFUSED EMITTERS

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Abstract

A novel stack passivation scheme, in which plasma silicon nitride (SiN) is stacked on top of a rapid thermal SiO_2 (RTO) layer, is developed to attain a surface recombination velocity (S) approaching 10 cm/s at the 1.3 Ω-cm p-type (100) silicon surface. Such low S is achieved by the stack even when the RTO and SiN films *individually* yield considerably poorer surface passivation. Critical to achieving low S by the stack is the use of a short, moderate temperature anneal (in this study 730°C for 30 seconds) after film growth and deposition. This anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO_2 interface, thereby reducing the density of interface traps at the surface. Compatibility with this post-deposition anneal makes the stack passivation scheme attractive for cost-effective solar cell production since a similar anneal is required to fire screen-printed contacts. Stack passivation also reduces the J_{oe} of 40 Ω/sq and 90 Ω/sq phosphorus diffused emitters by factors of 3 and 10, respectively, compared to conventional single layer passivation schemes. Application of the stack to *passivated rear* screen-printed solar cells has resulted in V_{oc}'s of 641 mV and 633 mV on 0.65 Ω-cm and 1.3 Ω-cm FZ Si substrates, respectively. These V_{oc} values are roughly 20 mV higher than for cells with untreated, highly recombinative back surfaces. The stack passivation has also been used to form fully screen-printed *bifacial* solar cells which exhibit rear-illuminated efficiency as high as 11.6% with a single layer AR coating.

1. Introduction

The front and back surface recombination velocities (S_f and S_b) are key loss components in Si solar cells. One way to reduce S_b is to implement an Al-BSF in the device design [1]. This structure is effective, but the stresses imparted to the Si substrate during Al-BSF formation can preclude application to thin wafers. Process-induced stress can be virtually eliminated by employing a *passivated rear* structure (Fig. 1) in which the rear side metallization covers only a small fraction of the surface area. In addition to reducing process-induced stress, this structure is well suited for bifacial operation since the rear surface is transparent to incoming light. However, in order to take advantage of this structural feature and attain a significant power output, the passivation at the rear surface must by effective.

In this paper, we report the use of a dielectric stack comprised of a rapid thermal SiO_2 (RTO) and a plasma silicon nitride (SiN) for effective passivation of the low resistivity (0.65-1.3 Ω-cm) p-type (100) Si surface as well as phosphorus diffused emitter regions (40 and 90 Ω/sq). These films are attractive from the standpoint of low-cost production since both can be applied in short times.

The essential feature of the stack passivation scheme is its ability to withstand moderate temperature annealing (700-800°C) without any degradation in S. In fact, the stack *relies* on such thermal treatment to achieve low S values. This novel method is used to fabricate passivated rear and bifacial screen printed solar cells. The finished devices are characterized so that the impact of the fractional metal coverage on S_b can be deduced. Model calculations are performed to demonstrate that the stack can be successfully applied to thin substrates without sacrificing performance.

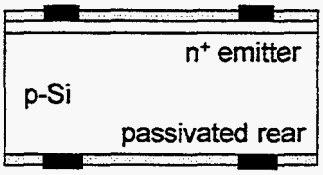

Fig. 1. Passivated rear and bifacial solar cell.

2. Quantitative Assessment of Low Resistivity Si Surface Passivation by the RTO/SiN Stack

The passivation quality of SiN, RTO, and an RTO/SiN stack were compared. The substrate materials used were 0.65 and 1.3 Ω-cm FZ Si. The surfaces were chemically polished, *not* mirror polished. All SiN films were deposited in a direct, high-frequency (13.5 MHz), parallel-plate reactor at 300°C. The RTOs were grown in a rapid thermal processing (RTP) unit at 900°C in 2 minutes. Ensuing thermal treatments (simulating contact firing) were carried out in a three-zone beltline furnace in which the "hotzone" temperature and time were fixed at 730°C and 30 sec. The passivation quality of each scheme was monitored by the transient photoconductance decay (PCD) technique. The effective lifetimes measured by PCD were converted to S values using a conventional analysis method [2]. In this paper, all S values are calculated assuming an infinite minority carrier lifetime in the substrate. The resulting S values are therefore maximum or "worst-case" limits.

The passivation quality of an RTO *alone* is shown in Fig. 2 for a growth temperature of 900°C. The as-grown oxide results in S higher than 10,000 cm/s which can be reduced to approximately 100 cm/s by a forming gas anneal (FGA) treatment at 400°C. However, the ensuing 730°C beltline anneal degrades the interface quality and increases S above 3000 cm/s.

A similar trend is observed here for the SiN film *alone* (also Fig. 2). The as-deposited SiN results in S greater than 10,000 cm/s which can be reduced to approximately 200 cm/s by an ensuing anneal in forming gas at 400°C. Again, the 730°C beltline treatment degrades the interface quality and increases S by approximately one order of magnitude.

Clearly, these two treatments (RTO alone or PECVD SiN alone) are not compatible with screen-printing requirements since neither can withstand a contact firing cycle without a significant increase in S. On the contrary, annealing the RTO/SiN stack actually *enhances* the passivation quality. The stepwise effect of stacking PECVD SiN on top of the RTO layer and then annealing at 730°C is shown in Fig. 3. The S value attained after the final beltline anneal (Step 3) is clearly superior to RTO growth (Step 1) or SiN deposition on top of the oxide layer (Step 2). The 730°C anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO_2 interface, thus reducing the density of states at the surface. *Maximum* S values of 11 cm/s and 20 cm/s are achieved by the stack passivation at the 1.3 Ω-cm and 0.65 Ω-cm p-type surfaces, respectively. These are among the lowest S values ever reported for solid film passivation of the low-resistivity Si surface.

Also evident in Fig. 3 is the weak injection level dependence of S within the measurement range (10^{14}-10^{15} cm^{-3}). This behavior is quite different than that reported for the highest quality remote SiN films where S increases by a factor of 5 as the injection level falls from 10^{15} to 10^{14} cm^{-3} [3].

The initial RTO growth temperature is observed to have an effect on the final S value of the annealed stack. For an 850°C RTO growth, final S values of ≈ 40 cm/s are achieved on 1.3 Ω-cm Si after the 730°C beltline anneal. This a approximately a factor 3 higher than for the 900°C RTO growth.

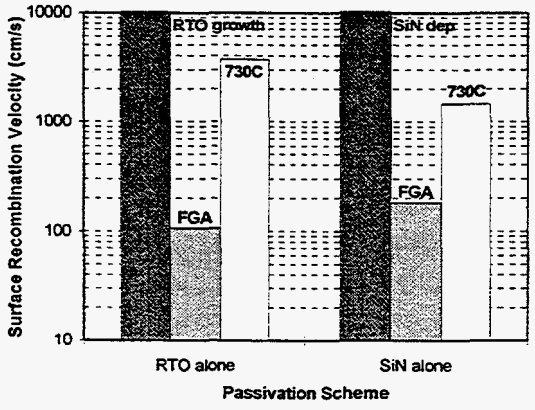

Fig. 2. Passivation by SiN and RTO films individually. The FGA treatment was 400°C in 30 min. The S values were measured at the 1.3 Ω-cm surface.

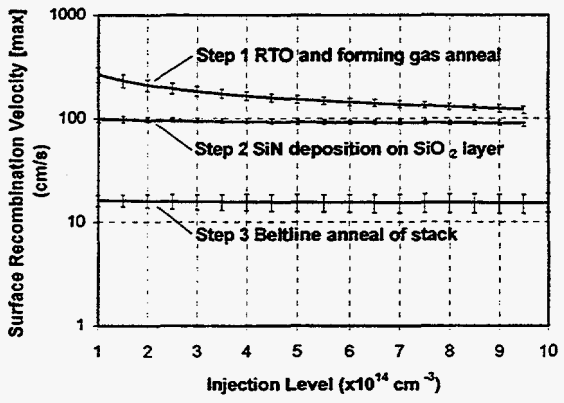

Fig. 3. Progression of S values for stack passivation of 1.3 Ω-cm Si.

3. A Comparison of Various Back Surface Passivation Schemes on Flat and Textured Surfaces

Different passivation schemes for the Si surface were analyzed and compared (Fig. 4). These included TiO_2 alone, RTO alone, *direct* plasma SiN alone (SiN_1 and SiN_2), *remote* plasma SiN alone (SiN_3), and RTO/SiN stacks. On 1.3-Ωcm *p*-Si wafers, the deposition of TiO_2 does not give any measurable surface passivation, nor does the growth of RTO alone or the deposition of SiN_1 alone. However, both the SiN_1 and RTO passivations improve considerably after an FGA. While as-deposited SiN_3 already gives very good passivation (27 cm/s on planar surfaces), double layers of RTO with all nitrides result in excellent S_{eff} values after an FGA. The same trend is found for textured surfaces (Fig. 5), with SiN_3 giving much better passivation than the other nitrides. After an FGA, all RTO/SiN double layers show good passivation, resulting in a low $S_{eff,max}$ value of 39 cm/s for RTO/SiN_3.

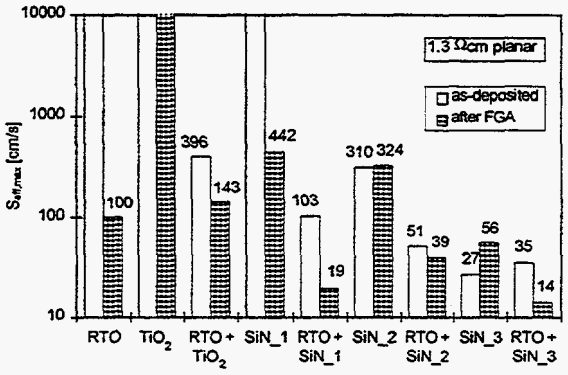

Fig. 4. Measured maximal S_{eff} values of different passivation schemes on *planar* 1.3-Ωcm *p*-Si wafers.

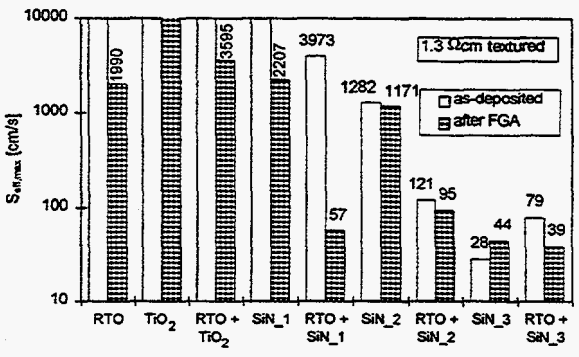

Fig. 5. Measured maximal S_{eff} values of different passivation schemes on *planar* 1.3-Ωcm *p*-Si wafers.

4. Passivation of Screen-Printable Emitters

The passivation of solar cell front surfaces was investigated on both 40 Ω/□ and 90 Ω/□ emitters. On 40 Ω/□ emitters (which can accommodate screen-printed contacts) the surface is largely decoupled from the bulk, because of the high surface dopant concentration and the large depth of the doping profile. Despite this, high-quality RTO or remote SiN_3 passivation was able to reduce J_{0e} by a factor of 2 – 3 compared with TiO_2, which offered virtually no measure of passivation (Fig. 6). Direct SiN_1 (deposited at 300°C) is clearly inferior to RTO or remote SiN_3. The stack combination of RTO and SiN_3 results in the best emitter passivation (174 fA/cm² on planar samples). Note that the high-temperature RTO treatment slightly changes the doping profile (reduced surface dopant concentration, increased emitter thickness), facilitating the achievement of a good surface passivation. The J_{0e} values of textured samples are about 1.5 to 2 times higher than those of planar ones, which resembles the increase in surface area.

5. Passivation of 90 Ω/□ Emitters

On relatively transparent 90 Ω/□ emitters, the difference in the degree of passivation for various schemes is more pronounced, as Fig. 7 shows. Again, TiO_2 does not provide any significant reduction of J_{0e}. For the planar surface, RTO growth reduces J_{0e} by more than a factor of 10 to below 100 fA/cm², as does the deposition of remote SiN_3. However, on the textured surface RTO alone is not as effective, resulting in a moderate J_{0e} value of 400 fA/cm². Here, the remote SiN_3 is clearly superior.

Stack combinations of RTO and SiN were better than the nitrides alone in all cases, resulting in very low J_{0e} values of less than 50 fA/cm² for planar and 100 fA/cm² for textured emitter surfaces (Fig. 7). A 400°C forming gas anneal does not change the surface passivation appreciably. The same applies for the contact firing cycle on the 40 Ω/□ emitters. For comparison, thin furnace oxides (CFOs) were grown on the same emitters. This passivation resulted in identical or only negligibly lower J_{0e} values than the RTO.

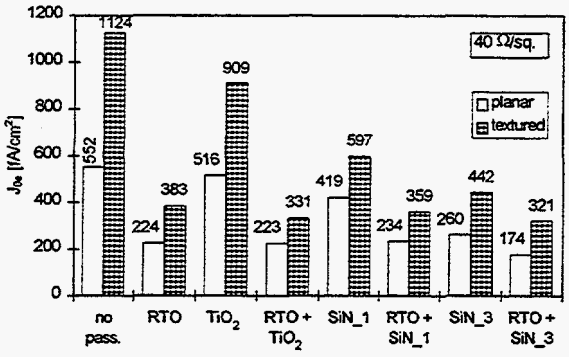

Fig. 6. Measured emitter saturation current densities of different passivation schemes on 40 Ω/□ emitters.

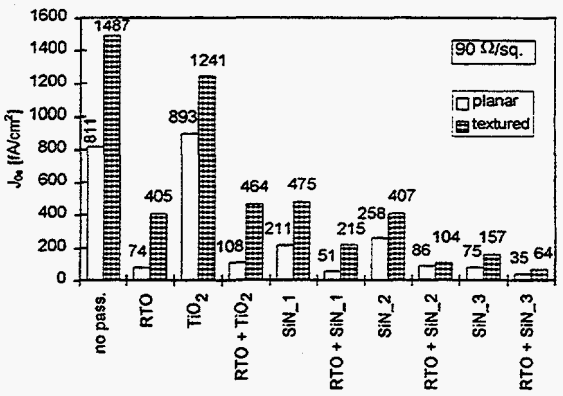

Fig. 7. Measured emitter saturation current densities of different passivation schemes on 90 Ω/□ emitters.

6. Solar Cell Formation

Passivated rear solar cells shown in Fig. 1 were fabricated on 0.65 Ω-cm and 1.2 Ω-cm FZ Si as well as 0.8 Ω-cm CZ grown by Siemens Corporation. A simple cell process (n^+ diffusion, RTO growth, SiN deposition, 2-sided screen-printing, and contact firing) was implemented. The gridline spacing of both front and rear contacts was maintained at 2.5 mm. The results of the fabrication are shown in Table 1. For comparison, the performance of cells which lack an effective back surface treatment are also listed. In all cases, the Voc's for the passivated rear cells are significantly higher than for those formed with highly recombinative back contacts. This clearly demonstrates the ability of the stack passivation to lower Sb.

Bifacial solar cells were also formed on the 0.65 Ω-cm FZ Si. The SiN used for the stack passivation served as AR coating to both sides. The results of this initial fabrication are shown in Table 2. To date, this rear efficiency of 11.6% is the highest reported for a fully screen-printed n^+p bifacial solar cell. The ratio of the *rear-J_{sc}* to *front-J_{sc}* is 0.75.

Table 1. Passivated rear screen-printed solar cell performance. The PV grade CZ material was grown by Siemens Corporation.

Material	Rear Surface	V_{oc} (mV)	J_{sc} (mA/cm²)	FF	Eff (%)
FZ 0.65	Passivated	641	33.3	0.776	16.6
Ω-cm	No Pass	621	32.8	0.785	16.0
FZ 1.3	Passivated	631	33.8	0.770	16.5
Ω-cm	No Pass	609	32.8	0.786	15.7
CZ 0.8	Passivated	622	32.0	0.776	15.5
Ω-cm	No Pass	611	31.0	0.782	14.8

Table 2. Bifacial solar cell performance (verified by Sandia National Labs).

Illum. Side	V_{oc} (mV)	J_{sc} (mA/cm²)	FF	Eff (%)
Front	640	33.7	0.761	16.4
Rear	624	25.1	0.743	11.6

7. Conclusions

A novel stack passivation scheme (consisting of RTO and SiN) has been developed which can attain S values approaching 10 cm/s at the 1.3 Ω-cm Si surface as well as low J_{oe} values of 174 fA/cm² and 35 fA/cm² for 40 Ω/□ and 90 Ω/□ phosphorus diffused emitters, respectively. The stack has been applied to rear passivated and bifacial screen-printed solar cells. Front and rear illuminated efficiencies of 16.6% and 11.6%, respectively, have been demonstrated on 0.65 Ω-cm Si. Device S_b values of 340 cm/s were measured for cells with 8.3% rear metallization coverage. It is clear that higher performance could be attained if a more precise (less coverage) contact scheme were devised.

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Approach Towards High Efficiency, Manufacturable Thin String Ribbon Silicon Solar Cells

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Abstract

The effect of impurity gettering and defect passivation by hydrogenation was examined on 100 μm thick string ribbon silicon material. The bulk lifetime of the material increased from an as-grown value of 1 μs to 9 μs after cell fabrication, which involved phosphorous and aluminum gettering and a forming gas anneal (FGA). Without the gettering treatments, FGA had little effect on the bulk lifetime. Solar cells were fabricated with photolithography contacts as well as screen printed contacts. Cells processed with conventional furnace processing and photolithography contacts had an average efficiency of 14.6% with a maximum of 15.4%. The average efficiency of cells annealed in forming gas was 1.2% (absolute) higher than those annealed without forming gas. The first 100 μm thick fully screen printed cell with a beltline diffused emitter (BLP) of 45 Ω/□ produced efficiencies as high as 10.9%. A comparison of the internal quantum efficiency of the cells fabricated with conventional furnace processing (CFP/PL) and beltline/screen-print processing cell shows that the main difference is in the short wavelength response. This difference is attributed to the poorer surface passivation and the lower sheet resistance emitter of the screen printed cell. Device modeling is performed to illustrate the importance of good back surface passivation for a 100 μm thick cell with a bulk lifetime of 10 μs. Cell analysis estimates an S_{back} of > 5000 cm/s, while the desired S_{back} should be less than 200 cm/s. An RTO/SiN stack passivation, that gives an S_{back} of less than 100 cm/s, has been developed to passivate the back surface, which should give higher efficiency screen printed thin string ribbon cells.

Introduction

String Ribbon is a vertical growth technique of polycrystalline silicon in which two high temperature strings are passed through a crucible of molten silicon[1]. Currently, commercial solar cells are made on ribbons that are 250 μm thick in a continuous production facility. By controlling the thermal stresses generated during growth, 100 μm thick string ribbon has been grown[1]. The bulk lifetime of the material before cell processing has been measured to be less than 1 μs. However, cell efficiencies of over 15%[1] from conventional furnace processing demonstrate that the material is responding to gettering and passivation treatments. To maintain the cost-effectiveness of string ribbon, the processing steps in the cell fabrication sequence must be low-cost. Integration of high efficiency features such as PECVD SiN coatings, screen printed Al-BSFs, selective emitters, and light trapping in an industrial fabrication line could produce higher efficiency cells.

In this work, the effect of hydrogen passivation of string ribbon before and after phosphorous and aluminum gettering is investigated. Photolithography cells with gettering and passivation are fabricated to achieve high efficiency 100 μm thick string ribbon cells. Commercially viable cells with a BLP emitter, PECVD front and back passivation and screen printed contacts are also fabricated on 100 μm thick string ribbon. Finally, model calculations are performed to provide guidelines for achieving higher efficiency screen printed string ribbon solar cells.

Experimental

i. String Ribbon Cells with Conventional Furnace Processing and Photolithography Contacts

The substrates used in this experiment were p-type 1.5 Ω-cm 100 μm string ribbon silicon. Emitters were formed by a conventional 80 Ω/□ $POCl_3$ diffusion at 845°C (CFP). After phos-glass removal, 2 μm of Al was evaporated to the back surface of all samples. Al-BSF formation and CFO growth in the conventional furnace was performed at 850°C for 10 minutes in an O_2 ambient and for 25 minutes in a N_2 ambient. Selected samples were then ramped down to 400°C and annealed for 2 hours in forming gas while others were ramped to 400°C and annealed in N_2 for 2 hours. The back contact was formed by the evaporation of Al-Ti-Pd-Ag and front contact metallization was formed by photolithography and the evaporation of Ti-Pd-Ag. Cells were isolated, silver plated, and a double layer anti-reflection coating composed of ZnS-MgF_2 was deposited.

ii. String Ribbon Cells with Beltline Furnace Processing and Screen Printed Contacts

The substrates used in this fabrication run were 100 μm thick 1.5 Ω-cm p-type string ribbon Si. Emitter diffusion of 45-50 Ω/□ was performed in a beltline furnace at 875°C for a dwell time of 36 min. Following diffusion and phos-glass removal, a single layer SiN film was deposited on the front and back surface in a parallel plate RF powered PECVD reactor. Gridded back contacts and Al-BSF were formed by screen printing Al paste and fired in the beltline furnace at a temperature of 850°C for two minutes. Front contacts were formed by screen printing Ag paste and fired in the beltline furnace at a peak setpoint temperature of 730°C for 30 seconds. Cells were annealed in forming gas for 20 minutes and isolated with a dicing saw. Al was evaporated on the back of the cells to connect the back grid for the I-V measurement.

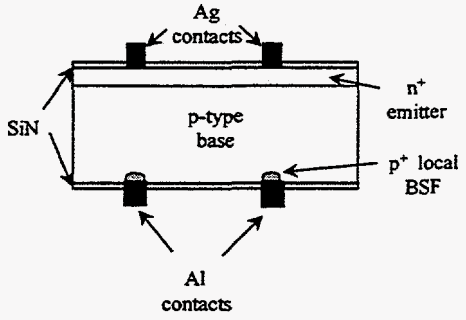


Figure 1: Structure of Screen Printed Gridded Back Contact Cell

Results & Discussion

i. Effect of Gettering and Hydrogen Passivation on String Ribbon

The as-grown lifetime in string ribbon measured by photoconductance decay (PCD) was 1 μs. Photolithography cells were fabricated to study the effect of gettering and passivation on string ribbon. Table 1 indicates that the 2 hour FGA in the oxide growth/BSF formation step improves both the J_{sc} and V_{oc} accounting for the 1.2% (absolute) gain in the average efficiency. Note that before FGA, cells have undergone phosphorous and aluminum gettering. In order to quantify the effects of gettering and passivation on the bulk lifetime, a sample was stripped of contacts and diffusions after light IV measurement and a bulk lifetime of 9 μs was measured by PCD. PCD measurements before and after the FGA on the as grown string ribbon gave a bulk lifetime of only 1 μs, indicating that hydrogenation without any gettering is not effective in improving the performance of string ribbon. However, a combination of gettering and passivation can raise the lifetime to 9 μs, which makes L/W > 1 for a

100 μm thick material. Table 1 shows that gettering alone is not sufficient because the cells without FGA gave an average efficiency of 13.4 %. Unlike the as-grown material, the solar cell data reveals that FGA is quite effective after gettering. It is noteworthy that the combination of gettering and passivation resulted in an average cell efficiency of 14.6 % with a maximum of 15.4 % using photolithography contacts and a 80 Ω/□ emitter.

Table 1: Light IV Data of Photolithography Cells

Process		*Average of Cells*				*Best Cell*			
	Area	J_{sc} mA/cm²	V_{oc} mV	FF	Eff %	J_{sc} mA/cm²	V_{oc} mV	FF	Eff %
CFP/CFO FGA	1 cm²	32.92	580	0.763	14.6	33.61	589	0.778	15.4
CFP/CFO (no FGA)	1 cm²	31.39	570	0.749	13.4	31.57	577	0.780	14.1

ii. Beltline Furnace/Screen Printed Manufacturable Cells on 100 μm String Ribbon

Because photolithography and long furnace processing is not cost effective, in this section an attempt was made to fabricate high efficiency, manufacturable 100 μm thick string ribbon cells using PECVD SiN passivation, screen printed contacts and a beltline diffusion. Fabrication of the screen printed 100 μm thick solar cells has so far proven to be very challenging. Fabrication procedures are being developed that should improve the yield of fabrication runs. This paper presents only preliminary results of screen printed thin string ribbon solar cells. An encouraging efficeincy of 10.9 %, confirmed by Sandia National Labs, has been achieved which will serve as a starting point for the development of manufacturable thin string ribbon cells.

Model calculations in Fig. 2 illustrate the dependence of cell efficiency on the back surface recombination velocity for a 10 μs bulk lifetime. The efficiencies are calculated assuming a good fill factor and a screen-printing type emitter diffusion profile. For all values of S_{back} less than 2,000 cm/s, a 100 μm thick material has a higher efficiency than the 250 μm thick material. The difference in efficiency between the thick and thin cells increases with decreasing S_{back} until S_{back} reaches 100 cm/s. Our analysis of a 2 μm evaporated Al-BSF on a float zone cell showed an S_{back} of > 5000 cm/s. Therefore, the S_{back} of the photolithography cell is quite poor and is estimated at > 5000 cm/s. At this level of S_{back}, Fig. 2 indicates that a thin cell will have a lower efficiency than a thick cell.

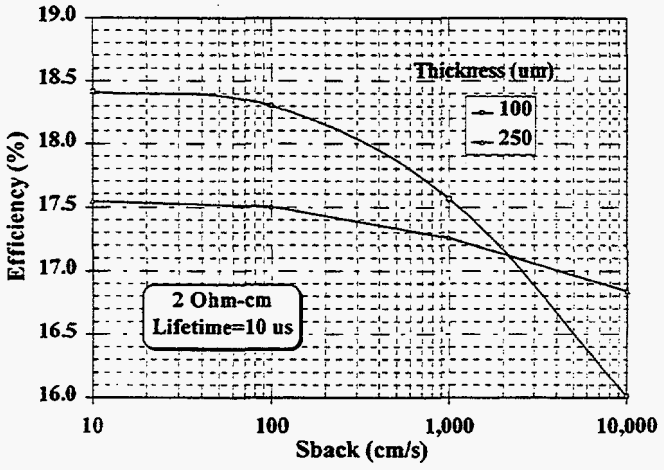
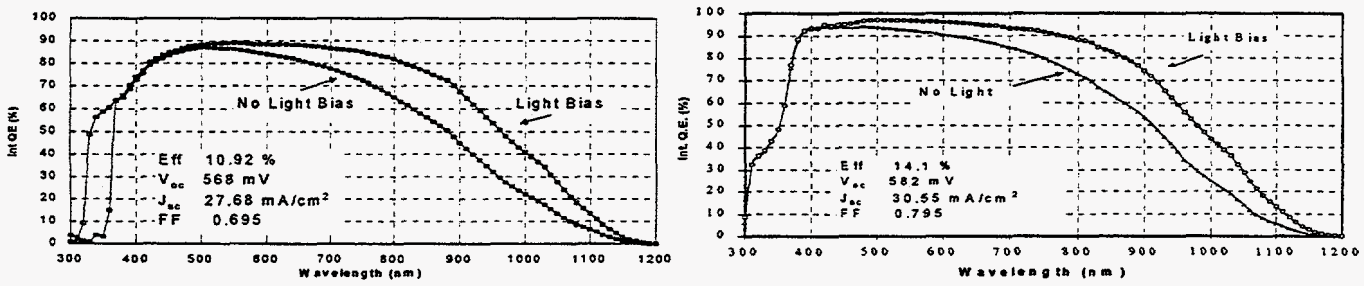


Figure 2 Effect of BSRV and thickness on cell efficiency for 10 ms bulk lifetime

Fig. 3 compares the IQEs of the a beltline/screen printed cell and the high efficiency conventional furnace processed cell. The higher short wavelength response of the high efficiency cell is attributed to a high sheet rho emitter (80 Ω/□ emitter) and good front surface oxide passivation. The screen printed cell requires a 45 Ω/ emitter and relies on a lower quality, high throughput PECVD SiN for front surface passivation and anti-reflective coating. The long wavelength IQEs (900-1150 nm) of the cells are closely matched indicating that the combination of bulk lifetime and back surface passivation may be the same for both cells. A bulk lifetime of over 9 μs after BLP emitter formation supports that the S_{back} for the screen printed cell is similar to that of the photolithography cell, namely 5000 cm/s. The reported efficiency of 10.9% is lower than expected and is believed to be a result of a poor fill factor and poor back surface passivation. The poor passivation is attributed to a degradation in SiN surface passivation as a result of the screen printing firing cycle. We have found that an as deposited SiN film has a very high S_{back}. Even after screen printing heat treatments, S_{back} due to PECVD SiN remains > 1000 cm/s, which is too high for thin cells. We have recently developed a rapid thermal oxide (RTO)/SiN stack passivation scheme that has resulted in an S_{back} of < 100 cm/s after screen print firing. Application of this stack on the front and back surface should provide significant enhancement in cell efficiency in the future.



a) **b)**

Figure 3: IV and Light biased IQE measured by Sandia National Labs of cell fabricated by a) beltline furnace/screen printing and b) high efficiency furnace processing/photolithography

Conclusions

Defect passivation by FGA was effective in increasing the efficiency of CFP/PL cells by an average of 1.2% absolute. The as grown bulk lifetime of 1 μs in the string ribbon increased to 9 μs as a result of phosphorous and aluminum gettering and hydrogen passivation. Hydrogen pssivation without gettering did not have an appreciable effect on the bulk lifetime of string ribbon. Emitter formation by BLP, combined with PECVD SiN and screen printed contacts was used to fabricate manufacturable cells with efficiencies as high as 10.9% on 100 μm thick string ribbon. A comparison of the IQEs of a CFP/PL cell and a screen-printed cell indicate that the difference lies in emitter sheet resistance and surface passivation. In addition, both photolithography and screen printed cells suffer from poor back surface passivation. Future work will include the use of selective emitters, improved surface passivation by an RTO/SiN stack, and optimization of gettering and passivation of thin string ribbon for achieving high efficiency, manufacturable cells.

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EVOLUTION OF DEFECT ELECTRICAL ACTIVITY IN SILICON WAFERS DURING PROCESSING STEPS BY LBIC SCAN MAPS AT 80 K.

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Multicrystalline silicon (mc-Si) wafers are characterized by the presence of large densities of intergrain and intragrain defects, mainly dislocations. These defects become highly recombining for minority carriers when they have segregated impurities (oxygen ; metals). However defects and impurities are sometimes electrically inactive at room temperature but can be activated by annealing treatments. Such treatments which must be carried out at relatively high temperature, are needed to transform the wafers in solar cells and it was verified that (frequently) the annealings have by themselves a degrading effect [1].

It is known that electron beam induced current (EBIC) contrast of dislocations varies with temperature T, increasing when T decreases if the contrast is initially low at room temperature (RT) [2 ; 3]. This is explained by the Shockley-Read-Hall statistics, when shallow levels govern the lifetime τ of minority carriers. Conversely, when deep levels control τ, the contrast is marked at RT, and decreases with T. EBIC could be used to detect at low temperatures all the defects present in the material, which have a poor effect at RT due to their low recombination strength. However such a technique investigates only few micrometers below the surface of the material. Light beam induced current scan maps (LBIC) can be advantageously used, because near infrared light i s absorbed deeply in the bulk.

The present paper deals with the prediction of the behaviour of conventionally casted or electromagnetically casted mc-Si wafers during annealings at temperatures higher than 700°C

P type mc-Si samples were cut from polix wafers made by Photowatt Int. S.A. France, and from electromagnetically casted (EMC) silicon wafers prepared by Sumitomo Sitix or by EPM Madylam-France [4 ; 5]. LBIC scan maps at 900 nm and minority carrier diffusion length scan maps are used to detect the presence of recombining defects and to evaluate their recombination strength. LBIC maps are also obtained at 80 K thanks to an Oxford Instruments microcryostat. Raw samples are investigated after they have been transformed in MIS diodes, with a semitransparent metallic layer. Then the MIS diode is removed by chemical etching and the sample is annealed at temperature of 800°C to 900°C for 20 mn to 1 h, in order to simulate the formation of p-n junctions by phosphorus diffusion or/and a gettering treatment.

It is found that the LBIC contrast increases lightly in polix wafers, and consequently the diffusion length (L) decreases lightly, after the annealings. It decreases neatly at 80 K in the main part of the wafers. Conversely, in EMC samples, the contrast is poor at RT, and increases strongly at 80 K.

After annealing, the contrast increases strongly and the LBIC maps reveal the same features which appears initially at 80 K. As a consequence L is neatly smaller after annealing : $L \equiv 60$ µm after annealing at 850°C for 30 mn instead of 130 µm in the raw sample. Figures 1 and 2 illustrates these results.

These evolutions indicate that in conventionally casted mc-Si, the lifetime of minority carriers is governed by deep levels due to metallic impurities, while in raw EMC wafers the lifetime is determined by shallow levels. However these shallow levels are rapidly transformed in deep levels, during the thermal treatments.

The comparison of the LBIC scan maps at RT and at 80 K is able to predict the behaviour of the material :

- If the contrast is approximately the same, the material can support the processing steps without a noticeable degradation,
- If the contrast is poor at RT and increases at 80 K, the material will be degraded during the processing steps.

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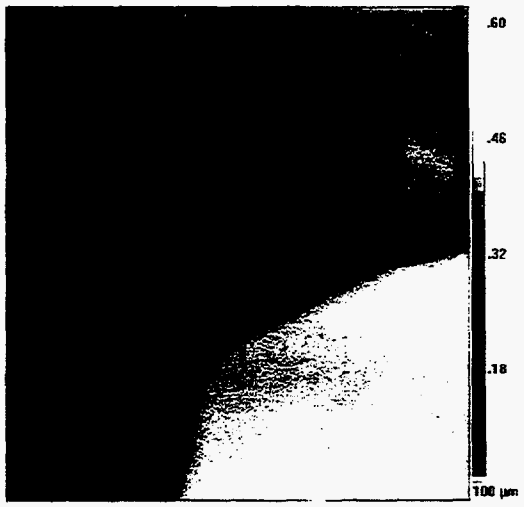
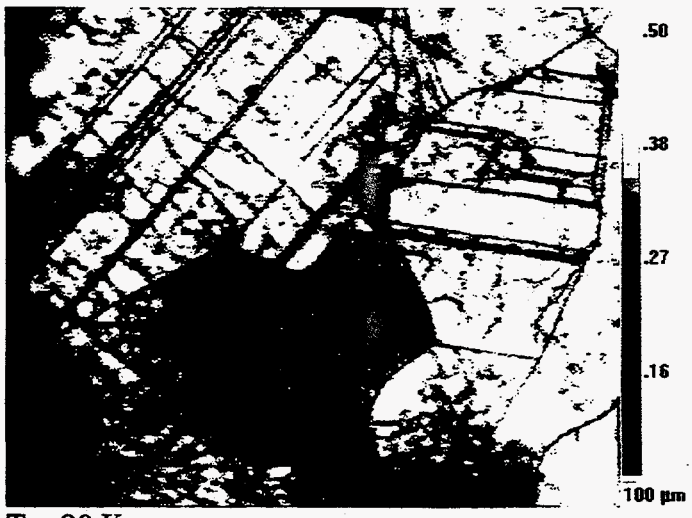


T = 300 K

T = 80 K

Fig.1 LBIC scan map at 900 nm of a Polix sample showing two different regions :
In the right part the contrast of defects decreases when T decreases : this region is not degraded by thermal treatments.
In the left part the contrast increases at 80 K : this region will be degraded by thermal treatments at T ≥ 700°C.

T = 300 K



T = 80 K

Fig.2 LBIC scan map of a sitix sample : the contrast of defects increases markedly when T decreases from room temperature to 80 K. This sample will be degraded by thermal treatments at T ≥ 700°C, and the same features of intragrain defects are observed at 80 K as well as after annealing.

Using *PV Optics* for solar cell and Module design

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Introduction

High-efficiency solar cells and modules involve a number of features that are difficult to handle by simple optics. Hence, a dedicated optical design package is required that can address various device features that are important for the design and analysis of solar cells; they are (i) nonplanar interfaces such as those required for optimizing light-trapping; (ii) thick devices such as crystalline silicon solar cells as well as thin cells based on a-Si, CdTe, and CIS; (iii) antireflection and dielectric coatings; (iv) metallic absorption arising from contacts and back reflectors; and (v) thicker materials such as glass and encapsulants used in modules. We have developed a software package — *PVOptics* — suitable for accurate design and analysis of any solar cell or modules.

PV Optics is an easy-to-use software that accurately models the optics of any solar cell or module, and provides information needed to design a device with maximum light-trapping and optimum photocurrent. *PV Optics*' sophisticated model uses the coherence length of light as a criterion to categorize various regions of a cell as "thin" or "thick" — the former have thicknesses less than the coherence length of light and include interference and polarization effects; the latter are much thicker than the coherence length and are treated on the basis of ray optics. The model separates a multilayer structure into several composite layers each as a "thin" or "thick" group. Each group of layers is analyzed and the entire structure is reassembled. Regions such as glass superstrates or encapsulation layers having thicknesses greater than a few microns, and textured structures, are treated in a noncoherent regime. Thin and specular layers, such as those used for antireflection (AR) coatings and in thin film a-Si devices, are treated as coherent regions.

PV Optics can be used to optimize a variety of cell parameters, such as cell absorber thicknesses, the structure of the texture, AR coating parameters, and the back-reflector design. Here, we will demonstrate some capabilities of the package by specific examples. The model is a user-friendly tool using a "Windows" environment. It requires (as input) the optical constants of each layer as a function of wavelength and the layer thicknesses. Texture is simulated by allowing the user to select appropriate geometric features in addition to co-planar layers. Computing times depend significantly on the conditions chosen and can vary from minutes to hours. The examples we present are intentionally kept simple to demonstrate the capabilities of the package and show that results are often obtained that would not have been expected intuitively.

Operating *PV Optics*

PV Optics starts with a generalized device configuration as illustrated in Fig. 1. From this, one can select a desired device configuration. The device may include glass, encapsulation, AR coating, up to three semiconductor layers, a buffer, and a metal layer. The device-configuration choice is made

by simply deleting, with a click of a mouse, portions of the device configuration that do not correspond to the desired device.

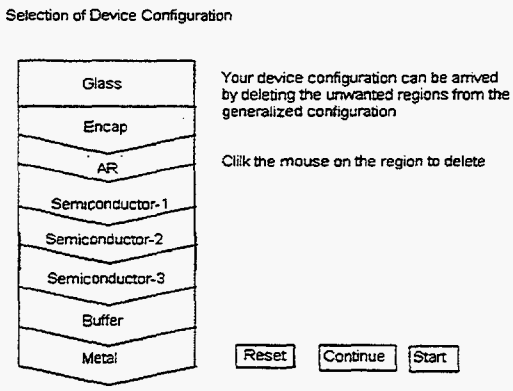

Figure 1: Illustration showing how the device configuration can be selected from the total module configuration.

Once the device configuration is reached, the program expects data pertaining to each layer and its interfaces. There is a "page" of each layer. The software provides default values for the interface type, thickness in microns, and n and k of each region. The default values correspond to standard materials used in PV manufacture. One can either use the default values or change them simply by a click. The antireflection page provides the default values for the interface type, n1, k1, thickness1, n2, k2, and thickness2 for a two-layer AR coating (n1, n2 are the refractive indexes and k1, k2 are the extinction coefficients). The selection of the semiconductor page provides choices of up to three junction cells and options to select the material "Silicon" or "Amorphous-Silicon," "Amorphous-Silicon Top," "Amorphous-Silicon Middle," or "Amorphous-Silicon Bottom." Additional semiconductor data can be incorporated at request.

PVOptics can output the calculated results in seven types of graphs: (1) Reflectance/ Transmittance, (2) Absorbance, (3) Weighted Absorbance, (4) Photon Flux, (5) Reflectance/ Transmittance (Non-Coherent), (6) Reflectance/Transmittance (Coherent), and (7) Weighted Absorbance.

Results

In this section, we present the results of calculations for a number of cell and module structures as examples of the capabilities of *PV Optics*. The first example is a comparison of the optical characteristics of a silicon solar cell before and after encapsulation. Fig. 2 shows the reflection and the absorption spectrum of a Si solar cell. The calculations include the absorption in Si as well as in the metal. The structure of the cell considered in the calculation has the textured front with a two-layer AR coating consisting of 710 Å of Si_3N_4 (refractive index = 1.95) on 100 Å of SiO_2 (refractive index = 1.45). The texture height is 3 μm, the thickness of the Si layer is 250 μm. The backside of the cell is also textured and has Al metallization. The calculated Maximum Achievable

Current Density (MACD) = 41.02 mA/cm^2. Fig. 3 shows similar plots after the cell is encapsulated. The structures of the cell and the module are both illustrated in each figure. The MACD value after the encapsulation is 38.75 mA/cm^2. Thus, there is a loss of approximately 2.3 mA/cm^2 associated with encapsulation. From Fig. 3, we can see that after encapsulation there is a significant increase in the reflection (in the wavelength range of 0.5μm - 1μm). The loss caused by this increase in reflection is offset by a decrease in the reflectance in the wavelength range of 0.4μm - 0.5μm.

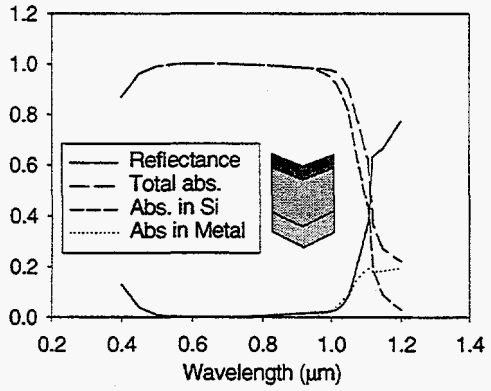

Figure 2: Calculated characteristics of a silicon solar cell (see text for the cell structure).

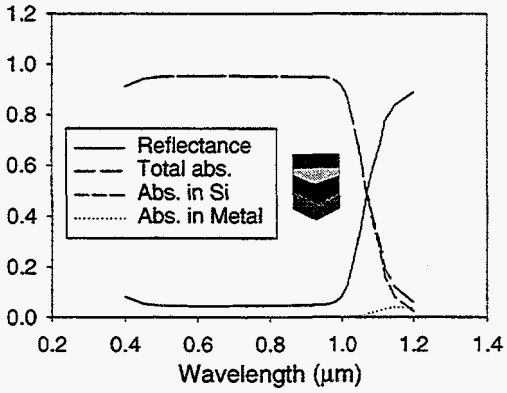

Figure 3: Calculated characteristics of the cell shown in Fig. 2, after encapsulation (see text for the cell structure).

From Fig. 2 and Fig. 3 we see an expected behavior of the reflectance — the cell reflection has a broad null in the wavelength range of 0.5 (m and 0.9 (m, while the module reflectance is dominated by the glass reflection. These figures also show absorption in the back metal is slightly less in the encapsulated case.

We will now compare the optical characteristics of a frontside textured cell with the double-sided textured cell of Fig. 2. To do this, we consider the cell of Fig. 2 and change the backside of the cell to a planar interface. The calculated results are shown in Fig. 4. Notice that the loss in the metal is lower, yet the MACD decreases to 40.66 mA/cm2. The lower loss in the back planar surface, compared to the back textured surface, can be explained in a rather oversimplified manner as follows. The light that reaches the backside undergoes one reflection at this planar surface, while a textured interface leads to more than one reflection. Because each reflection from the Si-Al interface is accompanied by metallic absorption, the textured interfaces lead to higher metal absorption. Clearly, the metallic loss depends on a number of parameters that include angle of incidence at the Si-Al interface and the intensity of light incident at the interface. Interposing a buffer layer of low refractive index between the semiconductor and the metal can mitigate this loss.

In other example, we consider optimization of AR coating thickness for a cell in air and for module operation. The cell has a 100-μm thick substrate with a 3-μm pyramid-type texture on both sides.

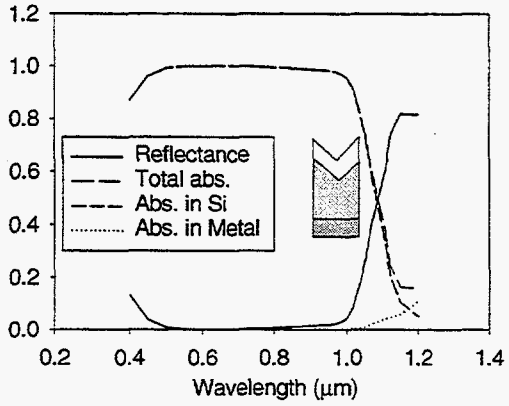

Figure 4: Calculated characteristics of a Si solar cell with frontside textured (see text for cell structure).

The AR coating consists of Si_3N_4 (n = 1.95) on a 100 Å of SiO_2. Figure 5 shows the calculated MACD, as a function of Si_3N_4 thickness, for two cases — cell in air, and after encapsulation. From this figure one can notice several important results: (a) as expected, there is an optimum thickness, around 700 Å, (b) the optimum thickness is about same (for this refractive index film) for air and encapsulated operation, (c) an unexpected feature is that the MACD for module operation is higher for the double-side textured cell, and (d) the dependence of MACD on AR thickness is less critical for module operation.

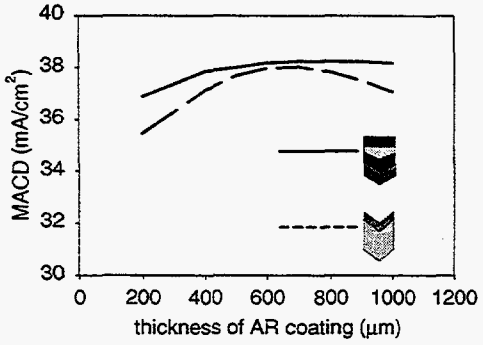

Figure 5. Calculated MACD as a function of Si_3N_4 thickness in a double layer AR coating. The dashed line and solid lines correspond to air and module operation.

Conclusion

PV Optics is a solar cell and module design package that is applicable to thin- as well as thick-cell design and analysis. It can be applied to devices based on all material system. Because of its unique capability to analyze losses caused by metal absorption, the amorphous silicon solar cell community, in particular, has a strong interest in *PV Optics* for the analysis and design of thin cells and modules.

SELF-DOPING CONTACTS AND ASSOCIATED SILICON SOLAR CELL STRUCTURES

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ABSTRACT: Contacts to <111> Si which are self-doping and self-aligning were investigated. Such contacts are applicable both to conventional cell structures as selective emitters and to more demanding structures such as interdigitated back contact cells. Emphasis was placed on alloyed contacts of Al for providing a self-doping p-type contact and of Ag-Sb for a self-doping n-type contact. Alloying at 900°C of 1.1% (wt.) Sb in Ag doped Si to a value of 2×10^{18} Sb/cm^3, suggesting a 5% (wt.) Sb is needed for ohmic contact. An Al alloy p-n junction was found to be suitable for a solar cell if placed at the back of the cell, with 13.2% efficiency and good IQE demonstrated for a fully screen-printed dendritic web cell. A prototype interdigitated back contact cell was fabricated by screen printing (Al and Ag) with tight alignment (100 μm lines and spaces) on a dendritic web substrate with an efficiency of 10.4%.

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13. ABSTRACT *(Maximum 200 words)*

The theme of this workshop is "Supporting the Transition to World Class Manufacturing." This workshop provides a forum for an informal exchange of information between researchers in the photovoltaic and non-photovoltaic fields on various aspects of impurities and defects in silicon, their dynamics during device processing, and their application in defect engineering. This interaction helps establish a knowledge base that can be used for improving device fabrication processes to enhance solar-cell performance and reduce cell costs. It also provides an excellent opportunity for researchers from industry and universities to recognize mutual needs for future joint research. The workshop format features invited review presentations, panel discussions, and two poster sessions. The poster sessions create an opportunity for both university and industrial researchers to present their latest results and provide a natural forum for extended discussions and technical exchanges.

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