DOE/GO/10390-Q

Quarterly Report- 3
DOE Grant Number :- DE-FG36-99GO10390
Project Title:- A DSP based power electronics interface for alternate/renewable energy systems.

Abstract: -

This report is an update on the research project involving the implementation of a DSP based power electronics interface for alternate/renewable energy systems, that was funded by the Department of Energy under the Inventions and Innovations program 1998.

Objective:

The objective of this research is to develop an utility interface (dc to ac converter) suitable to interconnect alternate/renewable energy sources to the utility system. The DSP based power electronics interface in comparison with existing methods will excel in terms of efficiency, reliability and cost. Moreover DSP-based control provides the flexibility to upgrade/modify control algorithms to meet specific system requirements. The proposed interface will be capable of maintaining stiffness of the ac voltages at the point of common coupling regardless of variation in the input dc bus voltage. This will be achieved without the addition of any extra components to the basic interface topology but by inherently controlling the inverter switching strategy in accordance to the input voltage variation.

System Block Diagram:

The block diagram of the proposed DSP based interface is shown in Figure 1. Texas Instruments DSP TMS320F240 is used in the implementation of the controller. TMS320C24x is the newest DSP family introduced by Texas Instruments Inc. for motor control and power electronics applications. TMS320C240 has 12 PWM channels, 9 of which can be controlled independently. A programmable dead band generator is provided to avoid shoot through faults in a three phase voltage source inverter. The required currents or/and voltages can be sampled using the integrated dual 10bit, 16 channel ADC. Moreover, the DSP (TMS320F240) which is chosen to implement this algorithm not only provides the computational capability but also integrates all the power electronics peripherals necessary to implement any such system. These peripherals include PWM generators, timers, ADC etc.

DISCLAIMER

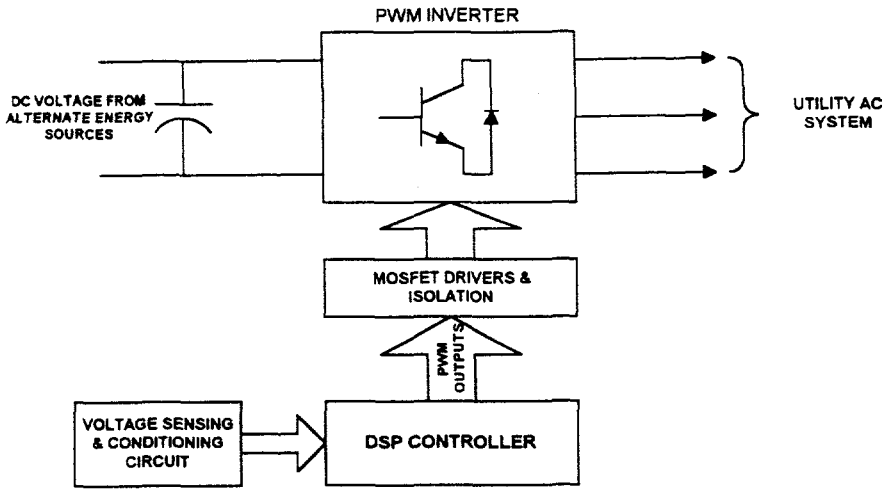


Fig. 1 Block diagram of the proposed DSP based interface.

Hardware Setup:

The main controller setup (an Evaluation board for TMS320F240) for this project has been obtained from Texas Instruments under University Support program and is shown in Figure 2.

Figure 3 shows a three phase voltage source inverter module which has been purchased from Spectrum Digital Inc. This module has all the necessary power devices (MOSFETs) and the necessary MOSFET driver circuits.

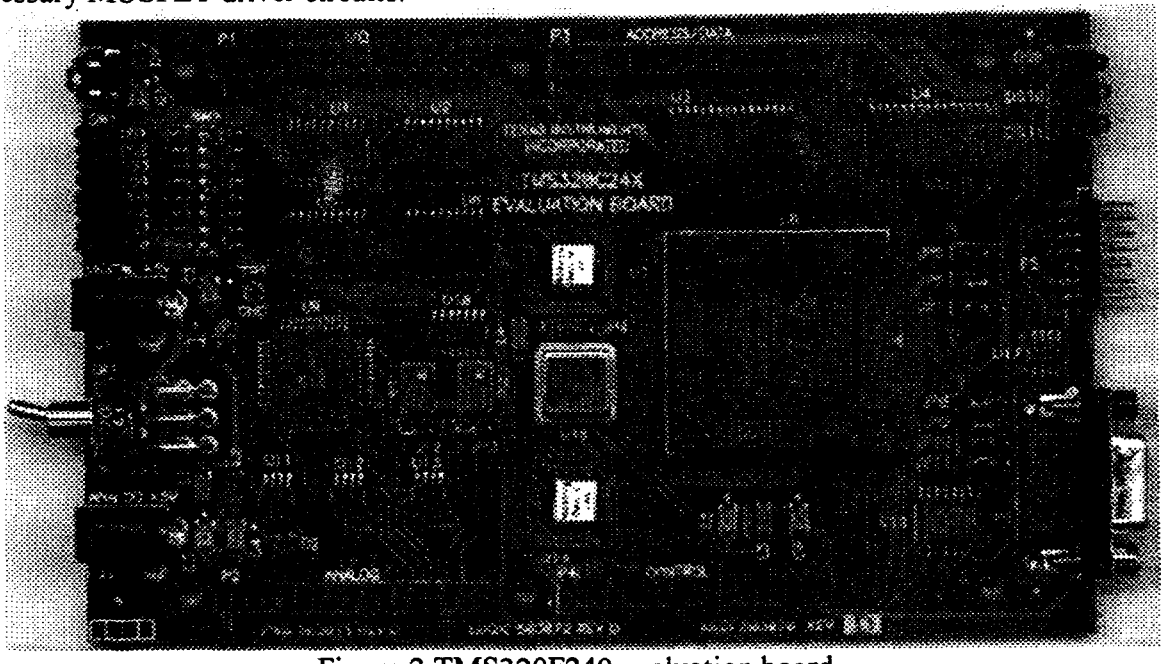


Figure 2 TMS320F240 evaluation board.

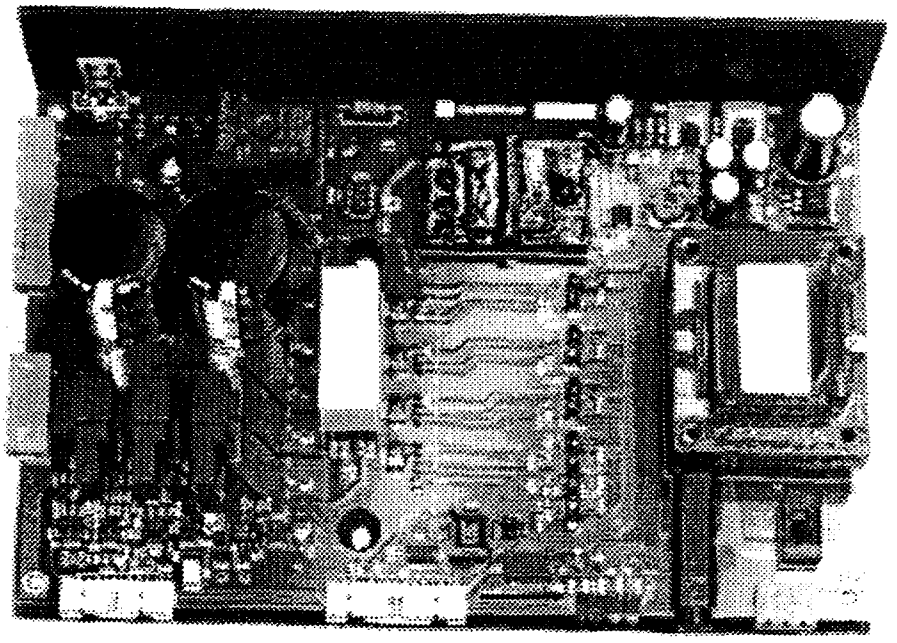


Figure 3 Three Phase Voltage source inverter .

A Lab Drive Interface Module is used to interface the DSP Module with the three phase pulse width modulated (PWM) Inverter Module. The block diagram of the hardware setup is shown in Figures 4 and 5. A 1/3 horsepower ac induction motor is being used as the three phase load for the inverter.

The DC bus voltage on the 3 phase inverter module is sensed using a divider circuit and then isolated with an opto-coupler. On the detector side of the opto-coupler, the sensed voltage is conditioned with a voltage amplifier before the signal is passed to the Labdrive Interface Module. This analog signal is then applied to the analog expansion bus on the DSP board. Input 4 of the A/D converter is used for the inverter bus voltage sense (ADCIN4). It was measured that ADC changes count for every 0.21V change on the inverter bus voltage. The A/D conversion time is about 7uS.

The capacitors on the inverter module were changed from two 470uF, 400V capacitors to two 22uF, 350V capacitors. The reduction in the size of the filter capacitors allows the bus voltage to vary with a high degree of ripple. When the 3-phase induction motor is starting, it requires a great amount of torque and draws relatively large currents. Therefore, the ripple is really high, but as it gains rotational speed, the current demand lowers and so does the ripple. Nevertheless the ripple is still noticeable at desired speed.

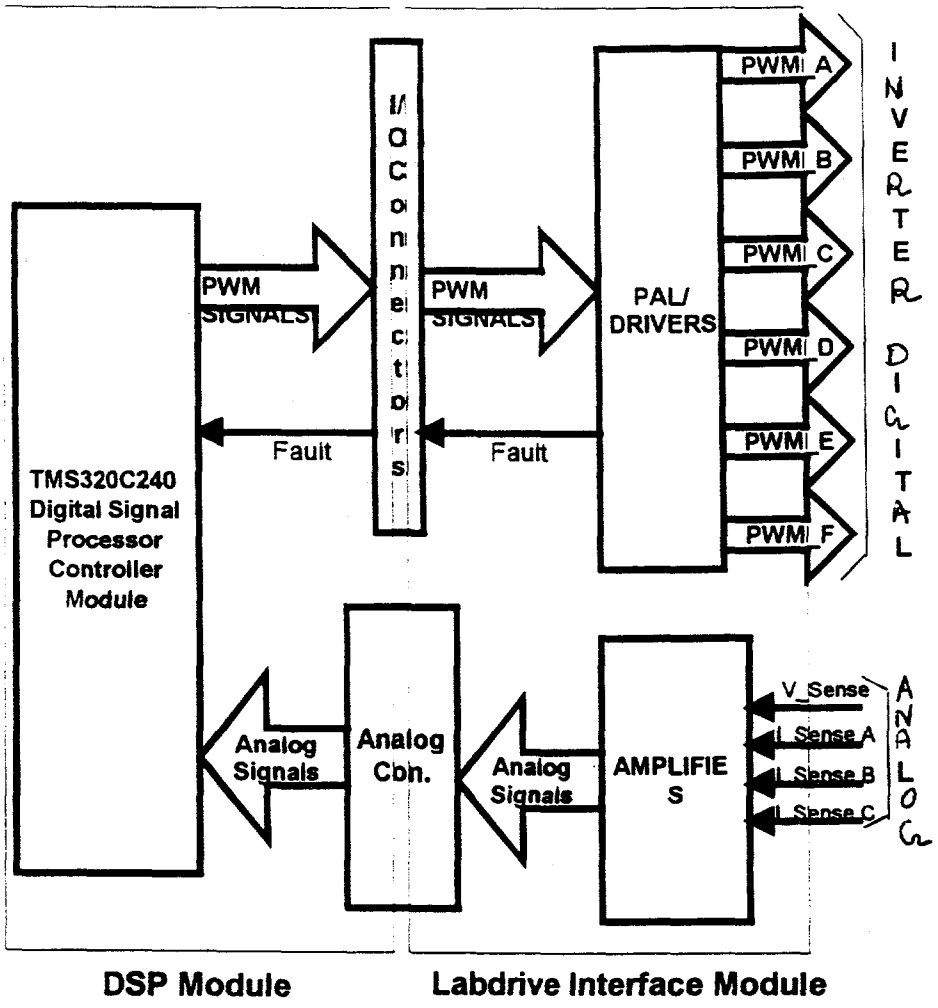
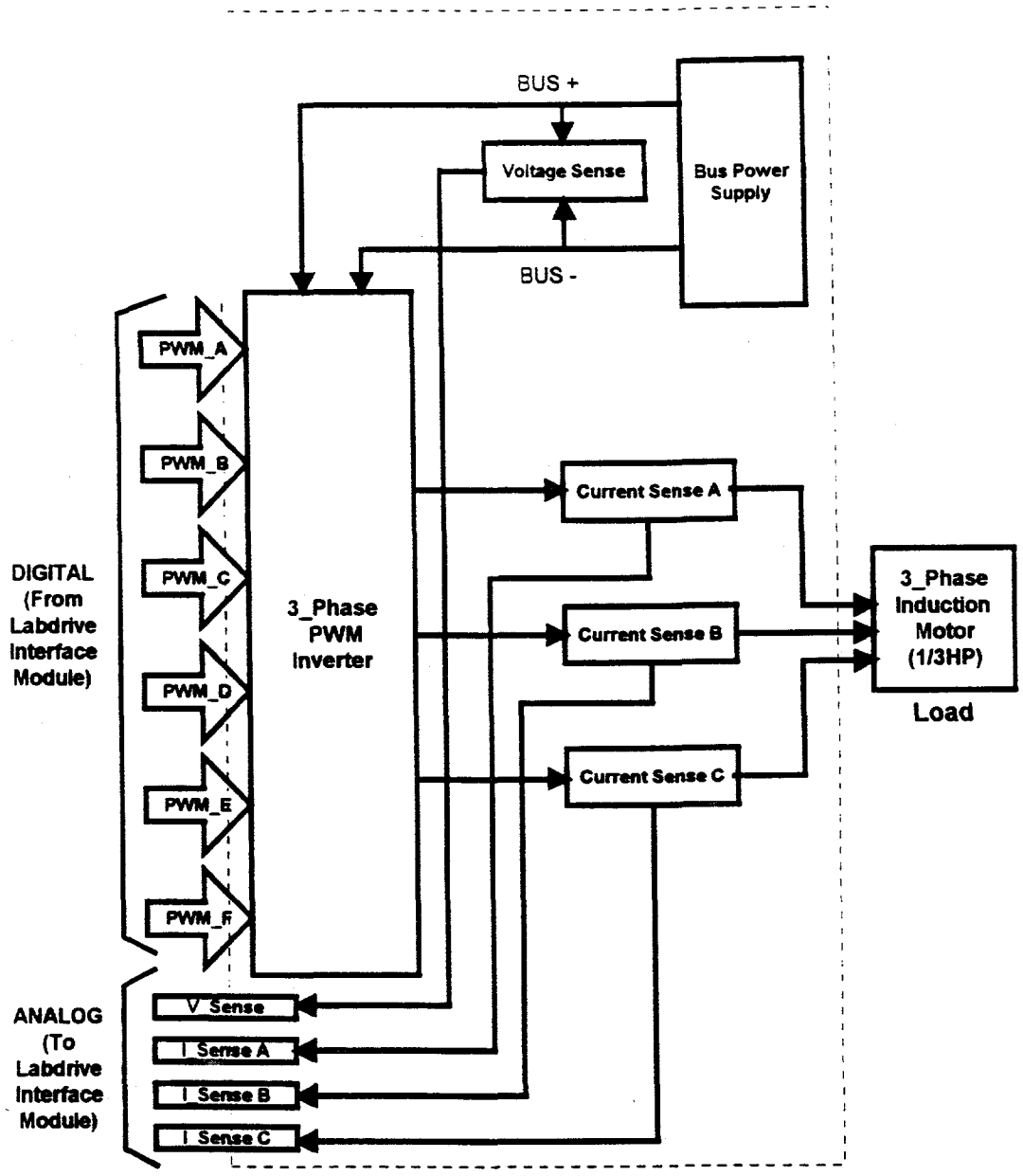


Figure 4: DSP and Lab drive Interface Module



3_Phase AC Induction Inverter Module

Figure 5 : Three-Phase Inverter Module Interface

Software Algorithm:

The relevant software for the DSP Board are,

- XDS510PP Emulator
- TMS320C2xx C source debugger/ Linker.

The software will gather voltage readings from the DC bus on a continuous basis and locate the maximum and minimum points of the ripple voltage and then find the average. Then on real time basis, it will compare the bus voltage with the average bus voltage. If the bus voltage is less than the average voltage, then it will add to the count of the register period (T1per) which allows the up/down counter to count higher before it reaches its peak, therefore, the pulse width will increase, allowing more energy to get to the load. If the bus voltage is more than the average bus voltage, then the opposite will happen.

Implementation of the switching scheme

The symmetric switching scheme is implemented with the TMS320F240 DSP which determines the switching order for the three PWM channels. The switching order scheme is shown in Figure 6.

The following properties are observed in the patterns: 1) There is a fixed switching order for the three PWM channels in each sector, 2) Each pattern starts with O_{000} and ends with O_{000}. The space vector switching PWM pattern remains the same. Only the timing is increased or decreased depending on the fluctuations of the monitored bus voltage.

Two steps are taken to implement this switching scheme. The first step is to initialize the compare units and set up timer 1 for symmetric PWM. The second step is the channel toggling sequence, which is based on the look up table and the timing for each compare register.

Timer 1 is set up for continuous up/down mode for symmetric PWM:

SPLK #1000100000000010b,T1CON

Action register is in charge of PWM output polarities. PWM outputs 1,3 and 5 are active low and PWM outputs 2, 4 and 6 are active high:

SPLK #0000100110011001b, ACTR

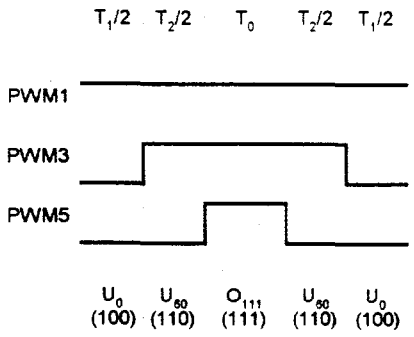
Channel dead band is determined and enabled. Dead band is set for 2uS.

SPLK # 0000010111111000b, DBTCON

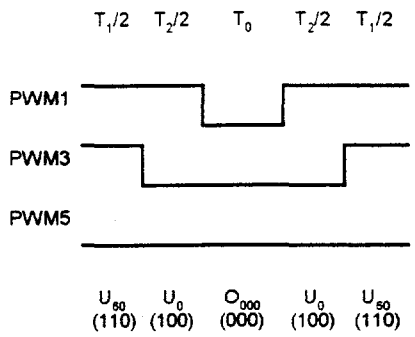
The compare operation is enabled and PWM mode is selected.

SPLK #1000001000000111b, COMCON

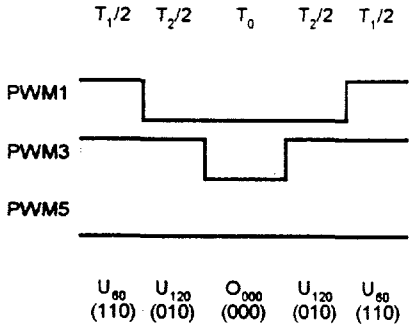
The software determines in which sector the vector Uout is located. The software also decomposes the Uout to find the timing contribution (Ta, Tb, and Tc) for each PWM period. Ta Tb and Tc are the full compare values which are then loaded in the full compare registers. When the up/down counter value reaches the value of a full compare register, a transition is made and a toggling action occurs. The critical count (the highest count of period register) is varied in an inverse proportion to the monitored inverter bus voltage. The software varies the critical count, which affects the width of the PWM pulses, hence reducing the low order harmonics.



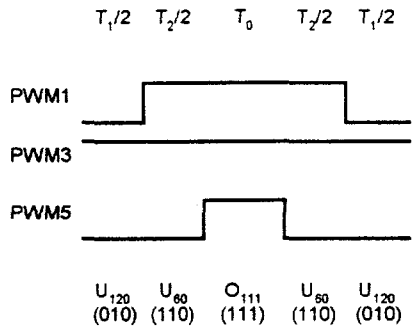
U_{out} in sector of U_0 - U_{60}, SVRDIR=0, (D_2 D_1 D_0)=(001)



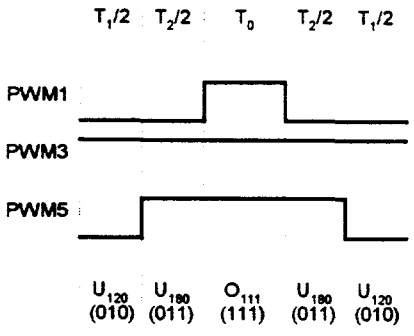
U_{out} in sector of U_0 - U_{60}, SVRDIR=1, (D_2 D_1 D_0)=(011)



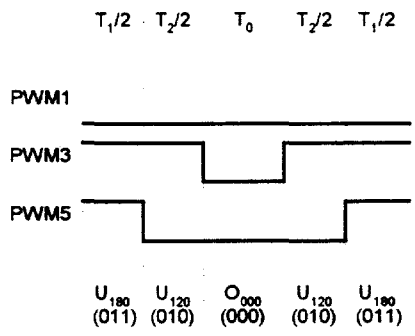
U_{out} in sector of U_{60} - U_{120}, SVRDIR=0, (D_2 D_1 D_0)=(011)



U_{out} in sector of U_{60} - U_{120}, SVRDIR=1, (D_2 D_1 D_0)=(010)



U_{out} in sector of U_{120} - U_{180}, SVRDIR=0, (D_2 D_1 D_0)=(010)



U_{out} in sector of U_{60} - U_{120}, SVRDIR=1, (D_2 D_1 D_0)=(110)

Figure 6. Modified Space Vector Switching scheme.

Present Status :

As described in the above sections, the hardware setup is complete. The software development for generating appropriate PWM waveforms to implement the proposed algorithm using a modified space vector switching scheme is underway.

Research Personnel:

The PI is being assisted by a graduate research assistant on this project.

Technology Transfer:

- The PI worked closely with a DOE selected Market Analyst from New Horizon Technologies on a market survey. Few company leads have been obtained from the internet. The completed survey will be used to negotiate some collaborative work.
- The Power Electronics/ Motor Drives Application group at Texas Instruments, Houston is providing support in the DSP area and they are interested in marketing their DSP for this certain application.