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NANOFABRICATED SiO_2-Si-SiO_2 RESONANT TUNNELING DIODES

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ABSTRACT

Resonance Tunneling Diodes (RTDs) are devices that can demonstrate very high-speed operation. Typically they have been fabricated using epitaxial techniques and materials not consistent with standard commercial integrated circuits. We report here the first demonstration of SiO_2-Si-SiO_2 RTDs. These new structures were fabricated using novel combinations of silicon integrated circuit processes.

INTRODUCTION

One approach to the generation and detection of millimeter wavelength radiation is the use of Resonance Tunneling Diodes. These structures consist of a thin (nm scale) layer of high quality crystalline material, sandwiched between two thin (nm scale) barrier layers. These devices can exhibit negative differential resistance and extremely high-speed operation [1-2]. RTDs have almost invariably been fabricated using epitaxial growth techniques. This restricts the possible combinations of materials that may be employed, typically to the III-V or Si/Ge systems [3-6]. In particular, there are few good choices for barrier materials and this limits device performance. Due to the overwhelming dominance of silicon in most areas of microelectronics and the maturity of Si processing techniques, SiO_2/Si/SiO_2 structures would be highly desirable. However, due to the amorphous nature of SiO_2, such a structure is impossible to fabricate using standard epitaxial techniques. In this paper we will describe a fundamentally different RTD fabrication approach that makes use of novel combinations of Si processing techniques. Single crystalline, parallel and smooth, sheets of Si were nanomachined using a combination of reactive ion etching and KOH wet etching of Si {110} substrates. The tunnel oxide barriers were grown using processes developed for non-volatile memory applications. These structures were integrated with modified IC fabrication processes to form trench isolation and electrodes. The finished devices were orientated perpendicular to the wafer surface and had active areas less than one square micron. Using this approach we have been, to the best of our knowledge, the first to demonstrate negative differential resistance with SiO_2/Si/SiO_2 structures.

FABRICATION

The major problem to be overcome is fabrication of the thin (1-10nm) layer of high quality single crystalline Si, which will act as the resonant layer. Over the years, etch processes have been developed which have very high (at least 100:1) selectivities. Examples are the relative etch rates of SiO_2 to Si in HF [7] and the selectivity of KOH to {100} Vs the {111} planes [8]. Furthermore, it is readily possible to grow thin layers of material with dimensions down to 1.5-3nm (for example tunnel oxides for memory

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technologies) and deposit thin films down to tens of nm. We have been able to demonstrate that novel combinations of these processes can be used to fabricate active $SiO_2/Si/SiO_2$ resonant tunneling structures.

The approach we have taken employed a combination of fillets as reactive ion etch masks, a systematic miss-orientation of the masks, KOH etching of {110} substrates and the further thinning by the growth of the tunnel oxide. In summary, a 50-100nm wide silicon nitride fillet mask was used to define thin fillets of silicon during a reactive ion etch 1μm into a Si {110} substrate. The fillets connected to pads and were ~2μm long. The fillets existed in arrays each rotated 0.1° one from another to +/- 1.5° (a total of 31 splits). The 0° offset was nominally aligned to one of the perpendicular {111} planes. The resulting topography was then filled with silicon dioxide and chemical mechanical polishing (CMP) was used to planarize the surface. The embedded oxide served as dielectric isolation. The wafers were then coated with 100nm SiN, which will acted as a HF and CMP stop. Following this, holes were opened up in the SiN along both sides of the thin Si fillet. The underlying oxide was then partially removed by a combination of dry (RIE) and wet (HF) etching. The fillets were then thinned by a brief exposure to a KOH etch which stops on {111} planes. The range of angles of misalignment of the silicon lines to the perfect {111} direction led to a continuous range of Si sheet thickness. There was also a relatively fixed amount removed as a result of the micro-roughness and taper associated with the Si etches. When the amount of miss-orientation was too great, the Si was completely removed. As expected, this occurred in a systematic manner across the die. The thin sheets of Si were single crystalline, defect free, atomically parallel and smooth and supported on all 4 sides. The thinned Si sheets were then given a dilute HF dip just prior to the growth of a thin tunnel oxide in a vertical thermal reactor. An example of a thinned sheet with the dielectrics removed using HF is given in Fig. 1.

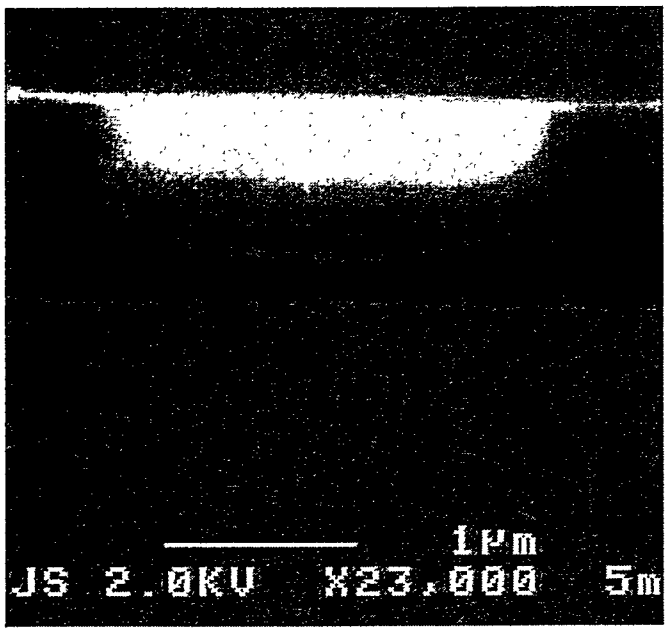

Fig. 1.
Oblique view of a thinned sheet . The dielectic films have been removed by HF. The sheet remains supported on three sides by the Si fillet. The sheet is sufficiently thin that charge from the electron beam can not be carried away sufficiently rapidly to prevent charging effects which cause the sheet to "glow".

Immediately following growth, a 100nm layer of insitu doped Si was deposited by CVD (Chemical Vapor Deposition). This was followed by depositions of Ti/TiN and CVD W, which formed the contacts on either side of the resonator. CMP was then performed, stopping on the patterned SiN underlayer. This planarized the structures and electrically isolated the pads. Further isolation was provided by a brief etch of the silicon followed by a 500nm silicon dioxide deposition. The oxide was patterned down to the W and Al was deposited and patterned to facilitate the formation of wirebonds. Finally, a N_2/H_2 anneal was employed to reduce interface traps between the Si and the SiO_2.

During testing the sample was placed inside a liquid helium Dewar for low temperature ($4.2K < T < 77K$) measurements. A calibrated RuO_2 resistor mounted next to the sample was used to measure the temperature. By applying a small (2mV at 13.7Hz) modulation voltage, both the current (I) and differential conductance (dI/dV) versus bias voltage (V) were measured simultaneously.

RESULTS AND DISSCUSSION

In this initial approach, the exact alignment of the photolithographic system to the {111} was unknown and this was addressed by introducing a range of miss-orientations on the mask. This problem could be approached in a more manufacturable manner by first performing a test etch and then aligning the photolithographic alignment marks to the correct set of etched planes. We have used this approach in the past and have found that it can result in alignment to within 0.2 degrees. Accuracy in Si sheet definition could also be further improved by refinements in fillet formation and pattern transfer.

Electrical testing of the structures clearly demonstrated resonance tunneling effects. We show I and dI/dV versus V measured at T=4.2K in the top and bottom panel of Fig. 2 respectively. In the top panel, negative differential conductance (NDC) is clearly observed at bias V~370mV with peak to valley current ratio of 1.15. Another shoulder feature in I-V can also been seen at bias V~930mV. Their corresponding features can be clearly seen in dI/dV as shown in bottom panel of Fig. 2. In Fig. 3, dI/dV versus V is plotted for the feature around 370mV measured at five different temperatures. This plot shows that the feature becomes sharper and more pronounced with decreasing temperature. Similar temperature dependence is also observed for the feature around 930mV. This temperature dependence is consistent with resonant tunneling. Both features remain unchanged after more than ten thermal cycles between 300K and 4.2K, again indicating that the observed I-V features are most likely due to the resonant tunneling of quantum well states. Tunneling through defect states is expected to be significantly affected by thermal cycling. Two other samples are also found to have similar IV features but with slightly lower resonance voltages. Table 1 summarizes the resonant voltage for all three samples, where the resonance voltage is defined as the voltage at which the differential conductance reaches its minimum.

Table 1

Sample	1st resonance voltage	2nd resonance voltage
Die 1 (w<10nm)	370mV	932mV
Die 2 (w<10nm)	224mV	644mV
Die 3 (w<10nm)	195mV	650mV

To quantitatively compare our measured I-V behavior with double barrier resonant tunneling theory, we calculated energy eignvalues for a Si quantum well (QW) sandwiched between two layers of SiO_2. We assumed a barrier height of 3.34eV for SiO_2 and effective masses of $0.35m_o$ and $0.6m_o$ in Si and SiO_2 respectively, where m_o is the bare electron mass [9]. In Fig.4, we plot the calculated values of the ground state (E_1 solid curve) and first excited state (E_2 dotted curve) energies versus width of the Si QW. To compare with our experimental data, we assumed that the resonance voltage occurs at $3E_n$. The factor of 3 comes from the assumption that the voltage drops are equally divided among the quantum well and two barriers. The voltage drop across the contacts was found to be negligible. We fit our measured value of E_1 to the calculated result with the width (w) of the QW as fitting parameter. Using the fitting result of w, we plot measured values of E_1 and E_2 versus w for all three samples in Fig. 4. The fitted result of w~3-4nm is very close to the value from our fabrication estimate.

Future work will concentrate on improvements in the signal-to-noise ratio. This will be done by improvements to the design and process flow. As fabricated, the parts have a very small active area ($<1\mu m^2$) in comparison to most devices reported in the literature [3,4,6]. This results in a relatively large ratio of perimeter-to-area.

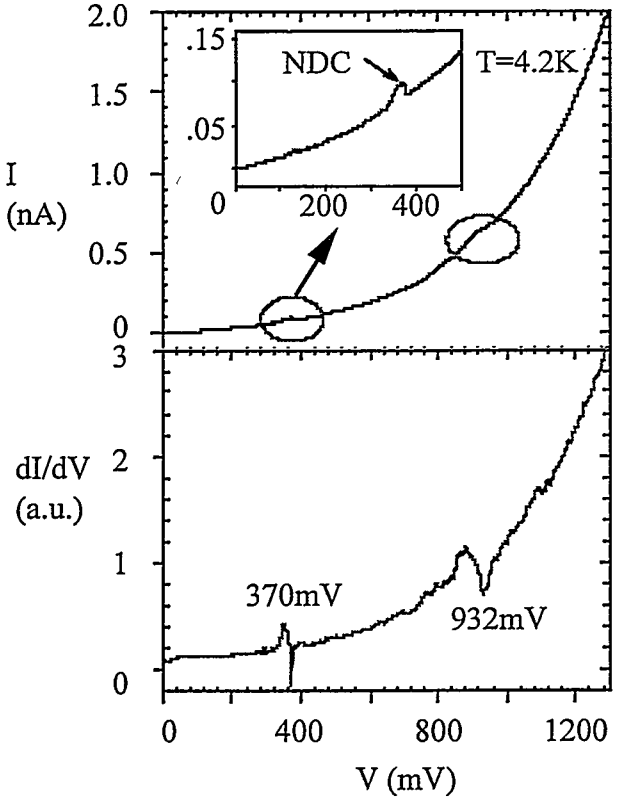

Fig. 2
Plots of current versus voltage and dI/dV versus voltage for parts tested at 4.2K

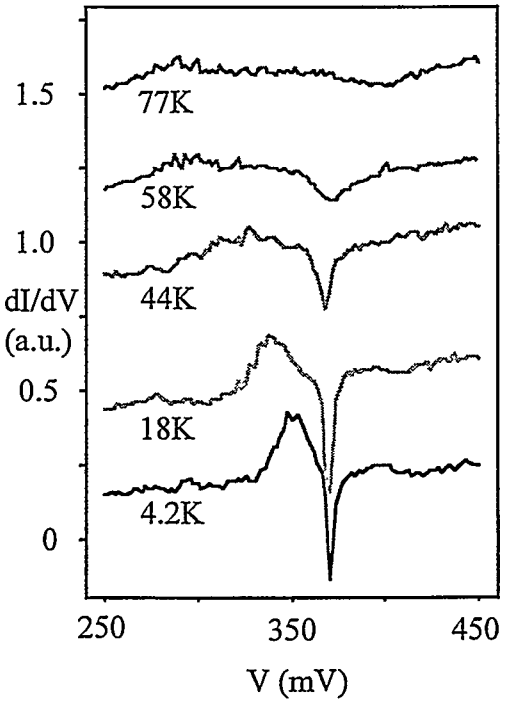

Fig. 3
Plots of dI/dV versus V for different temperatures.

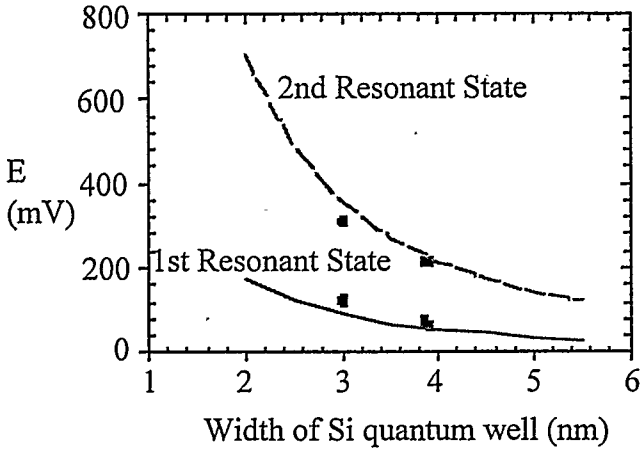

Fig. 4
Our measured value of E1 to the calculated result with the width (w) of QW as fitting parameter.

It seems reasonable that leakage on the perimeter of the device will be relatively high. This problem can be addressed by increasing the active area. However, this increases the likelihood that the thin Si membrane will break during processing. This can be addressed by forming one side of the sheet and then anchoring the sheet on that side, so that it is supported during the thinning process. This relatively simple process change should allow for an increase in active area and enable thinner Si sheets, all of which should improve the signal-to-noise ratio. The use of silicon on insulator material could also potentially reduce edge effects.

There are many other possible modifications to the process. For example it can be extended to the more commonly used Si {100}. Also, the structure in Si {110} is orientated perpendicular to the surface. In this orientation it is relatively easy to make electrical contact to the sheet. This is in contrast to the standard MBE approaches and may also offer some advantage for the generation and detection of millimeter waves.

CONCLUSION

This work demonstrates that silicon compatible nanomachining techniques show promise for the fabrication of $SiO_2/Si/SiO_2$ resonant tunneling structures. The electrical performance is not sufficient for application to practical devices. However, this work is in its very early stages. Through further, obvious refinements to the fabrication process we hope to increase the operating temperature and the peak-to-valley ratio of the devices.

ACKNOWLEDGEMENTS

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