Comparison of Fabrication Approaches for Selectively Oxidized VCSEL Arrays

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MAY 04 2000
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ABSTRACT

The impressive performance improvements of laterally oxidized VCSELs come at the expense of increased fabrication complexity for 2-dimensional arrays. Since the epitaxial layers to be wet-thermally oxidized must be exposed, non-planarity can be an issue. This is particularly important in that electrical contact to both the anode and cathode of the diode must be brought out to a package. We have investigated four fabrication sequences suitable for the fabrication of 2-dimensional VCSEL arrays. These techniques include: mesa etched polymer planarized, mesa etched bridge contacted, mesa etched oxide isolated (where the electrical trace is isolated from the substrate during the oxidation) and oxide/implant isolation (oxidation through small via holes) all of which result in VCSELs with outstanding performance. The suitability of these processes for manufacturing are assessed relative to oxidation uniformity, device capacitance, and structural ruggedness for packaging.

Keywords: VCSEL, arrays, selectively oxidized, fabrication

INTRODUCTION

There has been a dramatic improvement in VCSEL performance with the advent of monolithic oxide confined VCSELs¹. The selectively oxidized devices have record low threshold currents², threshold voltages only slightly above the photon energy³, and high efficiencies⁴. The enhanced electrical and optical confinement provided by the oxide layer in these devices have made high performance devices the norm in the laboratory. Fabrication of these devices requires exposing the epitaxial layers to the oxidizing ambient by etching through the top distributed Bragg reflector (DBR) stack. The simplest device to fabricate is the Mesa Etched structure shown in Fig. 1. This Mesa Etched structure works well for testing on the probe station in a research laboratory, but commercial devices require that the electrical contacts be brought out to a package. We describe here several significant challenges in achieving robust electrical contact from the device to the package which are relevant as we develop high-density, high-count 2-dimensional VCSEL arrays for emerging applications. Thus, we have examined several different device structures and present the attributes of each below. It is the purpose of this work to provide insight into suitable fabrication techniques for packaged VCSELs relevant for present and emerging VCSEL applications.

FABRICATION REQUIREMENTS

Packaged VCSEL performance can be significantly impacted by the device structure used. Four basic characteristics have been evaluated to determine the suitability of a given device structure for the development of packaged high performance oxide VCSEL arrays: (i) Packaging yield, i.e. amenable to wire bonding; (ii) Oxidation uniformity; (iii) Low capacitance; and (iv) Repeatable fabrication.

Developing prototype arrays of ever-increasing complexity requires that the finished product be easy to wire bond into a package. Low packaging yield is unacceptable for high-count 2-D arrays. Thus, the device packagability is the first metric considered for determining the suitability of a device structure for prototyping applications. The typical failure mode is that the bond pad metal adhesion to the layer below it is insufficient to maintain integrity during the wire bonding process. There are many factors that can influence the adhesion but repeatability of the wire bond is essential and any wire bond failures are intolerable.

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Figure 1. Mesa Etched VCSEL used for probe testing in the laboratory.

The next metric considered is the oxidation uniformity. It has been shown that the Mesa Etched structure in Fig. 1 results in outstanding oxidation uniformity across a wafer⁵. Changing the device structure can severely effect the oxidation uniformity resulting in wide variations in device performance across a wafer. Most applications require good uniformity across the arrays and this is increasingly important with 2-D arrays. Thus, the oxidation uniformity must not be compromised by the choice of device structure.

As prototype requirements move to higher speeds, the capacitance associated with the bond pad metal becomes a significant consideration. The bond pad is the largest part of the device, typically $100\mu\text{m} \times 100\mu\text{m}$. This large area metal contact is parallel to the conducting substrate resulting in a significant capacitance that can easily dominate the packaged device speed as indicated in the equivalent circuit of Fig. 2. Ideally, there should be no capacitance associated with the bond pad to minimize packaging parasitics, thus allowing the maximum VCSEL modulation rate.

Finally, small variations in the VCSEL fabrication process should not significantly effect the finished device characteristics. Thus, the fabrication sequence for the device must be straightforward and repeatable for robust manufacture.

Figure 2. A simple VCSEL equivalent circuit which includes the bond pad capacitance.

VCSEL STRUCTURES

Using the packagability, oxidation uniformity, bond pad capacitance and fabrication reproducibility as evaluation metrics, four basic device structures have been evaluated; the Mesa Planarized, the Trench Oxidized, the Oxide Isolated and the Mesa Bridged, as described below.

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Our initial packaged VCSEL arrays were fabricated using the Mesa Planarized structure shown in Fig. 3. This is a straightforward extension of the Etched Mesa structure where the area between mesas is filled with a polymer and the bond pad metal is deposited directly on top of the polymer. This structure retains all of the positive attributes of the Etched Mesa structure such as good oxidation uniformity, excellent device to device electrical isolation, and ease of fabrication. In addition, the bond pad capacitance is low due to the low dielectric constant and large thickness of the polymer, resulting in a low packaged device capacitance. Indeed, this device structure has produced the record VCSEL small signal modulation bandwidth⁶. Unfortunately, polymer planarization typically results in either 'peaks' or voids at the mesa/polymer interface, either of which can result in breaks in the metal trace connecting the mesa to the bond pad. More significantly, reproducibly obtaining good bond pad metal adhesion to the polymer has proven very difficult. Typically, individual devices can be packaged but packaging yields for arrays can be low due to bond pad failure.

Figure 3. The Mesa Planarized VCSEL exhibits very low bond pad capacitance, but poor metal/polymer adhesion.

The Trench Oxidized structure is currently being fabricated by commercial VCSEL manufacturers. Rather than etching a mesa, a set of small via holes are etched into the mirror stack allowing oxidation as shown in Fig. 4. The resulting structure is essentially planar with the bond pad metal being deposited directly on the top of the VCSEL resulting in excellent metal adhesion. Achieving the correct etch depth for the small vias, obtaining good oxidation uniformity across the wafer and realizing good device to device electrical isolation with stacked ion implantation are the challenges to be met in attaining reproducible fabrication. The Trench Oxidized structure requires the use of a conducting substrate which is only slightly separated from the large bond pad by perhaps a thin dielectric layer and resistive (implanted) GaAs. Thus, this structure exhibits a significant bond pad capacitance that typically limits device speeds to around 1 GHz.

Figure 4. The Trench Oxidized VCSEL is currently being pursued by several vendors.

For the Oxide Isolated structure⁷, the oxide layer is completely oxidized everywhere except in the VCSEL aperture. The top view of the device in Fig. 5 shows the via holes etched in the bond pad area to allow complete oxidation under this large area structure prior to the smaller VCSEL mesa. The simplicity of the device fabrication is very enticing, only 2 mask levels are required, one for the mesa etch and one for the metalization. The mesa nature of the structure results in very good oxidation uniformity, however, great care in mask layout and oxidation rate characterization are required to leave the VCSEL aperture conducting while completely oxidizing the rest of the structure. The bond pad capacitance for this structure is the highest of the four structures considered due to the fact that the oxide layer used for electrical isolation is very thin. Unfortunately, the device packagability is the critical limiting factor for this structure. The oxide/semiconductor interface between the oxidized isolation layer and the top DBR is too fragile to withstand the force of wire bonding resulting in intermittent bonding success and low packaging yields.

Figure 5. The Oxide Isolated VCSEL is very simple to fabricate, but exhibits a low packaging yield.

The Mesa Bridged structure is shown in Fig. 6. This structure retains all of the positive attributes of the Mesa Etched devices while placing the bond pad directly on semi-insulating (SI) GaAs resulting in excellent metal adhesion for wire bonding. Note that eliminating the conducting substrate removes most of the capacitance due to the bond pad such that the device response speed should be dominated by the diode junction capacitance. The bridge from the mesa top to the SI substrate is formed by flowing a polymer at elevated temperature prior to the metal deposition. If the interconnect metal is thick enough, the polymer can then be removed forming an air bridge which further reduces the capacitance of the device. Using a semi-insulating substrate necessitates the incorporation of a front side contact for the bottom of the VCSEL which can be a problem for individually addressed 2-D arrays where bringing twice as many leads out of the array becomes difficult. This dual contact configuration is, however, required for both matrix addressable arrays and for high speed wafer probed devices. The most challenging part of this fabrication is spanning the large height difference ($>9\mu$) while maintaining good lithographic fidelity. The wide selection of thick photoresists and developers currently available, however, makes this process straightforward and reproducible.

Figure 6. The Mesa Bridged VCSEL can be fabricated on a semi-insulating substrate providing excellent metal adhesion and low bond pad capacitance.

SUMMARY

The results of this study of VCSEL device structures for high performance prototype applications are summarized in Table 1. The Mesa Planarized and Oxide Isolated structures are undesirable due to intermittent packagability problems resulting in a reduced yield of packaged devices. The Trench Oxidized structure can be used for current VCSEL applications, but future applications will require greater performance. The structure that shows the most promise of providing high performance VCSELs with high yields in large arrays at the highest speeds is the Mesa Bridged structure which is currently utilized for prototype VCSEL development at Sandia.

Table 1. Comparison of VCSEL structure characteristics.

VCSEL Structure	Mesa Planarized	Trench Oxidized	Oxide Isolated	Mesa Bridged
Packagable	No	Yes	No	Yes
Uniform Oxidation	Yes	Maybe	Yes	Yes
Low Capacitance	Yes	No	No	Yes
Reproducible Fabrication	Maybe	Maybe	Yes	Maybe

ACKNOWLEDGEMENTS

Sandia is a multiprogram laboratory operated by Sandia Corporation for the United States Department of Energy under Contract DE-ACO4-94AL85000.

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