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# Semiconductor Product Analysis Challenges Based on the 1999 ITRS



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**Abstract.** One of the most significant challenges for technology characterization and failure analysis is to keep instrumentation and techniques in step with the development of technology itself. Not only are dimensions shrinking and new materials being employed, but the rate of change is increasing. According to the 1999 *International Technology Roadmap for Semiconductors*, "The number and difficulty of the technical challenges continue to increase as technology moves forward."[1] It could be argued that technology cannot be developed without appropriate analytical techniques; nevertheless while much effort is being directed at materials and processes, only a small proportion is being directed at analysis.

Whereas previous versions of the Semiconductor Industry Association roadmap contained a small number of implicit references to characterization and analysis, the 1999 ITRS contains many explicit references. It is clear that characterization is now woven through the roadmap, and technology developers in all areas appreciate the fact that new instrumentation and techniques will be required to sustain the rate of development the semiconductor industry has seen in recent years. Late in 1999, a subcommittee of the Sematech Product Analysis Forum (PAF) reviewed the ITRS and identified a "top-ten" list of challenges which the failure analysis community will face as present technologies are extended and future technologies are developed.

This paper discusses the PAF top-ten list of challenges, which is based primarily on the Difficult Challenges tables from each ITRS working group. Eight of the top-ten are challenges of significant technical magnitude; only two could be considered non-technical in nature. Most of these challenges cut across several working group areas and could be considered common threads in the roadmap, ranging from fault simulation and modeling to imaging small features, from electrical defect isolation to deprocessing. While evolutionary changes can be anticipated fairly easily, revolutionary changes require large multi-faceted research efforts. Each of the ten challenges will be discussed in the context of the roadmap, and specific needs in each area will be given.

## DISCUSSION

Table I summarizes the top-ten technical challenges for characterization and analysis and cites the Technology Working Group Difficult Challenge table in the ITRS to which each relates. Each of the ten technical challenges are discussed below, with some detail given regarding the magnitude of the challenge and possible impact in terms of the roadmap.

### Localization and Electrical Characterization

A large portion of the effort and time expended in failure analysis is in locating where on a die the defect responsible for the failure is located. This includes performing adequate electrical measurements to ensure that the defect found explains the original chip or system-level failure. Several factors contribute to making this a significant challenge for the future. First, obvious factors such as increasing die size and smaller features continue to make defects a smaller proportion of an increasingly large area. Second, decreasing power

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**Table I.** Top-ten challenges for Characterization and Analysis and the sections of the 1999 ITRS that relate to or reference each.

| Product Analysis Challenge | Roadmap Difficult Challenge Table |
|---|---|
| Localization and Electrical Characterization | Design; Process Integration, Devices, and Structures; Front End Processes; Interconnect; Factory Integration; Assembly and Packaging; Modeling and Simulation |
| Deprocessing Techniques for New Materials | Design; Process Integration, Devices, and Structures; Front End Processes; Interconnect; Metrology; Modeling and Simulation |
| System-on-a-Chip | Design; Process Integration, Devices, and Structures |
| Imaging of Small Defects and Structures | Front End Processes; Lithography; Assembly and Packaging; Defect Reduction; Metrology |
| Detection and Characterization of Non-visual Defects | Defect Reduction; Modeling and Simulation |
| Verification and Test | Design; Test and Test Equipment |
| Globally Dispersed Entities as Virtual Factory | Design; Factory Integration |
| Fault Isolation and Simulation Software | Design; Test and Test Equipment |
| Cost of Failure Analysis | Process Integration, Devices, and Structures; Test and Test Equipment; Factory Integration |
| Complexity and Volume of Data | Design; Test and Test Equipment; Factory Integration; Assembly and Packaging; Metrology |

supply voltages and on-chip signal voltages, statistical variations in devices, and devices which will be much more sensitive to interference from neighboring circuit elements will increase the signal to noise requirements for localization tools. Present non-invasive localization and characterization techniques which image a difference in photon emission or temperature at a defect site while power is applied to the chip will not have the sensitivity to discern defective devices from good devices in the future. Invasive techniques such as electron beam probing, photon beam probing and low impedance contact probing may disturb circuit operation to the point of overshadowing the defect that caused the original failure. New techniques that allow non-contact, non-invasive measurement are required. Some progress has been demonstrated in the area of scanning probe measurement of voltage, temperature, etc. but much development work is needed to make these measurements practical on working chips. Currently, physical limitations of scanned probe systems prevent the probe from accessing (often buried) chip internal features while leaving the rest of the chip functional. To measure statistical variations, non-averaging techniques will need to be developed to characterize internal nodes.

## Deprocessing Techniques for New Materials

Materials with features beneficial to electrical performance and manufacturing robustness continue to be sought in the microelectronics industry. While large amounts of effort are expended in development to achieve and control the properties and processing of these materials, similar efforts are required to allow the characterization and metrology community to meet the challenges these new materials bring. For the analysis of chips to be effective, new techniques will have to be developed to allow removal of each new material with selectivity to other materials which are present. Also, preparation techniques will be needed for inspection for physical features which will affect the material's behavior in an application environment (uniformity, voids, adhesion, fill properties, etc.). Particular types of new materials that will require new characterization techniques are low k and high k dielectrics, novel interconnect materials and ferroelectrics. Shrinking feature sizes also will play a role here as any new techniques will require greater precision in preparation to accurately analyze smaller devices and thinner layers.

## System on a Chip

The integration of many elements from an electrical function standpoint will present significant challenges. Embedded memory and embedded logic are the most obvious, however the integration of power devices, rf devices, mixed signal, and micro-mechanical devices will introduce new challenges. These will first be in the

area of electrical and mechanical interaction between these elements where the entire chip must be operating to observe a failure in one element. Also new and presenting a significant challenge to analysts will be the need to measure mechanical features such as wear, stiction, deflection, etc. on active components. Internal measurement of rf devices at frequency will pose problems both in developing detection schemes that can operate at the required frequencies and in being non-invasive so as not to affect circuit operation during measurement.

## Imaging of Small Defects and Structures

Traditionally, inspection to find the cause of a failure has been done with optical and scanning electron microscopy (SEM). These two techniques have been used in a complimentary fashion where a defect was located optically, possibly under a transparent insulating layer, and then, knowing where the defect was, prepared for inspection by SEM. In recent years, as geometries have decreased, optical microscopy has been relied on less and electron microscopy more. One significant limitation of the SEM is that it is a surface or near-surface imaging technique. As geometries and defects get smaller, it will be more and more difficult to prepare samples for SEM so that the structure of interest is in the imaging volume and sufficient contrast can be obtained to discern the defect from its surroundings. New inspection techniques, such as x-ray tomography, need to be brought into the laboratory environment to enable the detection and imaging of defects and structures in a volume of material.

## Detection and Characterization of Non-Visual Defects

With smaller dimension devices, thinner gate oxides, and shallower junctions, many defects will go from being able to be imaged to non-visual in nature. Since the imaging of these defects - which often provides most of the clues towards both their nature and origin - will be impossible, new techniques will be required for this type of analysis. For example in the past, gate oxide defects have typically been due embedded particles or holes. Future gate oxides will fail due to defects such as tunneling, where a defect consists of a local thickness reduction of several atoms, or a small amount of contamination, which changes work function. Other examples are parasitic capacitances, statistical variations in device behavior, and increased sensitivity to trapped charge and mobile ion contamination. Techniques will be required to measure these effects on a small scale and on product devices.

## Verification and Test

In order for a failure to be isolated, the conditions leading to failure often need to be reproduced in the laboratory, including exercising the device at speed and possibly in the same environmental conditions as the end application. This requires complex, engineering intensive, expensive testers to be available to the analyst. These testers must also have the flexibility to alter conditions to make detection of the fault with defect isolation tools possible. In addition to the technical requirements of verification and test, the logistics in accessing and maintaining the large test files for complex die is a formidable task. Another factor in this area is the number of design files that may need to be kept available and accessible at any given time.

## Globally Dispersed Entities as a Virtual Factory

It is becoming more commonplace for the different phases of producing an IC to be done at multiple locations; activities from process development to design, wafer fab, packaging and assembly and test may be done at geographically removed locations. With failure analysis often requiring data from multiple of these entities, the challenge of assembling all the details from chip and process specification to history of the actual failing device in a timely manner is significant. Information must be retained and made available for several years after a particular entity has finished its piece of the effort so that it is available if there are problems to be resolved later in the product life cycle.

## Fault Isolation and Simulation Software

Particularly in complex logic designs, a failing signature at the pin level could be due to a single defect at one of dozens of locations on the chip. In addition, circuit nets cover such a large area, often traversing an entire chip, that all the possibilities may not be able to be considered during analysis. Software is required which will use the fail signature, circuit schematics, and physical design layout to identify the specific possibilities for which physical area of the chip contains a defect or which circuit(s) could be responsible for the failure. This will both narrow the possibilities to make

analysis more efficient and will increase effectiveness by directing the analyst to the correct areas to analyze. Without this type of simulation, and with increasingly complex chip designs, it will be impossible to inspect or to perform fault localization to identify where on a chip further analysis should be concentrated.

## Cost of Failure Analysis

As the cost of building and equipping a wafer fab has increased steadily, so has the cost of obtaining and maintaining the equipment needed for failure analysis. A compounding economic factor in the cost of failure analysis is that the number of tools sold is much smaller than for wafer fab equipment. This makes the cost of individual tools high but, more significantly, makes vendor development in new tools a much higher risk as the smaller demand may make it more difficult to recover development costs. New methods of developing tools, such as industry consortia and university partnerships must be exploited to supply the tools necessary at a reasonable cost.

## Complexity and Volume of Data

Data for performing characterization is often in different formats for different tools, making sequential analysis, from tool to tool, difficult and time consuming. Common formats are needed between testers, fab inspection tools, and characterization tools to ensure an efficient flow of analysis and minimize the possibility of errors due to navigation or wrong data. In addition, the volume of data must be compressed, segmented, or shared in such a fashion that storage and CPU resources are not a limiting factor in characterization.

# CONCLUSION

Ten significant challenges to characterization and failure analysis have been identified from the 1999 International Technology Roadmap for Semiconductors which must be addressed to enable the technology advances the roadmap projects. It has been shown that both new analytical techniques and new tools are needed to enable the development and implementation of the new materials and manufacturing techniques projected in the Roadmap. Also, business challenges related to characterization have been discussed such as dispersed organizations, common data formats, and the cost of developing new characterization and analysis tools.

# REFERENCES

1. Semiconductor Industry Association, *International Technology Roadmap for Semiconductors: 1999 edition.* Austin, TX: International SEMATECH, 1999, p.iii

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