MOS-Gated Thyristors (MCTs) for Repetitive High Power Switching

ABSTRACT

Certain applications for pulse power require narrow, high current pulses for their implementation. This work was performed to determine if MCTs (MOS Controlled Thyristors) could be used for these applications. The MCTs were tested as discharge switches in a low inductance circuit delivering 1 μ s pulses at currents between roughly 3 kA and 11 kA, single shot and repetitively at 1, 10 and 50 Hz. Although up to 9000 switching events could be obtained, all the devices failed at some combination of current and repetition rate. Failure was attributed to temperature increases caused by average power dissipated in the thyristor during the switching sequence. A simulation was performed to confirm that the temperature rise was sufficient to account for failure. Considerable heat sinking, and perhaps a better thermal package, would be required before the MCT could be considered for pulse power applications.

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MOS-Gated Thyristors (MCTs) for Repetitive High Power Switching[#]

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Introduction

Although power semiconductor switches have been used extensively in many power electronics applications, their utilization in pulse power circuitry has remained low. The principle reason has probably been the perception that short pulse operation, particularly under fast turn-on stress, either was not possible at all, or when possible, led to early failure. However, it has been shown [1 - 5] that high peak currents and fast risetimes can be simultaneously obtained for short pulses in discrete semiconductor thyristors, and that the use of single elements in pulse power circuits is feasible for repetitive peak currents up to 10 kA and di/dt values in excess of 20 kA/ms in the burst mode [5]. Repetitive measurements at a 100 Hz repetition rate have also been successfully performed at around 5 kA and 40 kA/ms [6]. The advantage of thyristors over other types of semiconductor switches is their high blocking voltages and very high surge current capacities. There are, however, several types of thyristors, and both the gate turn-off thyristor (GTO) and the MOS-gated thyristor (MCT) are possible competitors; MCTs have, in fact, been proposed as a superior alternative to conventionally gated SCRs for pulsed power.

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Although some comparisons [4] between conventional thyristors and GTOs (and with a thyristor having a GTO geometry [7]) have been made, there have been none with MCTs. This work was done to determine the behavior of MCTs as closing switches (capacitor discharge) under high current, short pulse, and repetitive operation.

Experimental Procedure

A preliminary PSPICE^{®†} design was performed of a ringdown test circuit delivering a 1 μ s pulse (pulse width at half maximum) at peak currents up to at least 10 kA and pulse repetition rates up to 100 Hz. The design required a total capacitance of 15 mF, discharged into a 25 m Ω load, with a total circuit inductance less than 10 nH. The circuit was implemented in a wagon wheel configuration for the lowest parasitic inductance; figures 1a (front) and 1b (back) show the front and back sides of the completed circuit. The load consists of a parallel array of MSW 800 composition wires, isolated from the ground plane by Kapton[®] insulation, and was measured to be around 24 m Ω . Fifteen 1 μ F, 400 VDC ASC capacitors were connected in parallel to obtain the required capacitance. (Although the capacitors were rated only at 400 V, they could be used safely and repetitively, without degradation, up to 600 V.) The device under test is connected in the center of the circuit, where the soldered region is shown, through holes which match the device lead configuration. The circuit was tested by using an MCT itself as a closing switch. Figure 2 illustrates a typical MCT switched current output pulse waveform (shown inverted); some ringing exists, but is not considered to be significant. The total circuit inductance, based on this waveform, is estimated to be between 5 and 7 nH.

[†] Certain commercial products or materials have been identified in order to specify or describe the subject matter of this paper adequately. In no case does this identification imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products or materials are best for the purpose.

The capacitors were charged using an A.L.E. Systems Model 402L constant power charging supply, and the data were taken with an HP Model 54502A digitizing oscilloscope. An HP Model 5315B universal counter was used to count the number of pulses before the device failed. Because of the structure of the test circuit, a measurement of the anode current itself could not be performed, but was inferred by measuring the voltage drop (inverted by the oscilloscope) across the load with a Tektronix P-6009 probe. The anode-cathode voltage waveform was measured using another P-6009 probe.

Fourteen commercially purchased Harris Semiconductor 600 V, 75 A MCTs (MCTA75P60) in the TO-247 package (the MCT technology has now been acquired by SPCO) were tested as discharge switches both single-shot and repetitively at various voltages between 100 and 600 V and frequencies between 1 Hz and 50 Hz. The total die area for the MCTs is 0.65 cm^2 (0.39 in by 0.26 in), around 62% (0.4 cm^2) of which actively participates in conduction when the device is fully turned on. The cell dimensions are 20 mm on a side, and gating is by way of one turn-on gate per nine cells. Four 0.36 mm (0.015 in) wires are stitch-bonded to the active area, with conducting surface metal $4 \text{ }\mu\text{m}$ to $5 \text{ }\mu\text{m}$ thick between the wires. Figure 3 shows a typical device after the packaging epoxy has been stripped off in concentrated boiling sulfuric acid. The external leads did not survive the treatment.

A non-commercial gate driver and driver circuit board were provided by Harris Semiconductor, and used in these measurements. The MCT requires a special gating arrangement, inasmuch as the gate must be driven with a negative voltage relative to its anode, and the driver circuit and the MCT must be isolated from the gating pulse generator (the driver requires an isolated power supply). Figure 4 shows the gate circuit and a part of the optical coupler which provides the isolation from the pulse generator.

Experimental Results

Every MCT eventually failed when the stress became great enough. Some failed single-shot, some under repetitive stress, but no device could successfully be stressed at a pulse current level higher than around 10 kA. All failure modes were similar, independent of the current level or the pulse repetition rate; every anode failed open or resistive, and with only two exceptions, with accompanying failure or degradation of the gate. The results are summarized in Tables 1 and 2. (In Table 1, a single shot is defined such that at least 1 s elapsed between one shot and the next.) The value of di/dt at failure may be estimated from the peak failure current and the time to peak, around 0.5 μ s. Devices 1 through 6 were stressed only single-shot to failure; devices 8 and 9 were stressed single-shot first, then at 1 Hz, to failure; devices 7 and 12 were tested single-shot, then at 10 Hz; devices 11 and 14 were tested single-shot and at 50 Hz; device 13 was tested single-shot, at 10 Hz, then 50 Hz; and device 10 was tested single-shot, and at 1, 5, 10 and 50 Hz to failure.

Discussion of Results

The data indicate that, in the present configuration, the 600 V, 75 A MCT cannot be pulsed repetitively (the issue of configuration will be discussed below). Average peak current densities can vary considerably, depending on how much of the device has actually turned on. It was originally believed that the relatively low duty cycles involved in these measurements argued against average power loss and temperature of the silicon as causes of failure. What was considered more likely was that thermal failure occurred in the very thin metalization between the lead wire bonds. However, when the epoxy packaging material was stripped and the surfaces of the devices examined microscopically, no damage, in general, could be seen. Table 3 summarizes the results of the examination performed by Harris Semiconductor. Inasmuch as no metalization failure was observed, failure caused by the instantaneous high power densities, and

the evolution of high junction temperatures occurring during repetitive switching, was reconsidered as a failure mode, and thermal calculations were performed. (Gate failure is probably a corollary of the junction failure, and was not considered a primary mode.)

The power and energy delivered per pulse were calculated for a device tested at 400 V and a peak current of around 7 kA, pulsed repetitively at 50 Hz. The power pulse was obtained simply by a point-by-point in time multiplication of the voltage across the MCT and current flowing through it at that time, and the energy per pulse was found by numerically integrating the power over time. Figure 5 is a plot of power and energy delivered to the device per pulse. An analytical pulse-by-pulse calculation of the temperature increase in the device was not practical, so a numerical simulation was performed using the silicon chip and TO-220 package thermal models provided in Saber[®] [8, 9]. Heat generation was assumed to occur over the entire thickness of the device (0.036 cm) and the effective area for conduction (0.4 cm^2). The silicon chip thermal model assumes that the specific heat of the silicon remains constant during the pulse sequence, but the thermal resistance of the silicon varies with temperature. This approximation is reasonable within the temperature range used in the simulation, the intrinsic temperature of the silicon (480 K), which was considered to be the failure temperature.

Figure 6 illustrates the power and energy per pulse used in the simulation to represent the measured power function of figure 5. Although the power pulse used for the simulation (shifted in time by 1.0 ms) differs in its shape, the simulated energy delivered to the device, which determines the temperature increase, agrees well with that of the actual pulse.

Two simulations were performed, one assuming that no heat sinking other than the cathode tab was involved (the conditions of the actual experiment), and the other assuming that heat sinking was enhanced. Both simulations were performed over the same time and scale and are shown in figure 7. The top of the envelope of each curve represents the peak temperature of the

junction just after a pulse has been delivered, and the bottom envelope temperature is its value after cooling, just before the next pulse arrives. Both temperatures increase with time; however, failure occurs when the bottom temperature equals the intrinsic temperature. In the case of enhanced heat sinking, the device does not fail after 100 s, or 5000 pulses. In the case of no additional heat sinking (lower curve), the device fails at around 10 s, or 500 pulses. Some heat-sinking effect is evidently present in the actual measurements, inasmuch as several thousand pulses were obtained even at the higher currents, but there is no explanation for the earlier failures, except perhaps incomplete turn-on and greater heat evolution.

Conclusions

Thermal failure resulting from inadequate heat sinking is, if not the primary failure mode, at least a very important mode of failure. It was not possible, under the conditions of the experiment, to provide the extensive heat sinking, which would adequately test this conclusion. Even if additional heat sinking had been available, the early failure results suggest that, under these pulse conditions, another mechanism of failure may exist. If it does, additional heat sinking, although it might improve performance, would not alone qualify these devices for high power, narrow pulse operation.

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Table 1. Total Single Shots at Failure

(Lower currents were obtained at reduced charge voltage)

Device No.	Shots	Highest Current at Failure (kA)	Comments
1	5	10.4	
2	1	2.6	
3	2	9.4	
5	5	10.4	
6	3	2.6	
7	100	7.3	Did not fail
8	100	3.6	Did not fail
9	100	6.8	Did not fail

Table 2. Total Repetitive Shots at Failure

(Lower currents were obtained at reduced charge voltage)

Device No.	Shots	Highest Current at Failure (kA)	Highest Frequency at Failure (Hz)
7	450	4.7	10
8	1	Failed Immediately	1
9	6	6.8	1
10	1000	6.8	50
11	2750	6.8	50
12	9000	6.8	10
13	4505	5.2	50
14	55	5.2	50

Table 3. Results of Microscopic Examination

Device No	Comment
1	No sign of failure; cells were sharply defined even at 160X
2	Epoxy was not fully removed, but the cells which were visible next to the power leads appeared to be undamaged; no sign of failure
3-5	Same as Device 2
6	Same as Device 2, although epoxy removal is not as good
7-8	Same as Device 2
9	Excellent epoxy removal; no signs of failure
11-14	Same as Device 2

Figure Captions

Figure 1. (a) Front view of the completed test circuit, which is 17.1 cm (6.75 in) in diameter; and (b) back view of the test circuit.

Figure 2. Voltage and inverted current waveforms for device number 2 (these are typical for all the devices tested). The device is switched from 400 V and the peak current is 6800 V. The time scale is 2 μ s per large division.

Figure 3. Representative view of a device (number 4) after the epoxy package has been stripped. The two heavy outermost leads on the right are connected to an anode pin; the two adjacent heavy wires are connected to a second anode pin (these were tied together during the measurement); the outermost light wire on the left is the gate connection; and the inner light wire on the left is connected to the anode as the gate return. The cathode pin is connected to the metal backing, and can be seen as the longest pin in the center of the package.

Figure 4. Photograph of the gate drive circuit. The subcircuit on the solid board was provided by Harris Semiconductor. The optical coupler is shown at the left. The two wires at the right conduct the output gate pulse, the light-colored wire going to the gate pin and the dark-colored, to the gate return pin.

Figure 5. Plot of the power and energy for a single pulse (Device Number 2).

Figure 6. Simulated power per pulse (a) and energy per pulse (b) used in the thermal simulation.

Figure 7. Results of simulation of temperature excursions in the MCT with enhanced heat sinking (upper curve) and with no additional heat sinking (lower curve).

Figure 1

a.

b.

Figure 2

Main	Timebase	Delay/Poe	Reference	Mode
	2.00 us/div	0.00000 s	Center	Realtime (NORMAL)
	Sensitivity	Offset	Probe	Coupling
Channel 1	100 V/div	0.00000 V	100.0 :1	dc (1M ohm)
Channel 2	30.0 V/div	0.00000 V	100.0 :1	dc (1M ohm)

Trigger mode : Edge
 On Negative Edge Of Chan2
 Trigger Level
 Chan2 = -0.25000 V (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3

Figure 4

Figure 5

Figure 6

Figure 7