Epitaxially-Grown GaN Junction Field Effect Transistors

L. Zhang,* L. F. Lester,** A. G. Baca,* R. J. Shul,* P. C. Chang,* and C. G. Willison,* U. K. Mishra,*** S. P. Denbaars,*** and J. C. Zolper****

* Sandia National Laboratories, MS 0603, Albuquerque, NM 87185

Tel: (505) 284-3388, Fax: (505) 844-8985, e-mail: zhang@chtm.unm.edu

**Center for High Technology Materials, University of New Mexico, 1313 Goddard SE, Albuquerque NM 87106

***Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106

****Office of Naval Research, Arlington, VA 22217

ABSTRACT

Junction field effect transistors (JFET) are fabricated on a GaN epitaxial structure grown by metal organic chemical vapor deposition (MOCVD). The DC and microwave characteristics of the device are presented. A junction breakdown voltage of 56 V is obtained corresponding to the theoretical limit of the breakdown field in GaN for the doping levels used. A maximum extrinsic transconductance (g_m) of 48 mS/mm and a maximum source-drain current of 270 mA/mm are achieved on a 0.8 μ m gate JFET device at $V_{GS}=1$ V and $V_{DS}=15$ V. The intrinsic transconductance, calculated from the measured g_m and the source series resistance, is 81 mS/mm. The f_T and f_{max} for these devices are 6 GHz and 12 GHz, respectively. These JFETs exhibit a significant current reduction after a high drain bias is applied, which is attributed to a partially depleted channel caused by trapped hot-electrons in the semi-insulating GaN buffer layer. A theoretical model describing

the current collapse is described, and an estimate for the length of the trapped electron region is given.

KEYWORDS: GaN, junction field-effect transistors, velocity saturation, transconductance, cutoff frequency, current collapse, Mott-Gurney law

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

INTRODUCTION

GaN and related materials are highly attractive for high power and high temperature microelectronic devices owing to their large bandgap energy (3.4 eV for GaN), high breakdown field ($\sim 2.7 \times 10^6$ V/cm),¹ high saturation velocity (2.7×10^7 cm/s),² and excellent chemical stability.³ Much effort has been focused on the research and development of various GaN-based field effect transistors (FETs) including metal-semiconductor FETs (MESFETs),^{4,5} modulation-doped FETs (MODFETs),^{6,7,8} metal-insulator-semiconductor FETs (MISFETs),⁹ and ion-implanted junction FETs (JFETs).¹⁰ Recent development of GaN/AlGaN MODFETs has demonstrated impressive DC and rf characteristics, such as high transconductance (400 mS/mm),¹¹ high breakdown voltage (340 V),¹² high output power (>3 W/mm at 18 GHz)¹³ and high cutoff frequency (>50 GHz).^{13,14} High temperature characteristics of GaN MESFETs and MODFETs have also been reported.^{5,15} Compared to MESFETs and MODFETs, JFETs provide a higher gate turn-on voltage and a lower reverse gate leakage current due to a higher built-in potential of the p-n junction gate than the Schottky gate used in MESFETs and MODFETs. This is especially important for high temperature operation. In addition, the junction gate is metallurgically more stable and environmentally more robust than a Schottky gate since it is effectively buried beneath the surface and is subjected to high temperature during crystal growth. Based on this reasoning, JFETs are expected to withstand higher temperature operation than MESFETs and MODFETs. In this paper, we report the fabrication and characterization of epitaxially grown GaN JFETs.

MATERIAL AND FABRICATION

The GaN epitaxial structure used in this work, as shown in fig. 1, was grown by metal organic chemical vapor deposition (MOCVD) on a C-plane sapphire substrate. Ammonia (NH_3), trimethylgallium (TMG), silane (SiH_4), and biscyclopentadienyl-magnesium (Cp_2Mg) were used as precursors for N, Ga, Si, and Mg, respectively. A 200 Å GaN nucleation layer was deposited directly on the sapphire substrate at low temperature, followed by a 4.2 μm semi-insulating (SI) GaN buffer layer grown at 1040 °C in order to obtain a high quality GaN active layer. Next, a 950

Å Si-doped n-GaN channel, a 60 Å undoped GaN, and a 500 Å Mg-doped p-GaN contact layer were grown at 1040 °C. A Mg doping concentration of $5 \times 10^{19} \text{ cm}^{-3}$ was estimated. After the growth, the sample was annealed at 850 °C for 15 sec in a N_2 ambient to drive out the compensating hydrogen and activate the Mg dopant. Hall measurement was used to determine the free carrier concentrations in the p-type, n-type, and SI-GaN epi-layers. According to the doping concentrations, a depletion width of 15 Å at the p-GaN side of the junction was calculated, which was much smaller than the p-GaN thickness. Therefore the effect of the buried n-GaN on the Hall measurement of p-GaN was negligible. The samples used for Hall measurement on n- and SI-GaN were etched down to each corresponding layer using inductively coupled $\text{BCl}_3/\text{Cl}_2/\text{Ar}$ plasmas. The measured free carrier concentration in the p-GaN, n-GaN, and SI-GaN were $1.3 \times 10^{18} \text{ cm}^{-3}$, $2.4 \times 10^{18} \text{ cm}^{-3}$, and $6.1 \times 10^{14} \text{ cm}^{-3}$, respectively. The electron mobility in the n-GaN active layer was $270 \text{ cm}^2/\text{V}\cdot\text{sec}$.

The device fabrication process began with mesa isolation etching in an inductively coupled $\text{BCl}_3/\text{Cl}_2/\text{Ar}$ plasma. Next, a gate metal of Ni/Au/Ni (300 Å/2500 Å/1000 Å) was e-beam evaporated on top of the mesa. The top 1000 Å of Ni served as a mask for the following source-drain etching. The self-aligned source-drain etching was performed in an inductively coupled $\text{BCl}_3/\text{Cl}_2/\text{Ar}$ plasma to remove the p-GaN layer and expose the n-GaN in the source and drain region for ohmic contacts. In order to minimize the ion induced damage to the material, a low DC bias plasma etch recipe was used. The plasma conditions were -75 V DC bias, 500 W ICP source power, 2 mTorr pressure, and 8 sccm/32 sccm/5 sccm $\text{BCl}_3/\text{Cl}_2/\text{Ar}$ flow rate. The etch depth was 760 Å and the etch rate was 950 Å/min. Finally, Ti/Al (300 Å/2500 Å) was e-beam evaporated to form the source and drain ohmic contacts. All metal patterns were defined using a lift-off process. The sample was exposed to an oxygen plasma to remove residual photoresist followed by a 15 seconds $\text{NH}_4\text{OH}:\text{DI}$ (1:20) rinse immediately prior to metal evaporation to ensure good contact between the metal and semiconductor. Post-metallization annealing was not performed. A transmission line method (TLM) measurement showed an as-deposited source and drain ohmic contact resistance of $4.2 \text{ } \Omega\cdot\text{mm}$, a specific contact resistance of $5 \times 10^{-5} \text{ } \Omega\cdot\text{cm}^2$, and a sheet

resistance of 4700 Ω /square. These values were relatively large, possibly due to the thin n-GaN active layer and overetched source and drain region. Several different size devices were fabricated for this study, with gate lengths of 0.8 and 1.2 μm , and gate widths of 50, 100, 150, and 200 μm .

DC AND RF RESULTS AND DISCUSSION

Fig. 2 shows the drain current (I_{DS}) as a function of drain-source voltage (V_{DS}) up to 15 V for various gate biases (V_{GS}). The gate length and the gate width of the measured device are 0.8 μm and 50 μm , respectively. The spacing between source and drain is 3 μm and the gate-source spacing is about 1 μm . At $V_{\text{GS}}=1$ V, a maximum I_{DS} of 270mA/mm is obtained with a knee voltage of approximately 8 V. The channel is completely pinched off at a threshold voltage of $V_{\text{GS}}=-8$ V, with an $I_{\text{DS}}=210$ $\mu\text{A}/\text{mm}$ at $V_{\text{DS}}=15$ V. A gate-drain diode reverse breakdown voltage of 56 V is measured. This value is relatively small compared to the reported breakdown voltage on GaN MESFETs and MODFETs,^{4,12} but this result is not intrinsic to JFET design. Assuming all of the applied gate voltage is dropped across the p-n junction, a depletion width of 2200 $\text{\AA}$ and a breakdown field of 2.5×10^6 V/cm is calculated. The fact that the breakdown field reaches the theoretical limit of 2.7×10^6 V/cm for GaN indicates that the low breakdown voltage of the gate is primarily due to the high doping concentration of the n-GaN. Therefore a lower doping concentration in n-GaN active layer should improve the breakdown voltage by effectively increasing the junction depletion width. The forward turn-on voltage of the gate diode was ~ 1 V using a 1 mA/mm current criterion. This value is only 30% of the bandgap energy of GaN. The cause of this low turn-on is not known at present but may result from defect levels in the GaN.

Fig. 3 shows the drain current and extrinsic transconductance (g_m) as a function of applied gate bias at $V_{\text{DS}} = 12$ V. A maximum g_m of 48 mS/mm is obtained at $V_{\text{GS}}=1$ V and $V_{\text{DS}} > 12$ V. This value is 7 times larger than the previously reported value for ion implanted GaN JFETs by Zolper, et. al.,¹⁰ probably due to a higher electron mobility and higher electron concentration in epitaxially

grown n-GaN than ion-implanted n-GaN. The measured source and drain resistances (R_s and R_D) are 8.5 Ω -mm and 13 Ω -mm, respectively as determined by the end resistance measurement technique.¹⁶ The difference between the R_s and R_D is attributed to the alignment of the gate closer to the source than the drain. Based on these results, an intrinsic transconductance (g_{m0}) of 81 mS/mm is estimated using the relationship $g_m = g_{m0} / (1 + g_{m0} R_s)$.

The microwave performance of the JFETs was characterized using an HP 8510 network analyzer, and the short circuit current gain (H_{21}), unilateral gain (U), maximum stable gain (G_{ms}), and maximum available gain (G_{ma}) were obtained from the small-signal S-parameters. Fig. 4 shows the H_{21} , U , G_{ms} , and G_{ma} of a 0.8 μm x 100 μm JFET as a function of frequency for $V_{DS}=15$ V and $V_{GS}=0$ V. A unity current-gain cutoff frequency (f_T) of 6 GHz and a maximum frequency (f_{max}) of 12 GHz are obtained. The measured f_T remains constant over the range of $V_{GS}=-1$ V to 1 V, implying that no parasitic bipolar action is present in the device operation under these conditions. These values are comparable to the reported f_T and f_{max} on GaN MESFETs and GaN/AlGaN MODFETs with a similar gate length.¹⁷⁻²⁰ The intrinsic f_T of our JFETs would be higher by taking into account the large source and drain resistance, as pointed out by Tasker and Hughes,²¹ and by extracting the parasitic gate pad capacitance that does not scale with gate width.

Similar to what Binari and co-workers have reported on GaN MESFETs,⁴ a significant reduction in I_{DS} occurs in our JFETs after the device is subjected to a high V_{DS} . Two sets of I_{DS} - V_{DS} curves, both measured up to $V_{DS}=40$ V under white-light illumination, are shown in Fig. 5. The solid curves are measured individually with 5 min of illumination before each curve is taken while the dashed curves are measured in rapid succession. The upper dashed trace ($V_{GS}=1$ V) is nearly identical to the upper solid trace since they are both subjected to a long illumination. The subsequent dashed curves ($V_{GS}\leq 0$) demonstrate a significant reduction in I_{DS} at $V_{DS} < 25$ V. This current collapse effect is not significant unless V_{DS} is increased above 20V. For rapidly measured data, it is also noted that the output conductance is higher and remains relatively constant between the knee voltage and $V_{DS}=25$ V, the bias above which illumination or measurement speed makes little difference in I_{DS} .

As proposed by Binari,⁴ the reduction in I_{DS} is attributed to high-field injection and subsequent trapping of electrons in the SI-GaN. This trapped charge depletes part of the active channel from the backside as shown in fig. 6. However, we believe that the trapped electrons are not uniformly distributed under the channel. Most likely, they are shifted towards the drain side where the electrical field is the highest. The I_{DS} - V_{DS} data in fig. 7 is intended to demonstrate this non-uniform distribution of trapped carriers. The I-V curves are taken at $V_{GS}=0V$ and measured in the dark to prevent the trapped electrons from being released. The solid curve is taken after long illumination to form a normal I_{DS} - V_{DS} curve for comparison and to trap electrons in the SI-GaN. Compared to Binari's MESFETs in which the trapped electrons are readily released under illumination, a minimum of 2 min illumination is required to release the trapped electrons in our JFETs. The dotted curve, measured immediately after the solid one, shows a current collapse due to trapped electrons predominantly on the drain side of the channel. Next, a V_{DS} scan with reversed source and drain traps more electrons on the source side. The source and drain are then switched back to their initial configuration and the dashed curve is measured. With both sides of the channel partially depleted by trapped electrons, the dashed curve shows a ~10% reduction in the I_{DS} at $V_{DS}=40 V$ compared to the dotted curve.

To further understand the effect that the trapped electrons have on the channel region, I_{DS} is analyzed according to the device picture in fig. 6. At low drain bias ($<5 V$), the transistor is below saturation and the current is limited by R_s , R_D , and the channel resistance, R_{CH} . Since the channel is partially depleted by the trapped electrons, a lower channel conductance is obtained, resulting in a smaller slope in the dashed I_{DS} - V_{DS} curves as compared to the solid ones in fig. 5. Above the knee voltage, it is assumed that the channel region consists of a velocity-saturated section in parallel with a space-charge-limited current region formed by electrons trapped in the GaN buffer. The latter current flow mechanism is evidenced by the nearly constant output conductance between the knee voltage and $V_{DS}=25 V$ and is described by the Mott-Gurney law including velocity saturation.¹⁶

$$I_{DS} = 2Wd_{dep} \frac{\epsilon v_{sat} (V_{DS} - V_{DSat})}{L_{dep}^2} \quad (1)$$

where W is the gate width, ϵ is the dielectric constant, and d_{dep} and L_{dep} (shown in fig. 6) are the length and width, respectively, of the depletion region due to trapped electrons. The assumption of velocity saturation is justified because an average electrical field of 100 kV/cm, which is close to the field corresponding to the peak electron drift velocity in GaN,⁷ is found from a $V_{DSat}=8$ V and a $0.8 \mu\text{m}$ gate length. Referring again to fig. 5, the rapid increase in the I_{DS} of the collapsed curves at $V_{DS}=25\text{V}$ may indicate a local breakdown of the space charge region. Therefore, regardless of illumination at $V_{DS} \geq 25\text{V}$, I_{DS} is limited by an undepleted, velocity-saturated region of the channel on the drain side of the space charge layer as illustrated in fig. 6.

Next, a theoretical model is described that permits an estimate of L_{dep} using measured DC I-V characteristics. The output conductance for $V_{DS} > V_{DSat}$ can be found by differentiating (1),

$$g_d \equiv \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{2Wd_{dep} \epsilon v_{sat}}{L_{dep}^2} \quad (2)$$

and the thickness, d_{dep} , is determined from the following equation which uses the difference in I_{DS} at the knee voltage before and after current collapse:

$$d_{dep} = \frac{\Delta I_{DS}}{qN_D W v_{sat}} \cdot \frac{1}{1 - g_m R_s} \quad (3)$$

where $I_{DS} = qN_D W h v_{sat}$ for a velocity saturated FET is used, and the $1/(1 - g_m R_s)$ term accounts for the reduction in I_{DS} due to the source resistance. Then L_{dep} is found by substituting eq. (3) into eq. (2),

$$L_{dep} = \sqrt{\frac{2\epsilon \Delta I_{DS}}{qN_D g_d} \cdot \frac{1}{1 - g_m R_s}} \quad (4)$$

Assuming an ϵ of $9.5\epsilon_0$,²² an L_{dep} of $0.14 \mu\text{m}$ is estimated by fitting the $V_{GS}=0$ V curves to the above equation. The fact that L_{dep} is much smaller than the gate length corroborates the assumption above that the trapped electrons in the buffer are non-uniformly distributed. It is much more

difficult to estimate d_{dep} since we do not have an accurate value for v_{sat} from the f_t measurement due to the series resistances.

CONCLUSION

In summary, JFETs were fabricated on an epitaxially grown GaN p-n junction. These devices exhibited excellent pinch-off and a breakdown voltage that agreed with theoretical predictions. An extrinsic transconductance of 48 mS/mm was achieved with a maximum I_{DS} of 270 mA/mm. The microwave measurement showed an f_t of 6 GHz and an f_{max} of 12 GHz. A breakdown voltage of 56 V was achieved, although by reducing the doping concentration in the n-GaN active channel, a higher breakdown voltage can be expected. Drain current collapse was observed in these devices after a high drain bias was applied. This effect can be explained by the formation of a depleted layer at the channel-buffer interface due to trapped electrons. Assuming saturated velocity conditions, an estimate of the length of this space-charge region was made based on the Mott-Gurney law and the extent of the current decrease after high V_{DS} was applied.

ACKNOWLEDGEMENT

The authors gratefully acknowledge Dr. T. E. Zipperian for helpful technical discussion and Dr. T. Newell for technical support. This work was supported in part by the National Science Foundation CAREER Grant ECS-9501785. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-ACO4-94AL85000.

FIGURE CAPTIONS

- Fig. 1: Schematic of GaN JFET epi-layer structure grown by MOCVD.
- Fig. 2: Drain current as a function of drain voltage up to 15 V for a 0.8 μm gate GaN JFET. The gate bias starts at 1 V with -1 V steps. A maximum I_{DS} of 270 mA/mm was obtained at $V_{\text{GS}}=1$ V. The channel is completely pinched-off at $V_{\text{GS}}=-8$ V, with an $I_{\text{DS}}=210 \mu\text{A/mm}$ at $V_{\text{DS}}=15$ V.
- Fig. 3: The extrinsic transconductance and the drain current as a function of gate bias at V_{DS} of 12V. A maximum transconductance of 48 mS/mm was obtained at $V_{\text{GS}}=0$ V and $V_{\text{DS}}>12$ V.
- Fig. 4: Current gain (h_{21}), unilateral gain (U), maximum stable gain (G_{ms}), and maximum available gain (G_{ma}) as a function of frequency for a 0.8 $\mu\text{m} \times 100 \mu\text{m}$ GaN JFET at $V_{\text{DS}}=15$ V and $V_{\text{GS}}=0$ V. A cut-off frequency of 6 GHz and a maximum frequency of 12 GHz were obtained from this measurement.
- Fig. 5: $I_{\text{DS}}-V_{\text{DS}}$ characteristic showing the drain current collapse at $V_{\text{DS}}< 25$ V due to a partially depleted channel by electrons trapped in the SI-GaN. The solid curves were measured individually with 5 min of illumination to release trapped electrons in the SI-GaN. The dashed ones were measured in rapid recession.
- Fig. 6: Schematic illustration of the current flow mechanism under the gate with the channel partially depleted by the electrons trapped in the SI-GaN. h is the channel opening and d_{dep} and L_{dep} are the length and width, respectively, of the depletion region due to trapped electrons in the buffer.
- Fig. 7: $I_{\text{DS}}-V_{\text{DS}}$ curves measured (a) after long illumination to ensure no pre-existing trapped electrons, (b) after a high V_{DS} is applied to the device, and (c) with the same source and drain configuration as (b) but following a scan with the source and drain reversed. The measurements were taken in the dark to prevent the trapped electrons from being released, and the gate bias was set to 0 V.

References

1. V. A. Dmitriev, K. G. Irvine, C. H. Carter Jr., I. Kuznetsov, and E. V. Kalinina, "Electric breakdown in GaN p-n junctions", *Appl. Phys. Lett.*, vol. 68, no. 2, pp. 229-231, Jan. 1996.
2. B. Gelmont, K. Kim, and M. S. Shur, "Monte Carlo simulation of electron transport in gallium nitride", *J. Appl. Phys.*, vol. 74, no. 3, pp. 1818-1821, Aug. 1993.
3. S. N. Mohammad, A. Salvador, and H. Morkoç, "GaN and related materials", *Proc. IEEE* **83**, 1306, 1995.
4. S. C. Binari, W. Kruppa, H. B. Dietrich, G. Kelner, A. E. Wickenden, and J. A. Freitas JR, "Fabrication and Characterization of GaN FETs", *Solid-St. Electron.*, vol. 41, no. 10, pp. 1549-1554, Oct. 1997.
5. S. Yoshida and J. Suzuki, "Reliability of metal semiconductor field-effect transistor using GaN at high Temperature", *J. Appl. Phys.*, vol. 84, no. 5, pp. 2940-2942, Sep. 1998.
6. U. K. Mishra, Y. F. Wu, B. P. Keller, S. Keller, and S. P. Denbaars, "GaN Microwave Electronics", *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 6, pp. 756-760, June 1998.
7. M. A. Khan, Q. Chen, M. S. Shur, B. T. Dermott, J. A. Higgins, J. Burm, W. J. Schaff, and L. F. Eastman, "GaN Based Heterostructure for High Power Devices", *Solid-St Electron.*, vol. 41, no. 10, pp. 1555-1559, Oct. 1997.
8. Z. F. Fan, S. N. Mohammad, O. Aktas, A. E. Botchkarev, A. Salvador, and H. Morkoç, "Suppression of Leakage Currents and Their Effect on the Electrical Performance of AlGaIn/GaN Modulation Doped Field-Effect Transistors", *Appl. Phys. Lett.*, vol. 69, no. 9, pp. 1229-1231, Aug. 1996.
9. S. C. Binari, L. B. Rowland, G. Kelner, W. Kruppa, H.B. Dietrich, K. Doverspike, and D. K. Gaskill, in *Proceedings of 1994 International Symposium on Compound Semiconductors*, San Diego, CA, pp. 492-496, Sept. 1994 (Institute of Physics, Bristol, U. K. 1995).

-
10. J. C. Zolper, R. J. Shul, A. G. Baca, R. G. Wilson, S. J. Pearton, R. A. Stall, “Ion-implanted GaN Junction Field Effect Transistor”, Appl. Phys. Lett., vol. 68, no. 16, pp. 2273-2275, April 1996.
 11. C. H. Chen, S. Keller, G. Parish, R. Vetury, P. Kozodoy, E. L. Hu, S. P. Denbaars, U. K. Mishra, and Y. F. Wu, “High-Transconductance Self-Aligned AlGaIn/GaN Modulation-Doped Field-Effect Transistors”, Appl. Phys. Lett., vol. 73, no. 21, pp. 3147-3149, Nov. 1998.
 12. Y. F. Wu, B. P. Keller, D. Kapolnek, P. Kozodoy, S. P. Denbaars, and U. K. Mishra, “Very high breakdown voltage and large transconductance realized on GaN heterojunction field effect transistors” Appl. Phys. Lett., vol. 69, no. 10, pp.1438-1440, Sep. 1996.
 13. Y. F. Wu, B. P. Keller, P. Fini, J. Puskas, M. Le, N. X. Nguyen, C. Nguyen, D. Widmer, S. Keller, S. P. Denbaars, and U. K. Mishra, “Short-Channel Al_{0.5}Ga_{0.5}N/GaN MODSFETs with Power Density >3 W/mm at 18 GHz”, Electron. Lett., vol. 33, no. 20, pp. 1742-1743, Sep. 1997.
 14. L. F. Eastman, K. Chu, W. Schaff, M. Murphy, N. G. Weimann, and T. Eustis, “High Frequency AlGaIn/GaN MODFET’s”, MRS Internet J. Nitride Semicond. Res., vol. 2, art. 17, 1997.
 15. O. Aktas, Z. F. Fan, S. N. Mohammad, A. E. Botchkarev, and H. Morkoc, “High temperature characteristics of AlGaIn/GaN modulation doped field-effect transistors”, Appl. Phys. Lett., vol. 69, no. 25, pp. 3872-3874, Dec. 1996.
 16. M. Shur, *Physics of Semiconductor Devices*, Prentice Hall, Englewood Cliffs, NJ, 1990.
 17. Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbars, and U. K. Mishra, “Measured Microwave Power Performance of AlGaIn/GaN MODFET”, IEEE Electron Device Lett., vol. 17, no. 9, pp. 455-457, Sep. 1996.

-
18. O. Aktas, Z. F. Fan, A. Botchkarev, S. N. Mohammad, M. Roth, T. Jenkins, L. Kehias, and H. Morkoç, "Microwave Performance of AlGaIn/GaN Inverted MODFET's", IEEE Electron Device Lett., vol. 18, no. 6, pp. 293-295, June 1997.
 19. S. C. Binari, J. M. Redwing, G. Kelner, and W. Kruppa, "AlGaIn/GaN HEMTs Grown on SiC Substrate", Electron. Lett., vol. 33, no.3, pp.242-243, Jan. 1997.
 20. Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, P. Kozodoy, S. P. Denbarrs, and U. K. Mishra, "High Power AlGaIn/GaN HEMTs for Microwave Applications", Solid-St. Electron., vol. 41, no. 10, pp.1569-1574, 1997.
 21. P. J. Tasker and B. Hughes, "Importance of Source and Drain Resistance to the Maximum f_T of Millimeter-Wave MODFET's", IEEE Electron Device Lett., vol. 10, no. 7, pp. 291-293, July 1989.
 22. A. S. Barker, Jr. and M. Ilegems, "Infrared Lattice Vibrations and Free-Electron Dispersion in GaN", Phys. Rev. B7, no. 2, pp. 743-750, Jan. 1973.