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SPICE Level 3 and BSIM3v3.1 characterization of monolithic integrated CMOS-MEMS devices

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ABSTRACT

The monolithic integration of MicroElectroMechanical Systems (MEMS) with the driving, controlling, and signal processing electronics promises to improve the performance of micromechanical devices as well as lower their manufacturing, packaging, and instrumentation costs. Key to this integration is the proper interleaving, combining, and customizing of the manufacturing processes to produce functional integrated micromechanical devices with electronics. We have developed a MEMS-first monolithic integrated process that first seals the micromechanical devices in a planarized trench and then builds the electronics in a conventional CMOS process.

To date, most of the research published on this technology has focused on the performance characteristics of the mechanical portion of the devices, with little information on the attributes of the accompanying electronics. This work attempts to reduce this information void by presenting the results of SPICE Level 3 and BSIM3v3.1 model parameters extracted for the CMOS portion of the MEMS-first process. Transistor-level simulations of MOSFET current, capacitance, output resistance, and transconductance versus voltage using the extracted model parameters closely match the measured data. Moreover, in model validation efforts, circuit-level simulation values for the average gate propagation delay in a 101-stage ring oscillator are within 13-18% of the measured data. In general, the BSIM3v3.1 models provide improved accuracy over the SPICE Level 3 models. These results establish the following: (1) the MEMS-first approach produces functional CMOS devices integrated on a single chip with MEMS devices and (2) the devices manufactured in the approach have excellent transistor characteristics. Thus, the MEMS-first approach renders a solid technology foundation for customers designing in the technology.

Keywords: Micromechanics, CMOS, CMP, Intelligent Micromachines, Spice Models, SPICE Level 3, BSIM3v3.1

1. MONOLITHIC INTEGRATION OF MICROELECTRONICS AND MICROMECHANICS

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Structures (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer¹, which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. In another approach, researchers at Berkeley² have developed a MEMS-last modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing.

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, we have developed a MEMS-first monolithic integrated process.^{3,4} This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. Then, a high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics

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processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal processing associated with fabrication of the microelectronic processing does not adversely affect the mechanical properties of the polysilicon structures. These wafers with the completed, planarized micromechanical devices are then used as starting material for conventional CMOS processes. A cross-section of the MEMS-first monolithic integrated technology is shown in Figure 1.

This MEMS-first approach is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. In our facility, both 2 μm and 0.5 μm CMOS technologies on 6 inch wafers are available; the 2 μm process is being used as the development vehicle for the integrated technology. The CMOS process presented in this study is a standard 5-volt, twin-tub process with nominal 2 μm NMOS and PMOS gate lengths. The technology uses one level of metal and has lightly doped drains (LDD) for the NMOS transistors to reduce hot electron effects.

Figure 1. Cross-section of the MEMS-first monolithic integrated technology

To date, most of the research published on this technology has focused on the performance characteristics of the mechanical portion of the devices, with little information on the attributes of the accompanying electronics.^{3,4} This work attempts to reduce this information void by presenting the results of a set of SPICE Level 3⁵ and BSIM3v3.1⁶ model parameters extracted for the CMOS portion of the MEMS-first process. Both SPICE Level 3 and BSIM3v3.1 models are considered in this study because the SPICE Level 3 model is a legacy, semi-empirical model that is widely used for circuit design while BSIM3v3.1 comprises the latest physics-based, deep submicron model preferred by many circuit designers.

2. PARAMETER EXTRACTION SCHEME

Parameter extraction is an important part of the circuit design process and many different extraction schemes have been developed.^{5,7} The appropriate scheme depends on the model, the options available in the software being used for the model extraction, and on the way the model is to be used. In this study, based on the properties of the BSIM3v3.1 and SPICE Level 3 models, a combination of local and global optimization and group device extraction strategies are utilized. In the group device extraction strategy, measured data from a collection of different device geometries is used to incorporate the effects of varying lengths and widths directly into one set of model parameters. Clearly, design simulation work is made more efficient when each device geometry does not require a separate set of model parameters to adequately describe the behavior of the transistor. Optimization strategies refine a particular subset of the model parameters by optimally fitting a

prescribed range of the measured data (e.g., minimizing a least-squares error between the measured and calculated data over a chosen region). The software package used to accomplish these tasks was the SILVACO UTMOST III tool.

The BSIM3v3.1 dc parameter model extraction scheme requires an orthogonal set of large and small geometry MOS transistor devices with varying lengths and widths. The large devices are used to extract parameters which are independent of short/narrow channel effects and parasitic resistance while the devices with fixed large widths and varying lengths are used to extract parameters related to short channel effects. Similarly, devices with fixed long lengths and varying width are used to extract parameters which are related to narrow channel effects. Based on these requirements, various transistor test structures for extracting dc model parameters were manufactured in the MEMS-first process. The transistor geometries, marked with an “X”, are shown in Table 1. Various capacitance test structures for extracting ac model parameters and a 101-stage ring oscillator for validating the extracted model parameters were also manufactured. A schematic of the ring oscillator is shown in Figure 2. These manufactured devices were also used for the SPICE Level 3 model parameter extraction and evaluation.

Table 1. Device geometries used for parameter extraction

Length (microns) →					Width (microns) ↓
2	6	10	20	30	30
X	X	X	X	X	30
				X	20
	X			X	10
X		X		X	6
X				X	2

Figure 2. A schematic of the ring oscillator

3.0 DEVICE MEASUREMENT AND CHARACTERIZATION

Before any model parameters were extracted, key input process parameters were determined using various techniques. These techniques and the resulting parameters are listed in Table 2. Transistor current, output resistance, and transconductance versus voltage characteristics were then measured for the various device geometries given in Table 1 using a HP4062 parametric tester. Similarly, transistor capacitance-voltage (C-V) characteristics were measured on the various capacitance test structures using a HP4280 C-V meter. In addition, the oscillation frequency of the ring oscillator was measured in response to power supply voltages of 2, 3, 4, 5, and 6-Volts on a HP4062 tester.

The data collected from the ac and dc measurements were imported into UTMOST III and the dc and ac model parameters for SPICE Level 3 and BSIM3v3.1 were extracted using the global optimization and group device extraction strategies mentioned above. Similarly, the data collected from the frequency-voltage response of the oscillator was compared to the response simulated in SABER (and in PSPICE) using the extracted SPICE Level 3 and BSIM3v3.1 model parameters.

Table 2. Key input process parameters

Parameter		NMOS	PMOS	Notes
TOX	Gate oxide thickness (m)	2E-8	2E-8	From process and capacitance measurements
XJ	Junction depth (m)	3E-7	4E-7	From cross-section junction staining
LD	Lateral diffusion (m)	7.5E-8	3.4E-7	From cross-section junction staining
NCH	Channel doping concentration (/cm ³)	1.6E17	2.1E16	From spreading resistance measurements
NSUB	Substrate doping concentration (/cm ³)	2.5E16	1.0E15	From spreading resistance measurements

For the SPICE Level 3 dc parameter extraction, it was impossible to find a single set of model parameters that fit all the transistor geometries. However, four sets of model parameters were found that provided close agreement between the simulated and measured characteristics for the four groups of geometries listed in Table 3. Figure 3 shows an example comparison of the measured and simulated drain current (I_D) versus drain-source voltage (V_{DS}) characteristics for the 30/30 NMOS transistor (group 1) back-biased at 0 and -3 volts, respectively. The figure also shows similar comparisons for the output resistance (R_{DS}) versus V_{DS} . Note that measured I_D vs. V_{DS} characteristics fit the simulated ones well for varying gate-source voltages (V_{GS}) and back biases. Good fits are also obtained between the measured and simulated R_{DS} vs. V_{DS} characteristics in the triode region, but there was less agreement in saturation. These results in saturation are due to limitations in the SPICE Level 3 model and could result in some inaccuracies in analog circuit designs using these models.

Table 3. SPICE Level 3 transistor geometry groups

Transistor Geometry Groups	Geometries (Width/Length in Microns)
Group 1	30/30, 30/20, 30/10, 30/6, 20/30, 10/30
Group 2	30/2, 6/2
Group 3	6/30, 2/30, 10/6, 6/10
Group 4	2/2

Run by :Buddy
Process:CMOS5B
Temp. :27

Lot: MM12801A
Waf: Wafer03
Die: X-1Y2

File: L3_30-30_IDVD+RD.ps

Figure 3. Comparisons of the measured and SPICE Level 3 simulated drain current (I_{DS}) and output resistance (R_{DS}) versus drain-source voltage (V_{DS}) for the 30/30 NMOS back-biased at 0 and -3 volts, respectively.

Figure 4 shows an example comparison of the measured and simulated I_D vs. V_{GS} for V_{DS} at 0.1 and 5 volts, respectively. The figure also includes similar plots of the transconductance (g_m) versus V_{GS} . Note that the measured I_{DS} vs. V_{GS} and g_m versus V_{GS} characteristics fit the simulated ones reasonably well for varying drain-source voltages and back biases both in the triode and saturated regions. Good fits between the measured and simulated C-V characteristics were also obtained for the SPICE Level 3 model.

Run by :Buddy Lot: MM12801A
 Process:CMOS5B Waf: Wafer03
 Temp. :27 Die: X-172

File: L3_30-30_IDVG+GM.ps

Figure 4. Comparisons of the measured and SPICE Level 3 simulated drain current (I_{DS}) and transconductance (g_m) versus gate-source voltage (V_{GS}) for the 30/30 NMOS back-biased at 0.1 and 5 volts, respectively.

For the BSIM3v3.1 dc parameter extraction, a single set of model parameters was found that fit all the transistor geometries. Figure 5 shows an example comparison of the measured and simulated I_{DS} vs. V_{DS} characteristics for the 30/30 NMOS transistor back-biased at 0 and -3 volts, respectively. The figure also shows similar comparisons for the R_{DS} versus V_{DS} characteristics. Note that the measured I_{DS} vs. V_{DS} characteristics fit the simulated ones well for varying gate-source voltages (V_{GS}) and back biases. Excellent fits are also obtained between the measured and simulated R_{DS} vs. V_{DS} characteristics in the triode region, with improved fits over the SPICE Level 3 model in saturation.

Run by :Buddy
 Process:CMOS5B
 Temp. :27

Lot: MM12801A
 Waf: Wafer03
 Die: X-1Y2

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Figure 5. Comparisons of the measured and BSIM3v3.1 simulated drain current (I_{DS}) and output resistance (R_{DS}) versus drain-source voltage (V_{DS}) for the 30/30 NMOS back-biased at 0 and 3 volts, respectively.

Figure 6 shows an example comparison of the measured and simulated I_{DS} vs. V_{GS} characteristics for the 30/30 NMOS transistor back-biased at 0.1 and 5 volts, respectively. The figure also shows similar comparisons for the g_m versus V_{GS} characteristics. Note that the measured I_{DS} vs. V_{GS} and g_m versus V_{GS} characteristics fit the simulated ones well for varying drain-source voltages and back biases both in the triode and saturated regions. Good fits between the measured and

simulated C-V characteristics are also obtained for the BSIM3v3.1 model. Tables 4 and 5 provide a comparison of some important SPICE Level3 and BSIM3v3.1 ac and dc parameter values for NMOS and PMOS transistors, respectively.

Run by :Buddy
Process:CMOS5B
Temp. :27

Lot: MM12801A
Waf: Wafer03
Die: X-1Y2

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Figure 6. Comparisons of the measured and BSIM3v3.1 simulated drain current (I_{DS}) and transconductance (g_m) versus gate-source voltage (V_{GS}) for the 30/30 NMOS back-biased at 0.1 and 5 volts, respectively.

Table 4. A comparison of the extracted SPICE Level 3 and BSIM3v3.1 ac and dc model parameters for NMOS transistors

Model Parameters	BSIM3v3.1	SPICE Level 3 (Group 1)	SPICE Level 3 (Group 2)	SPICE Level 3 (Group 3)	SPICE Level 3 (Group 4)
Threshold voltage (VTO) [V]	1.16	1.07	1.31	1.07	1.09
Surface mobility (U0) [$\text{cm}^2/\text{V} \cdot \text{Sec}$]	573	455.8	537.95	466.65	480.6
Oxide thickness (TOX) [m]	2E-8	2E-8	2E-8	2E-8	2E-8
Non-LDD gate-source overlap capacitance (CGSO) [F/m]	1.0E-12	2.53E-10	2.53E-10	2.53E-10	2.53E-10
Non-LDD gate-drain overlap capacitance (CGDO) [F/m]	1.0E-12	2.53E-10	2.53E-10	2.53E-10	2.53E-10
Gate-bulk overlap capacitance (CGBO) [F/m]	1.1E-10	1.1E-10	1.1E-10	1.1E-10	1.1E-10
Junction capacitance (CJ) [F/m^2]	8.14E-5	8.14E-5	8.14E-5	8.14E-5	8.14E-5

Table 5. A comparison of the extracted SPICE Level 3 and BSIM3v3.1 ac and dc model parameters for PMOS transistors

Model Parameters	BSIM3v3.1	SPICE Level 3 (Group 1)	SPICE Level 3 (Group 2)	SPICE Level 3 (Group 3)	SPICE Level 3 (Group 4)
Threshold voltage (VTO) [V]	-1.02	-.0965	-0.98	-0.935	-0.95
Surface mobility (U0) [$\text{cm}^2/\text{V} \cdot \text{Sec}$]	213.9	208.4	164.3	183.2	133.3
Oxide thickness (TOX) [m]	2E-8	2E-8	2E-8	2E-8	2E-8
Non-LDD gate-source overlap capacitance (CGSO) [F/m]	1.93E-10	5.15E-10	5.15E-10	5.15E-10	5.15E-10
Non-LDD gate-drain overlap capacitance (CGDO) [F/m]	4.2E-10	5.15E-10	5.15E-10	5.15E-10	5.15E-10
Gate-bulk overlap capacitance (CGBO) [F/m]	1.1E-10	1.1E-10	1.1E-10	1.1E-10	1.1E-10
Junction capacitance (CJ) [F/m^2]	3.6E-4	3.6E-4	3.6E-4	3.6E-4	3.6E-4

4.0 RING OSCILATOR SIMULATION RESULTS

Once all the model parameters are extracted, it is necessary to verify the accuracy of the entire model in the transient mode of operation. Such validations were performed in the SABER and PSPICE simulators using a 101-stage ring oscillator to determine the average gate propagation delay at power supply voltages of 2, 3, 4, 5, and 6-Volts. Figure 7 shows a comparison of the measured gate propagation delays as a function of bias versus those simulated using the extracted SPICE Level 3 and BSIM3v3.1 model parameters. The results indicate that the average gate propagation delays from the SPICE Level 3 simulations are within 18% of the measured data. For the BSIM3v3.1 simulations, the simulated values are within 13% of the measured ones.

The smaller gate propagation delays obtained from the Level 3 simulation compared to the BSIM3 evaluation are due in part to the fact that the BSIM3 transistor ac and dc models are more accurate and complete than those in SPICE Level 3. For example, the BSIM3v3.1 model considers both LDD and non-LDD overlap and fringe capacitances which are not modeled in the Level 3 model. In addition, Level 3 model parameters were chosen from group 2, while the actual ring oscillator transistors sizes were 12/2 and 24/2 for NMOS and PMOS, respectively (See Table 3). Also, the higher gate propagation delays obtained from measurements could be due in part to additional parasitic capacitances in oscillator test equipment, causing delays which are not accounted for in the oscillator circuit simulation model. In fact, the addition of a capacitor to the oscillator output was shown in a preliminary investigation to produce simulation results that accurately matched the measured ones.

Figure 7. Measured versus SPICE Level 3 and BSIM3v3.1 simulated gate propagation delay as a function of bias in a 101-stage ring oscillator.

5.0 CONCLUSIONS

The results of SPICE Level 3 and BSIM3v3.1 ac and dc model parameters extracted for the CMOS portion of monolithic integrated MEMS manufactured in a MEMS-first process have been presented. Transistor-level simulation of MOSFET current, capacitance, output resistance, and transconductance versus voltage using the extracted model parameters closely match the measured data. Moreover, in model validation efforts, circuit-level simulation values for the average gate propagation delay in a 101-stage ring oscillator are within 13-18% of the measured data. In general, the BSIM3v3.1 models provide improved accuracy over the SPICE Level 3 models. These results establish the following: (1) the MEMS-first approach produces functional CMOS devices integrated on a single chip with MEMS devices and (2) the devices manufactured in the approach have excellent transistor characteristics. Thus, the MEMS-first approach renders a solid technology foundation for customers designing in the technology.

6. ACKNOWLEDGMENTS

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