A Practical Implementation of BICS for Safety-Critical Applications

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Abstract

This paper presents the challenges and solutions of applying Built-In-Current Sensors (BICS) to a safety-critical IC design for the purpose of in-situ state-of-health monitoring. The developed Quiescent Current Monitor (QCM) system consists of multiple BICS and digital control logic. The QCM BICS can detect leakage current as low as 4 μ A, run at system speed, and has relatively low real estate overhead. The QCM digital logic incorporates extensive debug capability and Built-In-Self-Test (BIST). We performed analog and digital simulations of the integrated BICS, and performed layout and tape-out of the design. Silicon is now in fabrication. Results to date show that, for some systems, BICS can be a practical and relatively inexpensive method for providing state-of-health monitoring of safety-critical microelectronics.

I. Introduction

Measuring the quiescent power supply current of an IC is a well known and widely used technique for detecting defects such as bridging, open, and parasitic transistor defects [1-3]. Normal operation of an IC can degrade previously undetected faults and increase leakage current [4]. In addition, environmental stresses, such as temperature, voltage, radiation, or age can aggravate faults, or cause damage resulting in elevated I_{DDQ} [5-7]. Our Quiescent Current Monitor (QCM) system can detect elevated I_{DDQ} current real-time during system operation for state-of-health monitoring of an IC. The QCM performs leakage current measurements on every transition of the system clock to get maximum coverage of the IC in real-time. The quiescent current trip point can be set as low as 4 μ A. BICS are placed on the end of every standard cell row of the monitored system core logic. Each BICS monitors the quiescent current for its row and contributes to a single state-of-health output. The QCM includes extensive built-in debug capability via scan to allow complete controllability and observability for each

BICS.

In the tester environment, the QCM distributed BICS can detect and locate faults in an IC. This can significantly reduce fault diagnosis efforts [8]. Real-time I_{DDQ} testing can also reduce tester time when normal I_{DDQ} test methods are time-intensive.

In the system environment, the QCM can provide state-of-health monitoring for the core of the IC by detecting high current faults introduced by extreme environment, or aging. It can also detect speed degradation of the technology due to radiation, temperature, or other environmental conditions. Highly critical outputs can be safely shut down in real time when faults or speed degradation indicate questionable logic function.

We will first describe the analog BICS and simulations, then discuss the digital control logic of the QCM. Finally, we will highlight specific problems and their solutions during integration, simulation, and layout of the QCM with the target IC design.

II. Analog BICS

The target IC, or Device-Under-Test (DUT), is fabricated in a 0.6 μ m *n*-well technology using a standard cell digital library. The design consists of approximately 20,000 gates and has a system speed of 200 kHz. BICS must monitor leakage current after every transition of the system clock in order to be real-time. Desired BICS accuracy is less than 10 μ A. These system parameters set the speed, size, and resolution requirements for the BICS.

The speed requirement is the most critical and is achieved by using multiple BICS across the die. Each BICS only monitors a sub-circuit of the DUT, which we call its Circuit-Under-Test (CUT). Either the power or ground for the CUTs must be isolated from each other in order to do multiple and concurrent BICS monitoring. In the DUT library, cell power or ground rails are shorted directly to the bulk of the transistors. Since this is an *n*-

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well technology, all grounded n-transistor sources are shorted together by the silicon substrate and can not be isolated. The n -wells for the p-transistors provide V_{DD} power isolation for each standard cell row. Thus, the BICS can perform V_{DD} power rail monitoring individually and simultaneously if each CUT consists of one standard cell row. Similarly, p-wells can provide isolation for p-well technology, and V_{SS} monitoring is possible.

The BICS must consume minimal area, especially since each standard cell row contains a BICS. The method of measuring static current will determine both size and resolution of the BICS. Many fast and small BICS have been proposed [9-14]. Fig. 1 shows the BICS cell that we developed to best suite our application. Fig. 2 shows the common bias generator (only one per DUT) that supplies bias voltages V_{P0} , V_{P1} and V_{N0} for the BICSs.

Fig. 1. QCM Built-In Current Sensor (BICS)

Fig. 2. Common Bias Generator

V_{DDQ} is the local power for each CUT and includes the n -well (i.e. PMOS bulk connections) and power rail for that standard cell row. The digital input **TEST** turns on **MP3** to supply power to the CUT at V_{DDQ} from V_{DD} when monitoring is not being performed. **MP3** is scaled

very large so that switching transients for the CUT are not significantly affected during normal operation. The bulk for **MP3** connects to V_{DDQ} , forming a diode connection between V_{DD} and V_{DDQ} . This insures that there will never be more than a diode drop in voltage between V_{DD} and V_{DDQ} , even during monitoring.

Fig. 2 shows the common bias generator for the BICS cells. This circuit generates global bias voltages needed by the individual BICS cells. Distributing voltages instead of reference currents to the individual BICS cells means only one bias generator is needed on the die. The current reference supplied to the bias generator, I_{REF} , comes either from an internal reference circuit or externally through a direct input. In either case, the reference current passes through **MN2** to create the global bias voltage V_{N0} . Devices **MN3** and **MN4** mirror the current into scaled devices **MP4** and **MP5** to produce global bias voltages V_{P0} and V_{P1} , respectively. Tying the bias nodes to unused bond pads provides additional capacitance for noise filtering.

In the BICS (Fig. 1), after transient currents have settled, a high on **TEST** turns **MP3** off to force quiescent current of the CUT through **MP1** instead of **MP3**. Devices **MP1**, **MP2**, and **MN1** form a high gain cascode amplifier (operated open loop as a comparator). **MP1** and **MP2** are sized up by $\sim 2X$ from the bias generator transistors **MP4** and **MP5**, therefore they can source $\sim 2 * I_{REF}$. **MN1** is $1X$ the bias generator transistor **MN2**, therefore it can sink only I_{REF} , or only half that of **MP1** and **MP2**. Under normal conditions ($I_{DDQ} \sim 0$) **MN1** limits the current through the cascode amplifier to I_{REF} and saturates at a high voltage near V_{DD} . Buffer **B1** amplifies **MN1** drain voltage and provides a proper digital output level, resulting in a low state at **HIGHQC** (High Quiescent Current detected). When the CUT quiescent current increases to the trip value (ideally I_{REF}), current through **MP1** will reach $2 * I_{REF}$, which is its limit. If the CUT quiescent current is increased further, the net current sourced by **MP2** drops below I_{REF} . (The CUT is in essence robbing the nominal I_{REF} from **MP2** and **MN1**) As a result, **MN1** drain voltage will drop near the V_{SS} rail causing a high state on **HIGHQC** indicating a high quiescent current fault. The actual I_{DDQ} trip point varies from I_{REF} due to the non-linear relationship between MOS drain current and voltage. As I_{DDQ} increases the bias points of **MP1** and **MP2** of the BICS change causing the trip point to occur somewhat lower than I_{REF} . Furthermore, **MP5** of the Bias Generator is sized to keep **MP1** of the BICS in the linear region rather than full saturation. Doing so minimizes the drop in V_{DDQ} during the test phase when I_{DDQ} passes through **MP1** of the BICS. The resulting trip point sits closer to half of I_{REF} than I_{REF} . This simply represents a factor easily calibrated.

BICS and Bias Generator layouts conform to the DUT standard cell library so that automatic placement

and routing can be performed. Simulations across temperature, voltage, and process conditions insure proper function during testing and system operation. Fig. 3 shows simulation results of the BICS and Bias Generator under typical conditions. HIGHQC is the digital output of the BICS. As the I_{DDQ} leakage current increases, HIGHQC switches from logic 0 state (0 V) to a logic 1 state (5 V). Detectable leakage current is below 10 μ A, as required. The chosen resolution for testing is 4 μ A. The circuit simulations work well below 4 μ A, but operation is approaching the threshold region, so results may not be consistent from die to die under use conditions

Fig. 3. HIGHQC output vs. I_{DDQ}

Fig. 4. V_{DDQ} vs. I_{DDQ}

Fig. 4 shows the change in V_{DDQ} during I_{DDQ} monitoring. Note that the voltage does not drop below 4.2 V because of the diode connection of BICS transistor MP3 bulk to V_{DDQ} .

The speed of the BICS will depend on how quickly V_{DDQ} can be discharged so that the voltage differential can be detected. This depends on the capacitance of the power net. Measured n -well unit capacitance times the maximum n -well dimensions of a standard cell row results in an estimated capacitance per BICS. Simulation shows 560 ns latency for BICS monitoring of 4 μ A leakage current under typical conditions. This is more than adequate for a system speed of 200 kHz (2500 ns per half cycle). Table 1 gives the simulated HIGHQC latency for given I_{DDQ} leakage currents.

Table 1. BICS Latency

I_{DDQ} leakage current	TEST to HIGHQC latency
2 μ A	985 ns
4 μ A	560 ns
8 μ A	330 ns
16 μ A	215 ns

III. Digital Control

QCM Digital Control must support multiple BICS, use minimal real-estate, and have relatively little impact on system design phase, including design insertion, placement, and routing. In the tester environment, each BICS must be individually controlled and observed for fault analysis and debug. In the system environment, BICS monitoring must occur real-time, and BIST for the QCM must be included.

Fig. 5 shows the QCM floorplan and block diagram. There must be no switching during I_{DDQ} monitoring. Therefore, asynchronous portions of the core logic can not be monitored. For the target DUT, asynchronous logic consists only of input registers (primary inputs are asynchronous).

Fig. 5. QCM Floorplan Block Diagram

The QCM Control contains the bias generator, clock generator, BIST control, and scan control. The bias generator provides a current reference for the BICS. The current reference for the BIAS generator can be provided externally or selected internally from 1 to 15 preset values. User controlled scan allows controlling and observing of individual BICS for debug and failure analysis. It is possible to go into and out of scan during normal system operation so that an offending vector can be analyzed. If a vector is known to trip the QCM, system operation is halted at that vector and scan is used to determine which BICS detected high I_{DDQ} . By narrowing the DUT search area to a particular standard cell row, failure analysis efforts can be significantly reduced.

The clock generator provides timing signals for the BICS and delays the input clock, PRE_SYS_CLK, before applying it to the monitored and unmonitored core as SYS_CLK. Delaying the system core clock provides time to latch the previous clock transition BICS result and turn on the large p-transistor (MP3 of Fig. 1) before the CUTs draw any switching currents. The number of BICS used determines the loading, and thus the delay required for the system clock. There is provision to multiplex the clock from PRE_SYS_CLK to SYS_CLK when the QCM is disabled. Fig. 6 shows a timing diagram for the clocking scheme. Note that T_{TST} , the I_{DDQ} test time, is the last event before the next input clock transition. Therefore, T_{TST} time can be shortened to meet system speed requirements, trading off with I_{DDQ} trip resolution. (See Table 2 for simulation times of target DUT)

Fig. 6. Clock Timing Diagram

The QCM End Cell contains a scan register used for BIST and User Controlled Scan. For the BIST, a single digital input, RUN_BIST, forces a logic 1 to propagate through the scan chain and perform a calibration for each BICS. If any BICS fails, HQC_TRIPPED will be asserted. A failed BIST indicates that a BICS is not functioning properly, or that the power rails are insufficient to supply enough current for calibration (if this is the case, there will also not be enough current for normal switching of the CUT).

The QCM End Cells are placed at the end of each standard cell row of the monitored system core and contains the BICS and a scan register. A fixed bus width (independent of the number of BICS) interfaces the QCM End Cells to the QCM Control. This reduces routing resources and circuit complexity. A fixed bus width means that each BICS digital output, HIGHQC, must contribute to a single digital pass/fail for the DUT. Fig. 7 shows the circuit developed to accomplish this. It uses a wired-OR arrangement where any BICS that pulls down HQC_PULL_L will overdrive the control logic and cause the HQC_TRIPPED output to go high and remain high until reset. This indicates that a high I_{DDQ} fault has been detected, and that logic is no longer reliable.

Fig. 7. HIGHQC Transistor OR Circuit

IV. QCM and DUT Integration

Integration of the QCM and DUT involves schematics, simulation, and layout. The QCM is self-contained and almost completely non-intrusive to the design, so schematic integration is achieved simply by instantiating the QCM Control and an array of 50 QCM End Cells in the top sheet of the design. Other minor edits include adding QCM I/Os, adjusting power and grounds, and intercepting and delaying the system clock.

With system design complete, integrated QCM and DUT analog simulations can proceed. The analog simulation SPICE file contains one QCM Bias Generator, 50 QCM End Cells, pad capacitance, V_{DDQ} capacitance, and surrounding logic, such as buffers, drivers, and miscellaneous logic. SPICE simulations verify driver sizes in and out of analog cells, clock timing, and logic functionality. Table 2 gives the simulation results for the target DUT under typical conditions. (Refer to Fig. 6) Simulation speed results are well within the DUT system speed requirement of 200 kHz.

Table 2. Timing for target DUT

I_{DDQ} trip	T_{LCH}	T_{TRS}	T_{TST}	Frequency
2 μ A	22 ns	8 ns	985 ns	990 KHz
4 μ A	22 ns	8 ns	560 ns	1.7 MHz
8 μ A	22 ns	8 ns	330 ns	2.8 MHz
16 μ A	22 ns	8 ns	215 ns	4.0 MHz

Analog SPICE simulations verify analog cell timing characteristics, such as delay, rise and fall times. SPICE extractions of layout cells provide capacitance loading of analog inputs and outputs. Behavioral models of the QCM analog cells incorporating these characteristics enable complete IC level digital verification of both DUT and

QCM functionality and timing.

Layout integration utilizes the normal backend auto-place and route tools, with the exception of a script to seed the QCM End Cells at the end of the monitored core standard cell rows. The placement tool relies heavily on the hierarchy of the design. Simple front-end tool 'find' and 'group' commands adjust the hierarchy to place the QCM End Cells with the monitored core, and the QCM Control with the unmonitored input registers.

Fig. 8 shows the power/ground strapping floorplan. Power is routed on the left of the core logic and ground is routed on the right. This prevents shorting of the standard cell row V_{DDQ} nets between QCM end cells and the core logic, and is an option in the power strapping tool. The layout has an 'equate' command that resolves LVS errors caused by isolated standard cell row V_{DDQ} nets. The final layout passes all LVS and DRC rules.

Real estate is also an important issue. After layout, the addition of the QCM added approximately 20% core die area. This will be reduced with optimization after the QCM concept has been proven. The target DUT is I/O bound, even with the addition of the QCM. Therefore, there is no effective real estate impact.

Fig. 8. Power/Ground Strapping Floorplan

VI. Conclusion

I_{DDQ} testing is a commonly used method for identifying faults in ICs. Certain environmental conditions such as extreme temperature, radiation, and aging can also cause high I_{DDQ} . Therefore, BICS can provide state-of-health monitoring for safety-critical ICs if

the BICS can operate not only in (lab) testing but also real-time in-situ. BICS can also aid in the failure analysis process by locating which standard cell row is drawing high I_{DDQ} . We have integrated BICS into a safety-critical application with minimal cost and impact to the DUT. Complete analog and digital simulations verified timing and function. Addition of the QCM has little impact on the normal layout process of the DUT. Hardware is currently in fabrication and extensive test programs will evaluate the performance of the QCM and DUT.

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