1.0 INTRODUCTION

The next generation 30-100 Tflops supercomputers used in massive data processing of parallel lines (>1,000,000) will require >10 Tbit/s of aggregate data rate. It outpaces the capabilities of electronic technology. At the same time, rapid growth of fiber optics for tele and data communication applications have demonstrated that fiber optic transmission speed is moving to multigigabit data rate. This technology is expanding in a new generation computer interconnect, sensor networks, security networks, New Generation Internet (NGI) and new generation High Performance Parallel Computer Interconnect (HIPPI 64). This is primarily due to the many advantages of fiber optics and wavelength division multiplexing (WDM) over electrical conducting media, such as smaller size, lower weight, two orders of magnitude higher data rates, lower losses, lower signal dispersion, high immunity to electromagnetic interference, and lower cost of transmission medium.

Our goal in this program is to develop Fast Access Data Acquisition System (FADAS) by combining the flexibility of Multilink’s GaAs and InP electronics and electro-optics with an extremely high data rate for the efficient handling and transfer of collider experimental data. This novel solution is based on Multilink’s and Los Alamos National Laboratory’s (LANL) unique components and technologies for extremely fast data transfer, storage, and processing. The system is based on Multilink components and the technologies listed below:

- Analog and digital data transmission data links with data rates up to 10 Gb/s
- High speed radiation-hardened electrical, electro-optical, and opto-electrical components
- Multilink proprietary elastic memory based processor allowing synchronization and multiplexing of data with different data rates up to 5GB/s
- Highly parallel VCSEL optical interconnects with BER performance less than \(10^{-12}\)
- 12 Gb/s 30 mV of sensitivity Decision Circuitry with peak-to-peak jitter less than 6 ps
- All Optical Packet Switching Network Technology

Multilink's FADAS system dramatically reduces the latency (Synchronization time during packet switching) and increases the bandwidth of existing data acquisition systems, allowing for on-line triggering and classification of events, and identification of rare events. The major elements of the Multilink approach are:

1. The proprietary high speed (>5 Gb/s) FIFO elastic memory processor (EMP), allowing multiplexing and synchronization of channels with different data rates;
2. The mixed signal fiber optic data link recently developed by Multilink;
3. Extremely low crosstalk parallel (10 channels by 3 Gb/s) Vertical Cavity Surface Emitting Laser Diode (VCSEL) technology;
4. Fully monolithic > 2 Gb/s Opto-electronic Integrated Circuit (OEIC), based on GaAs (850 nm), and InP (1300-1600 nm) technologies.
DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.
DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.
All of these components have been presented by Multilink at the OFC exhibition in San Jose, California in February 1998.

Multilink’s FADAS has an extremely high aggregate bandwidth (> 1Tbit/s), while still preserving extremely low access (synchronization) time (< 200 nsec). The FADAS architecture is fully based on Multilink proprietary components and technologies as shown on Figure 1-1. The Multilink’s concept could be used for ISDN, National Information Infrastructure, SONET, SDH, fast ETHERNET (FIREWIRE), and other applications of super multicluster systems.

In order to realize the full potential of this technology, our effort also addressed the development of the major components and data link needs in both device and system aspects. The main purpose was to bring developed technologies to a commercial market with a short-term transaction from development to a commercial product. The following achievements were realized in this program.

1. An understanding of the data link requirements of the DOE and worldwide High Energy Laboratories. We received an invitation from Dr. Grzegorz Wrohna from CERN to attend an optical workshop in Geneva. He is interested in integrating Multilink’s developed components and systems at the CERN testbed. Dr. Nina Taranenko from LANL visited Multilink and did a preliminary test of the Rainbow-3 WDM network’s front end utilizing Multilink’s circuitry such as a monolithic and hybrid clock and data recovery and an optical front end circuitry.

2. Design, analysis, and fabrication of several GaAs ASICs and board level units. These developments have led to the next generation of the time division multiplexing technique, allowing error free multiplexing of several 2.488 Gb/s data signals coming from different terminals.

3. Development of up to 5 Gb/s transceivers. Specially designed opto-electronic transceivers are needed for the operation combining several data streams coming from different terminals. A number of opto-electronic transceiver prototypes have been fabricated for this program, and they have been incorporated in some of the demonstration hardware in this program.

4. Completion of demonstration hardware prototypes. To attract market attention and accelerate the commercialization opportunities, two demonstration hardware prototype systems have been designed and constructed, including all optical switching network. This incorporates Multilink’s proprietary SAW filter based clock recovery technique.

5. The commercialization emphasis of this SBIR DOE program was toward the development of basic components and systems for high-speed datacom and telecom networks, utilizing the unique properties of asynchronous time division multiplexing (TDM) technique. The resulted information has motivated us to focus on 10 GB/s market segments.
Figure 1-1. The Architecture of MTC's Proposed FADAS System
2.0 Phase I Results and Achievements

The following is a summary of the findings and achievements made during this Phase I program.

(a) Based on a study of HEP networks Multilink successfully developed, optimized, fabricated and preliminary tested of 2.5 Gb/s, 5 Gb/s and 10 Gb/s data and clock recovery full custom integrated circuits to be used at front end electronics of HEP experiments.

(b) The successful development and optimization of the twelve channel receiver/transmitter array operating at a data rate of 1.5 Gb/s with excellent power budget (better than -14dBm of optical sensitivity), using vertical cavity surface emitting Laser Diode (VCSEL) and integrated opto-electrical integrated circuit receiver.

(c) Experimental demonstration of 5 Gb/s receiver board with 1:2 de-multiplexer output with optical sensitivity greater/less than -20dBm, based only on Multilink technologies. This achievement demonstrates the feasibility of using Multilink's fiber optic/electronic interface design for multi-gigabit scenarios.

(d) Successful development, optimization, fabrication and demonstration of a preliminary prototype of innovative channel bundling technology using Multilink proprietary double loop asynchronous bit multiplexing technology what increase the efficiency of the neural network multiprocessor system. This achievement demonstrates the feasibility of using Multilink's FADAS for HEP experiments in order to reduce latency and increase the efficiency and robustness of HEP networks.

(e) Identification of major applications that require the new capabilities of the FADAS technologies, including CERN experiment, Rainbow network, Lawrence-Llvermore multi-gigabit networks and novel OC 192 networks based on optical crass correct topology. These findings confirmed that Multilink's FADAS architecture is unique, and that it provides strong advantages over state-of-the-art technologies.

(f) Development of components and improved FADAS design will be implemented in Phase II for FADAS prototype fabrication. This design provides a solid and realistic implementation plan for FADAS components and technology and commercial product development in Phase II.

(g) Demonstration of all-optical packet switching network based on LANL and Multilink's components and technologies.
In addition, the proposed FADAS was built on Multilink's latest advances in asynchronous TDM, parallel data transmission, variable frequency clock recovery, variable wavelength low cost laser diode technology (developed jointly with Amp), and cost effective 10 Gb/s external electro-optical modulation technique. Based on the advances Multilink demonstrated asynchronous multiplexing technique allowing the combination of data processing from a large number of sensors (>100,000,000), with extremely low synchronization time on MUX/DEMUX interconnect (less than 3 ns). This provides very fast decision-making, limited only by processor speed. Multilink's FADAS approach offers exceptionally high-power budget (combination of Multilink's modulator driver and external LiNiO₃ electro-optical modulator from Multilink's commercial partner Uniphase Inc.), and a highly distributed point to point distance (>160 km) transmitters over a single fiber.

Multilink's FADAS also provides high performance routing of data to the appropriate controller node, which can then combine and process two asynchronous 2.5 Gb/s streams and transmit and receive 5 Gb/s data through optical fiber. In addition Multilink's components have a high level of radiation hardening, which is very important to improve reliability of HEP DAQ. The radiation hardening is achieved by using TRW's space qualified HBT and HEMT GaAs process.

2.1 Phase I Hardware Demonstration

The Phase I key feasibility demonstrations consisted of five major parts. They were related to the final FADAS system model, its basic components (including various fiber link interfaces, WDM, demonstration and preliminary testing of ATDM), and appropriate DSP and software for data handling. Specifically these demonstrations included:

- Demonstration of 10 Gb/s extremely low jitter decision circuitry
- Demonstration of FADAS' electro-optical interface with data rate 5 Gb/s.
- Demonstration of 10 Gb/s electro-optical interface with Q factor greater than 25.
- Demonstration of 10 Gb/s receiver with clock and data recovery that had extremely low BER at –16 dBm of sensitivity.
- Demonstration of 10 Gb/s Eye Synchronizer, allowing us to estimate the performance of the 10 Gb/s fiber optic system without channel interruption.
- Demonstration of 5 Gb/s fiber optic receiver with a 1:2 demultiplexer output.
- Demonstration and testing of a preliminary prototype of 2:1 ATDM.
- Demonstration and laboratory testing (jointly with LANL) of all-optical packet switched networks.
2.2 Experimental 5-Gb/s Electro-Optical Converter

Multilink's key Phase I demonstration related to the performance of the FADAS models in handling high-speed data streams. In order to demonstrate the feasibility of the high-speed electro-optical interfaces, Multilink developed an electro-optical interface with a data rate of 5 Gb/s. In this experiment, we demonstrated two 5-Gb/s transmitters using a direct laser diode modulation (from Ortel) and an external electro-optical modulator (EOM). The uniqueness of this experiment lay in its use of the same driver to drive the laser diode and the EOM. The difference resided in the loading of the modulator driver and the pre-distortion of the modulation pulses in order to obtain a 50% duty cycle at the output of the opto-electrical converter.

A block diagram of the electro-optical converter (OEC) based on the laser diode driver is shown in Figure 2-1. Multilink's laser diode driver allows the driver to drive up to 100 mA of current. This modulator driver was also tested at Northern Telecom. It was found that the operation of the chip is in compliance with Multilink's preliminary specifications.

![Figure 2-1 Block Diagram of OEC Based on Laser Diode Driver](image)
The RF current is controlled by an AC knob, allowing the AC current to be changed from 10 to 100 mA. A DC knob allows the DC current offset to be changed from 5 to 40 mA in order to optimize the threshold level of the laser diode. R5 and R6 allow the current to be limited via the laser diode. Inductance L1 provides current source conditions. Potentiometer R2 allows the duty cycle of the output data to be changed in order to maintain a 50% duty cycle at the receiver output.

A block diagram of the OEC based on the external electro-optical modulator is shown in Figure 2-2. Multilink’s laser diode driver allows for the delivery of 5-V pulses at the single-ended 50-ohm load, making the implementation of this type of modulator driver much easier in comparison with the laser diode driver. Potentiometer R2 makes it possible to control a duty cycle distortion of the output optical data in order to maintain a 50% duty cycle at the output of the OEC. The AC knob allows the pulse amplitude to be changed from 200 mV up to 5 V. Multilink used an external modulator driver from Pirelli to demonstrate the performance of the electro-optical converter. The photograph of the laser diode driver ASIC is shown on Figure 2-3.

![Figure 2-2](image)

**Figure 2-2**
Block Diagram of OEC Based on External Electro-Optical Modulator
2.3 10 Gb/s Electro Optical Modulator

The second part of Multilink’s key Phase I demonstration related to the performance of the FADAS models in handling 10 Gb/s data. In order to demonstrate the feasibility of the high-speed electro-optical interfaces, Multilink developed an electro-optical interface with a data rate of 10 Gb/s. In this experiment, we demonstrated the 10 Gb/s transmitter using an external electro-optical modulator (EOM). The uniqueness of this experiment lay in its use of the Multilink developed Modulator Driver (MDR) to drive the EOM. Multilink built two EOM based on Uniphase and Sumitomo Cement Company EOMs. MDR allows us to obtain an excellent extinction ratio (greater than 14 dB), and a phenomenal Q factor (> 25).
the input via passive clock recovery circuitry. Clock recovery is a passband filter based...
The OEC converts a signal from an optical to an electrical domain. The signal from the OEC output in non return-to-zero (NRZ) format comes to the input of the Exclusive OR (EXOR) circuitry in order to generate the return-to-zero (RZ) signal. This signal comes to the input via passive clock recovery circuitry. Clock recovery is a passband filter based on digital readout (DRO). This filter has a Q factor >1600, which allows recovery, with jitter transfer function, exceeding Bellcore requirements. The sine wave output signal is amplified through the use of a proprietary Multilink 8-dB gain block that was designed by Multilink's microwave engineer, Andrew Bonthron. The sine wave signal at the output of the 8-dB gain blocks has an amplitude of >100 mV. The 10-GHz signal is divided by two using Multilink’s proprietary, extremely low noise divider, which has two complementary outputs generating a square wave at a frequency of 4.976 GHz.

This divider concept was developed by Multilink's President, Dr. Richard Nottenburg, also a Lucent pioneer. Multilink's unique divider has an extremely low internal jitter, which was proven at SPRINT's Advanced Technology Laboratory as part of a preliminary prototype test. The second output of a divider-by-two is connected to the input of a divider-by-eight in order to reduce the frequency up to 622 MHz. An additional DFF is used to reduce the signal jitter and to reduce the rise and fall time up to 27 ps. The DFF concept was developed by Dr. Richard Nottenburg, summarizing his 18 years of research on the nature of HBT GaAs transistors at AT&T, USC, and TRW. The output signal of the divider-by-eight will be re-timed and reshaped using Multilink's DFF (evaluation fixture shown in Figure 2-6). It should be noted that the peak-to-peak jitter is less than 5.8 ps, and the rms jitter is less than 900 fs. All of these preliminary results were derived from DFF testing conducted during Phase I.
2.2.2 5-Gb/s Receiver with DEMUX 1:2 Output

During Phase I, Multilink designed and fabricated the 5-Gb/s receiver board (shown in Figure 2-7). This board is fully based on Multilink's components with the exception of the opto-electrical module, for which Multilink used an OEC from Northern Telecom. The design of this board proves that a 5-Gb/s board can be built through the use of a conventional PCB manufacturing technique. The PCB is shown in Figure 2-8. This board was designed and simulated by two Multilink engineers, Mr. Andrew Bonthon and Mr. Sergey Zelensky. The board was built using Rogers's material, which allows for the use of a conventional PCB technique up to 10 Gb/s. The output signal of the OEC (SMA connector) will be delivered to the input (a 10-GHz MMCX surface mount connector from Rosenberger) of a variable-gain-limiting amplifier. Multilink is using a semi-rigid cable that will allow for an input return loss greater than -14 dB. The AC coupling is performed by using a multi-layer 15-nF high-speed capacitor (C 35) with resonant frequencies above 6 GHz.
The PCB uses thermal via in order to dissipate power from the ASICs. The first output of the VGA is connected to the CDR input. The second VGA output is connected to a 6-GHz MMCX connector from SUHNER. This connector is used to determine the performance of the VGA circuitry. Under normal operating conditions, this output will be terminated using a high-speed 50-ohm load. The VGA threshold is controlled by potentiometer R11. The CDR 5-Gb/s data output is AC connected to the DEMUX data input.

The second CDR data output (MMCX SUHNER) is a control output that is terminated with a 50-ohm termination under normal operating conditions. The CDR Evaluation Fixture is shown in Figure 2-9. The CDR clock output is AC connected to the DEMUX input via an adjustable coaxial cable. It allows for the maintenance of an optimal data-clock distribution at the DEMUX inputs. The DEMUX has three outputs connected through microstrip lines to the surface-mounted SMA Rosenberger connectors. As a result, there are two channels of 2.5-Gb/s data and one output of a 2.5-GHz clock.
2.2.3 Multilink 10-Gb/s Eye Synchronizer

During Phase I, Multilink designed, fabricated, and preliminarily tested a 10-Gb/s Eye Synchronizer, (ES) utilizing off-the-shelf and in-house 10-Gb/s technologies. A block diagram of the ES is shown in Figure 2-4, while that of the ES board is shown in Figure 2-5. In this design, Multilink used an OEC from Northern Telecom and a clock recovery module from Veritech, Plainfield, NJ. Multilink and CTI’s joint efforts in Phase II will be directed toward the design of the clock recovery module. This design is based on Multilink’s 8-dB gain blocks, which are based in turn on a HEMT GaAs process. Multilink’s first prototype of the 10-Gb/s OEC will be ready for testing at the end of the first quarter of 1998. Its design is based on Multilink’s proprietary HEMT GaAs transimpedance amplifier design.

2.2.4 Demonstration of Two-Channel ATDM

The development of the two-channel ATDM is a key issue for the future design of the FADAS networks; therefore, we will discuss each aspect of this development process separately and in detail.
2.2.4.1 Theory of Operation

The ATDM allows two data streams coming from different network nodes to be aligned with a relative phase shift of 10 bits. The principle of a phase shift compensation is based on a first-input/first-output (FIFO), one-bit, 24-bit depth memory architecture initially preset at a 12-bit delay difference between write and read pulses as shown in Figure 2-10. Consider the input data $S(t)$ as:

$$S(t) = \sum_{k=1}^{N} a_k \delta[t + \frac{k}{B} + \phi_k(t)]$$

(1)

where $B$ = data rate in bounds and

$\phi_k(t)$ = phase distribution of data A

![Figure 2-10 Illustration of Data Alignment](image_url)
The Write Clock Distributor (WCD) generates pulse sequence $U(t)$ to store data in 24 DFFs sequentially:

$$U(t) = \sum_{k=0}^{N} \delta(t + 24 \frac{(k+i)}{B} + \varphi_i(t))$$

where $i = 0,1,\ldots,23$.

As a result, we will have data at the outputs of DFFs $S_D(t)$:

$$S_D(t) = \sum_{k=1,i=0,1,\ldots}^{N} a_{(k+1)} \delta(t + 24 \frac{(k+i)}{B} + \varphi_i(t))$$

The Read Clock Distributor (RCD) generates pulse sequence $Q(t)$ to assemble data at the output of a 24 wired OR circuitry:

$$Q(t) = \sum_{k=1}^{N} \delta(t + 24 \frac{(k+i+1/2)}{B} + \psi_i(t))$$

where $\psi_i(t)$ is a phase clock distribution.

In accordance with our preliminary assumption, the phase difference (PD) between Clock 1 and Clock 2 is less than 10 periods.

$$PD < 10/B$$

Put another way,

$$10/B = \sqrt{[\psi_i(t)]^2 - [\varphi_i(t)]^2}$$

Because clock signals $Q(t)$ and $U(t)$ are initially preset in 12 bits of phase difference, we will automatically avoid a competition effect during the write and read cycle of the FIFO operations.

As a result of data conversion, we will have output data at the output at the wired OR $S_w(t)$:
\[ S_w(t) = \sum_{k=1}^{N} a_k \delta \left[ t + \frac{(k+12)}{B} + \psi_i(t) \right] \]  \hspace{1cm} (7)

Data \( S_w(t) \) will be aligned with Clock 2.

In order to improve power consumption and minimize the problem caused by big chip layout parasitics, Multilink applied a de-multiplexing technique, allowing the speed of data conversion to be halved.

At the first stage of data conversion in the Multilink system configuration, we perform bit de-multiplexing by factor 2. In this case, we consider the input data \( S(t) \) as

\[ S(t) = \sum_{k=2n}^{N} a_k \delta \left[ t + \frac{2k}{B} + \psi_i(t) \right] + \sum_{k=2n+1}^{N} a_k \delta \left[ t + \frac{2k}{B} + \psi_i(t) \right] \]  \hspace{1cm} (8)

or

\[ S(t) = S_1(t) + S_2(t) \]  \hspace{1cm} (9)

We will delay the half-period \((1/B)\) signal \( S_1(t) \) and will receive two data streams — \( S_1(t+1/B) \) and \( S_2(t) \) aligned in time, which yields the possibility of providing data conversion at a lower data rate, as illustrated in Figure 2-11. This operation is performed by a standard 1:2 DEMUX.

Because the operational speed is reduced twice, we can perform all operations at half the speed using two channels working at lower speed.

A block diagram of Multilink ATDM configuration is shown in Figure 2-12.
2.2.4.2 General Description

The ATDM is a high-speed, two-channel elastic buffer device that allows for the compensation of a phase shift between two data streams, such as DATA A and DATA B coming from different terminals. The ATDM performs digital signal conversion based on FIFO memory architecture with a depth of 24 bits. This allows one to write DATA B into the FIFO using the clock recovered from this data stream, as well as to read the stored data by using the clock signal recovered from the DATA A channel. The phase
The delay of the read and write signals can be preset to a phase difference of 12 bits, allowing for the alignment of two data streams with more than a 10-bit phase shift.

During normal operation, 2.488-Gb/s data is written into one of the 24 memory cells at a time. The memory cell is selected by using a block of a multiphase WCD, which is synchronized by Clock B. WCD operates at a frequency of 103.66 MHz. The 2.488-Gb/s data stored in the memory cells is read using the multiphase Read Clock Distributor (RCD), which is synchronized with the clock from Channel A. RCD architecture allows one to optimize the multiplexing of the 24-memory cell outputs.

An on-chip phase detector allows for the monitoring and control of the phase shift between the two channels. The internal PRBS generator provides a replacement for the data in either one of the channels (Channel A or Channel B) when data is lost. The RESET signal presets the WCD and the RCD blocks of the Elastic Memory (EL-MEM) and sets the initial 12-bit phase shift between the memory write and read pointers. De-multiplexing of the input data by a factor of two allows one to handle all FIFO operations at 1.244 Gb/s. RESET1 is used to initiate the PRBS generation when one of the signals is lost. Under normal operation, RESET1 disables the PRBS generator block.

The ATDM chip is designed to allow two aligned 2.488-Gb/s data streams to be synchronized to a common clock in order to multiplex the aligned data 2 to 1 using a convenient TDM technique, as shown in the system block diagram.

2.2.4.3 Functional Description

The ATDM is designed to align two synchronous data streams coming from different terminals. In order to reduce power consumption, the input data from the second channel is de-serialized into two data streams with a speed of 1.244 Gb/s. Thereafter, these data streams are fed into a 2 x 12-bit FIFO operating at a frequency of 1.244 GHz. This architecture allows one to reduce the speed of the WCD and RCD blocks. A block diagram of the ATDM is shown in Figure 2-13. In this diagram, the 2.488-GHz Clock A is coming to the input of the Clock A Distributor (CAD). CAD distributes Clock A pulses to supply the PRBS generator in the control block with a 1.244-GHz clock. It also connects a 2.488-GHz clock signal to the Channel A Network (CAN) block. CAD accepts 2.488-GHz Clock A pulses coming from an external clock and data recovery circuitry and the 2.488-GHz clock coming from the output of the Clock B Distributor (CBD).
CAN accepts 2.488-Gb/s DATA A, a 2.488-GHz clock from CAD, and a PRBS signal from the PRBS generator of the control block. CAN distributes 2.488-Gb/s DATA A and 2.488-GHz Clock A pulses to the output of PBS, 2.488-GHz clock pulses to trigger ODBB, and a 1.244-GHz clock synchronous to Clock A to drive the RCD block of EL-M. The signal LOS A reconfigures CAD and CAN when DATA A is lost. If LOS A is low, Clock B will replace Clock A at the outputs of CAD. The input DATA A at CAN will be replaced by PRBS synchronized by Clock B. In this case, 2.488 GHz Clock B will replace Clock A at PRBS output. CBD distributes 2.488-GHz Clock B pulses at the input of CAD and 1.244-GHz Clock B pulses to drive the WCD circuitry.

CBN accepts 2.488-Gb/s DATA B and 1.244-GHz Clock B and de-serializes DATA B in two channels, DATA B1 and DATA B2. This data is delivered to the two inputs of the 2x12 FIFO memory.
The control block accepts external control signals in TTL (ECL) levels and distributes preset signals to the WCD and RCD blocks, thus ensuring a >10-bit initial phase difference between write and read pulses. The control block generates an internal 1.244-Gb/s PRBS in order to replace data lost in Channel A or Channel B.

The EL-MEM accepts de-serialized DATA B1 and DATA B2 and stores this data bit by bit in the 2x12 FIFO memory using the multiphase WCD initially preset by the RESET signal. The stored data is multiplexed by two 12:1 (6:1, 2:1) multiplexers that are externally synchronized by the RCD. After multiplexing, we are obtaining bit-by-bit DATA B1 and DATA B2 synchronized with Clock A. The final multiplexing is performed by a 2:1 multiplexer stage. As a result, we receive the 2.488-Gb/s DATA B signal synchronized to Clock A pulses.

The phase shift between WCD and RCD signals is monitored by the phase detector in the control block. Signal PHASE indicates the phase difference between Channels A and B. This phase detector is based on an RS flip-flop that is set with the WS signal coming from WCD and reset with the RR signal coming from RCD.

The Output Data Buffer B (ODBB) accepts 2.488-Gb/s DATA B pulses, the 2.488-GHz clock from CAN output, the 1.244-Gb/s PRBS signal, and control signal LOS B. If LOS B is high, DATA B is switched through to the output of ODBB. If LOSB is low, PRBS synchronized by Clock A will be at the output of ODBB. The timing diagrams of ATDM are shown in Figure 2-14. (Note: the PRBS generator must be activated to ensure a valid replacement signal on a LOS condition. Pulling signal RESET1 low performs the activation.)
The CAD normalizes Clock A pulses and allows to replace Clock A when the signal in channel A is lost. Clock A comes into the input of the input clock buffer (ICB) as shown in Figure 2-15.
The ICB normalizes the amplitude of a clock signal and sends the signal to the first multiplexer (MUX) input. The second MUX input is connected to the Clock B output of CBD. If the control signal LOS A is high, Clock A will pass the MUX; if the LOS A signal is low, Clock B will pass the MUX. The output of the MUX is connected to the buffer input. The first buffer output is the CAD 2.488-GHz clock output; the second output is connected to the input of a divider-by-two (DIVBY2). The 1.244-GHz clock output of DIVBY2 is connected to the buffer input. Two buffer 1.244-GHz outputs are clock outputs of CAD. Assuming that LOSA is high, the Clock A signal will supply the clock input of DIVBY2. A timing diagram of the CAD is shown in Figure 2-16.

The CAN block (Figure 2-17) normalizes DATA A pulses and generates output 2.488-Gb/s DATA A, the main-output 2.488-GHz clock signal, and the 2.488-GHz clock signal, which is used to synchronize output data buffer B (ODBB).
When LOS A is high, Data A passes the MUX and comes into the D input of the DFF. When LOS A is low, the PRBS signal passes the MUX block and is fed into the D input of the DFF. The 2.488-GHz Clock signal passes a buffer, toggles DFFAN, and generates an output data stream. The output buffer ODB allows 8-V differential Peak-to-peak pulses to be obtained. The timing diagram of the CAN is shown in Figure 2-18.

2.2.4.6 Clock B Distributor

The CBD (Figure 2-19) normalizes the 2.488-GHz clock pulses and generates 1.244-GHz clock pulses for DATA B de-multiplexing in the CBN block and 2.488-GHz clock pulses to supply the CAD. The timing diagrams of clock signal conversions are shown in Figure 2-20.
2.2.4.7 Channel B Networks

The CBN block (Figure 2-21) normalizes DATA B pulses and de-serializes the data into two channels, Data B1 and Data B2, with data rate 1.244 Gb/s, aligned with output Clock B1. The CBN timing diagrams are shown in Figure 2-22.

2.2.4.8 Elastic Memory

EL-MEM has two modes of operation: the write mode and the read mode. Data B1 and Data B2 are aligned with Clock B1. Clock B1 drives the WCD circuitry in order to generate multiphase clock signals and record the data in the FIFO memory cells. A block diagram of the WCD networks is shown in Figure 2-23.

The RESET signal (pulse width > 10 ns) presets the WCD loop (Figure 2-24) at the beginning stage 100000000000. After the release of the RESET signal, the shift register works in a closed-loop operation, shifting the preset data bit by bit as shown in the timing diagram in Figure 2-22. After releasing the RESET pulse, the WCD generates 12 sample pulses with different phases at a frequency of 104 MHz. These are used to write data to
the memory cells. The WCD generates a multiphase signal that is used to store Data B1 and Data B2, as shown in the timing diagram in Figure 2-24.

![Block Diagram of WCD](image)

**Figure 2-23**
Block Diagram of WCD

![Timing Diagram of WCD](image)

**Figure 2-24**
Timing Diagram of WCD Networks
2.2.4.9 Multiplexer

The multiplexer uses 6:1 and 2:1 multiplexer functions to provide 24:1 multiplexing. The principle of the 24:1 multiplexer operation is illustrated in Figure 2-25. Data stored inside the 24 memory cells is multiplexed using the 6-input AND/OR gates (1-4) shown in Figure 2-23. Memory bits 2, 6, 10, 14, 18, and 22 are assembled by AND/OR gate 1, while memory bits 4, 8, 12, 16, 20, and 24 are assembled by AND/OR gate 2. The odd bits 1, 5, 9, 13, 17, and 21 are assembled by AND/OR gate 3, and the odd bits 3, 7, 11, 15, 19, and 23 are assembled by AND/OR gate 4.

Figure 2-25
Block Diagram of Multiplexer Network
The timing diagram of RCD outputs is shown in Figure 2-24. In order to avoid glitches, the first MUX stage combines data from memory cells 2, 6, 10, ..., 4, 8, 12, ..., 1, 5, 9, ..., and 3, 7, 11, .... This data is then sampled by short pulses from RCD outputs, as shown in the timing diagrams in Figure 2-26. The second stage of multiplexing is performed by two OR gates (5, 6). The third level of multiplexing is done through use of a standard 2:1 multiplexing technique with re-timing flip-flops to avoid glitches.

2.2.4.10 Output Data Buffer B

The ODBB (shown in Figure 2-27) allows lost Data B to be replaced with the PRBS signal from the Control block. When signal LOS B is high, Data B passes through the multiplexer and comes to the D input of the DFF. The clock input of the DFF is connected to the clock buffer output, which delivers the 2.488-GHz Clock pulses. The ODBB timing diagram is shown in Figure 2-28.
2.2.5 IC Design

2.2.5.1 Design Strategy

The design strategy for the ATDM IC was to keep the whole design in the digital domain, thereby mitigating the risk common to mixed analog-digital designs. Almost all blocks used in the ATDM design are standard blocks with proven operating characteristics that were previously used in the target process. The design uses current switch logic that is limited exclusively to two levels. This leads to large power savings owing to the reduced supply voltage of -3.3 V.

The complexity of the IC is cut in half by building only one channel with variable delay. It greatly increases manufacturing and yield. Only one big FIFO memory is required. The other channel is only re-timed by a single flip-flop.
Another concept used in this design lies in the reduction of processing speed in the FIFO from 2.5Gb/s to a very conservative 1.25Gb/s through splitting of the incoming 2.5Gb/s signal into two 1.25-Gb/s separately stored data streams. This allows for the mitigation of design risks such as those associated with transmission line effects, distributed loads at high speed, and other problem areas.

Since it has been our experience that transmission line and coupling effects play a major role in GaAs HBT circuits on semi-insulating substrate, we selected a signal distribution scheme that is particularly favorable for high-speed applications in this technology. In this scheme, all data signal lines that require high-bandwidth operation are driven from the collector node of a current switch. The transmission line, which connects the driver and the load, is resistor terminated at both the source and the sink. Since the characteristic impedance varies depending on the propagation mode, especially for coupled lines, a compromise was chosen with a lower-impedance termination at the load and a slightly higher termination at the driver. This scheme conserves power but results in solid suppression of even-mode and odd-mode reflections.

All signals are distributed using differential transmission lines. This increases the noise margin, since coupling and noise on the power supply rails do not affect the odd-mode signal. In GaAs HBT technology, however, it is important to observe even-mode effects so as to eliminate unwanted effects that might reduce performance. The TTL inputs for the off-chip control signals, which are single-ended in nature, are converted immediately using single-ended to differential input buffers. This exploits the additional robustness of the differential signal distribution scheme for the on-chip control signals in a similar way. The other major advantage of differential signal distribution lies in the potential for power savings through reduced signal swing and eliminated reference-voltage generation circuitry compared to single-ended logic.

### 2.2.5.2 Design Implementation

The design implementation is based on a top-down design strategy so as to draw as many advantages as possible from a prudent system design. The main chip functionality was partitioned into five main functional units:

- Clock selection logic
- FIFO for Channel B
- Re-timing circuitry for Channel A
- PRBS generator block
- Glue logic for the data path of Channels A and B

The largest-complexity block, the FIFO for Channel B, was considered the most critical one. Before starting with the cell design for this block, an extensive simulation feasibility study was performed to predict any design problems that could potentially arise when putting together a big circuit block.

The issues considered most critical at this point were the MUX 6 to 1, which is a complex gate that performs the logic function of six 2-input AND gates and a 6-input OR gate. The loading of the collector node was considered an especially key parameter with respect to the success of this particular design implementation. Simulation revealed that
with application of air-bridged transmission lines, this block could operate beyond 2.5 Gb/s, which is twice the speed required for this block.

Another major gating factor pertaining to the feasibility of the design on the system level was the drive capability signal in the RCD and WCD blocks. As a pre-cell design test, a similar block was assembled with similar loading characteristics and simulated with estimated transmission-line models. The driver circuitry was explored with regard to its ruggedness and stability margins in the target configuration. The margin for the operating speed was estimated at 3X. The decision to limit the maximum number of loads to seven for this type of driver situation gave some additional margin under the anticipated layout constraints.

Changing the output duty cycle of the WCD timing loop could optimize the data driver circuitry for the memory cells. Of six memory cells that load a data line, only one can be active at any point in time. This greatly reduces loading for the data driver circuitry, since the input capacitance of the storage cells with low clock signal is much lower. It also reduces the feed through of the timing signals back into the data line. On the overall, this system concept increases the noise margin of the data lines to the memory cells.

2.2.5.3 Design and Simulation of Circuit Blocks

All cells are simulated to have a 2X margin compared to the actual circuit speed in the bit synchronizer chip. All cells are also required to work over a 0-125°C temperature range and a 3.3-V ± 10% voltage range. The transistors were chosen to operate well below the current limit, which sets the upper limit of the collector current for transistors in this technology. The expected temperature rise of the junction temperature compared to the temperature of the backside of the chip is below 10°C, which will give ample margin for the specified 0-75°C operating temperature range.

The current for the various cells on the chip was set using a simple current mirror approach. It allows the implementation of local current reference circuitry for each and every cell on the chip without the need to distribute reference voltages across the chip to bias multiple cells. This was seen to hold a significant advantage for the management of global wiring resources in view of the two-level gold liftoff process used. This strategy also eliminates potential crosstalk through reference lines along with any risk of current reference oscillations. The alternative approach that uses a band-gap reference circuit with a large number of powered cells was also avoided, since a characterized test chip for the band-gap reference circuit was not available at the time. Also the temperature characteristics of GaAs HBT devices differ significantly from those of silicon, where proven band-gap reference circuits have been implemented. The drawback of this design style is that output voltage levels vary slightly over the supply voltage range. It was shown, however, that the output voltage levels stay within about ±10% of the specified nominal value for the specified temperature and supply voltage range.

Differential current switch logic is used throughout the design. The differential voltage swing is 500 mV nominally. In the case of a two-level current switch gate, emitter-follower level shifts are used only to drive the lower-level current switches. The upper-level current switches are driven directly from the collector node of the preceding current switch gate. This allows the use of the reduced supply voltage of 3.3 V to conserve power.
while also mitigating the risk of emitter-follower oscillations, that can pose major problems—especially when the driver is connected to the load via a long on-chip transmission line.

The flip-flop cells were generally buffered with a simple current switch output buffer. This reduces the clock crosstalk to the output, cleans up the output signal, and improves noise margin. For the memory cells, an increased differential voltage swing of 1 V was chosen, providing an additional safety margin for bit error rate (BER) performance.

One of the problem areas identified in earlier designs lay in the on-chip dividers. The issue here is that if the noise margin is degraded by poor external conditions (e.g., poor bypass on the supplies, large supply variations, and temperature stress), the divider has an increased probability of phase flipping. The reason for this effect was identified to be significant clock crosstalk to the divider output due to low transistor reverse isolation of the GaAs HBT transistors in the standard divider design. A new approach was thus chosen which improves the divider noise margin by about 400%. This approach improves the reverse isolation in the divider loop by individually buffering the master and the slave output connections with one emitter-follower for each load rather than driving several loads with only one emitter-follower.

All high-speed input buffers have an on-chip 50-ohm termination, which was proven to be the right method in previous designs. The TTL inputs are equipped with special large-area ESD protection devices connected to ground, which are expected to significantly reduce the ESD sensitivity of the TTL inputs.

The output buffers were optimized for power consumption. Since the multiplexer chip will be located on the same board as the ATDM chip, the output matching resistor were chosen to be 200 ohms, which represents a good compromise between power savings and output match for outputs that are not driving long cables and can be connected differentially.

### 2.2.5.4 Floor Planning

The strategy for assembling the various blocks of the design was to keep the length of the high-speed signal path limited and to arrange the high-speed signal blocks as close to the I/Os as possible. This strategy partitions the design into two major circuit clusters. The first circuit cluster consists of WCD, the memory cells, and the CBN. It represents the full de-multiplex function with clock distribution and storage in the FIFO path. The second circuit cluster includes the RCD loop and the complete multiplexer circuitry. The timing and signal distribution between those two blocks is running at a speed of 100 Mb/s, thereby allowing for a very conservative busing scheme in the middle of the chip. To ensure adequate noise margin for the stored information in the memory cells, bus shielding was considered to be necessary. This increases the chip area but eliminates coupling effects, which would otherwise represent a serious problem in terms of interconnect modeling and full-speed functional verification at the simulation level.

All the other functional units of the ATDM chip were arranged around the de-multiplexer and multiplexer blocks. The main issue here was to streamline the on-chip signal flow to keep the high-speed signal lines short and the wiring congestion low. In addition, it is important to satisfy the requirements imposed by the pin-out of the CDR and the MUX
circuitry. The high-speed input and output signal pads were oriented to allow direct
differential connection to the CDR and MUX chips without crossovers. The TTL input
pins, however, were arranged more freely, since it is not necessary to impedance-match
the board traces for those control signals.

The VEE power buses were dimensioned to provide enough current-carrying capability
for cases in which all four corners of the chip are connected to the power supply.
Therefore, it is necessary to connect all available VEE package pins to the board power
plane. In-package bypassing with 82-pF and 1-nF, chip capacitors are recommended for
assembly.

2.2.5.5 Modeling and Simulating Main Functional Units

Initially, the main functional blocks were simulated using estimated transmission line
length. The transmission line length was derived from an initial chip floor plan along
with cell size information on similar cells implemented in previous designs. The blocks
that turned out to be the most critical in the design were the WCD and the RCD loops.
These two blocks operate at a relatively high speed (1.25 Gb/s) and have two clock lines
each that must drive six and seven cells, respectively. The focus of the simulation was to
optimize the driver circuitry and the transmission line type under the given layout size
constraints. It turned out that a simple emitter-follower driver with a shielded,
differentially coupled coplanar transmission line was more than adequate to fulfill the
requirements for clock distribution in those two blocks.

The next step in the simulation process was to assemble the complete de-multiplexer
section to optimize clock and data signal distribution and to verify timing feasibility
under the existing floor-planning constraints. The floor planning of this entire block,
which consists of the WCD, the memory cells, and the CBN, concentrated on minimizing
the signal skew in the parallel signal path. A one- to two-driver approach was chosen that
keeps the distances and the loads approximately the same for all branches of a high fan-
out driver system. Especially for the clock and data signal distribution, this strategy
turned out to meet the timing requirement with a solid margin and to give enough
flexibility to implement the collector node double-terminated driving scheme for those
timing- and bandwidth-sensitive nets. The timing of the WCD loop was adjusted such
that the memory cells sample the data signal lines in the middle of the eye.

The critical aspect of the multiplexer simulation lies in the verification of the timing
between the RCD loop and the re-timing circuitry in front of the final 2:1 multiplexer
stage. It was necessary to insert a delay buffer stage in the clock path driving the 2:1
multiplexer to optimize the timing in this block. The glitches which were expected at the
output of the 12:1 multiplexer units turned out to be far smaller than anticipated due to
careful timing optimization on the system level. These glitches do not represent a
problem, since all data signals are re-timed and aligned in front of the core 2:1
multiplexer circuit.

The PRBS generator block was treated separately. An estimated transmission line model
was used to predict the performance. The critical issue in this block was whether the
timing constraints could be met with the EXOR gate delay and loading due to the
transmission line in the feedback path. The cells were therefore arranged in a ring
topology that minimizes the impact of transmission line loading of the cell outputs. The clock distribution buffer and clock distribution lines were also carefully optimized.

2.2.5.6 Chip Layout

For the layout of the ATDM chip, a very conservative metal design rule set was chosen to significantly enhance the functional yield of the devices beyond the percentage values guaranteed for comparable designs that use minimum design rules. In addition, on-chip capacitors were avoided, and a very conservative cell placement strategy was chosen. The use of an air bridge was limited to a total of 24 sites on the chip, which represents no yield factor.

Coupling between signal lines and reduction of capacitance for the high-speed transmission lines was the main goal for interconnect routing. All differential signal traces are routed in close proximity. In places where several differential signals are running in parallel, cross-coupling was reduced by choosing a microstrip-type transmission line or by using a ground-shield wire to separate the different differential pairs. This layout style is also required to reduce the amount of simulation modeling for transmission line coupling in a big circuit. Low-speed lines were mostly routed as microstrip-type transmission lines to improve the signal integrity by effectively bypassing the signal traces with the largest possible distributed capacitance. Microstrip also provides the lowest possible coupling.

Despite the very loose layout style, a very compact and streamlined layout was achieved. A total of 1939 GaAs HBT transistors, 1652 thin-film resistors, 3 Schottky diodes, and 3 protection diodes were used. As a backup, the chip also contains 320 transistors that are not connected to allow for fast prototype adjustments where only the metal and resistors are changed. The chip area is 2750 x 3800 µm².

2.2.5.7 Full Chip Simulation

The full chip simulation was performed to prove the full functionality of the chip as well as to provide complete modeling of parasitic effects. In this process, it was necessary to convert the system-level schematic into a layout-oriented schematic that would allow for the insertion of the extracted layout parasitics. Currently, no commercial computer program is available to extract RLC transmission line parasitics and power supply inductances automatically. Therefore, careful manual extraction of all global wiring parasitics and power supply inductances were performed.

A full-scale simulation model of the IC with RLC transmission lines, power bus inductances, bond wires, and packaging models were used for verifying on-chip timing constraints and drive strength. This seemed to be necessary to catch potential oscillation problems in connection with the emitter-followers used for driving clock lines in the FIFO address generation units WCD and RCD. Wherever possible, simulations needed to verify the timing were performed on partitions of the chip to limit circuit complexity.

Major problems were encountered with simulation speed and the convergence of the complete chip simulation with full parasitics. This model was therefore used mainly to double-check the performance results from simulations without parasitics as well as to
verify the timing in the various blocks. Because it is important to reference to a single source of schematics in the design process, the schematics with parasitics were prepared in such a way that all the parasitics can be removed easily from the generated simulation netlist with a proprietary computer program for simulation and layout checking.

This simulation strategy allows selective parasitic modeling for the various blocks. It is therefore possible to achieve very accurate results for certain functional blocks without wasting too much simulation resources for blocks that are not important for the specific verification problem.

2.2.5.8 ATDM Test Plan

The ATDM test is performed in accordance with the testbed shown in Figure 2-27. The PRBS generator generates PRBS at a data rate of 2.488 Gb/s. Data 1 arrives at the data input of the clock recovery circuitry. The clock recovery circuit regenerates Data A and Clock A to supply Data A and Clock A of the BS input. The second output of the PRBS generator is connected to the input of the 5-GHz, 5-ns variable delay line with 5-ps increments available from Giga Baudics, which allows data shifts of > 10 bits.
Data B from the output of the variable delay line arrives at the input of the second CDR. The second CDR recovers Clock B and Data B. Those signals go to Data B and Clock B of BS.

Under normal conditions, LOS A and LOS B are high. In this case, after release of the Reset (R), we will obtain on the oscilloscope identical eye diagrams in both channels that are aligned in time, as shown in Figure 2-30.
When we change the delay in Data 2 path by changing the control voltage, the eye diagram must remain the same. In order to test BS when Channel A is lost, we will disconnect the inputs of Data A and Clock A. The LOSA must be set at a low level. After releasing R, we need to release R1. In this case we will obtain the eye diagram shown in Figure 2-31.

To test BS when Channel B is lost, we will disconnect the inputs of Channel B data and the Channel B clock. LOSB must be set low. In this case, after releasing R we need to release R1. As a result, we will obtain the eye diagram shown in Figure 2-32.
Multilink / LANL Test Bench

During Phase I Multilink did a preliminary test of all optical packet switching networks based on components developed during Phase I. The block diagram of the high speed optical packet switching test bed is shown on Figure 1.

Multilink applied a passive clock recovery technique that has several very important advantages over active pulse frequency detector based clock recovery.

The optical signal is converted from optical to electrical domain by using OEC. As a result at the OEC output we will have non-return to zero (NRZ) data. The NRD data does not have first tone in its spectrum. In order to enrich the spectrum of NRZ data with first tone we differentiate data, performing an exclusive OR logic. Assuming NRZ signal $S(t)$ we will obtain $S_d(t)$ at the exclusive OR output.

$$S_d(t) = S(t) + S(t+\tau),$$

where: $+$ is an exclusive OR operation,

- is $1/2B$

where: $B$ - is data rate in bonds.

This signal will have the first harmonic in its spectrum. Since the probability of positive and negative transition, is 0.5

$$V = A/(2\pi) * \sin (\pi t/T),$$

where: $A$ - amplitude of a digital signal at EXOR output,
ti - is pulse duration.

Because of the high selectivity of the narrow band filter clock, it can be recovered below sensitivity of optical receiver.
For example, if optical sensitivity is -16 dBm clock can be recovered at -26 dBm of input optical power, what is a big advantage over PFD clock recovery, which is able to recovery clock when the probability of error at the receiver output is 10.

The Laser Drivers generate optical signals with different wavelengths (1515, 1551 nm) modulated by PRBS. Those signals are combined by using a wave division multiplexer.
In order to demonstrate an optical packet switching we apply tunable optical filter (TOF) technology, driven by Driver, developed by LANL. The output of the TOF is split into two channels such as Low Frequency Receiver (LFR) and High Frequency Receiver (HFR).

The LFR is used to detect the average level of optical power at the TOF output. It allows us to scan optical channels and determine the number of optical channels, by counting the number of picks during wavelength scan. LANL driver allows us to hop to the selected wavelength and to provide optical packet switching. HFR generates high-speed data (1,25 Gb/s) in analog mode. A variable gain amplifier is used to regenerate data in a soft limiting mode (shown on Figure 2-34) in order to minimize the time jitter. The frequency doubler is used to enrich the NRZ data with first harmonic. The output signal waveform at frequency doubler output is shown on Figure 2-34.

Those signals excite low quality (less than 150) narrow band filter, which has an output reaction, as shown on Figure 4. This signal will be amplified by a second stage of limiting amplifier. The output signal waveform is shown on Figure This signal will have a timing jitter caused by an amplitude variation (>20 dB) at the filter output.

This signal will path a high quality (Q>600) SAW filter with internal attenuation 16 dB. As a result of filtering we will have a sine wave (shown on Figure 2-34) with amplitude 60 mV.

This signal will be amplified by the limiting amplifier. As a result, we will regenerate a square wave with an extremely low jitter (820 fs rms). This is much less compared to ITO/SONET specification (4 nc). The clock signal will trigger on output D flip-flop. The SAW filter has a temperature variation (±18°); therefore data must be adjusted in time domain in order to avoid an output D flip-flop failure.

Piezoelectric Fiber Fabry-Perot Tunable filter

Fast wavelength tuning is performed by using a high-speed piezoelectrically driven Fiber Fabry-Perot tunable filters (FFP-TFs). Microsecond tuning raises a whole new set of challenges, such as ringing, thermostability and mechanical inertia control. One approach to achieve fast wavelength tuning as well as polarization insensitivity and low loss that
are necessary to perform high-speed optical packet switching is to use **high-speed piezoelectrically-driven Fiber Fabry-Perot tunable filters (FFP-TFs)**.

Piezoelectric Fabry-Perot filters are typically reported to have millisecond tuning speeds. At our set up we used an FFP-TFs from Micron Optics Inc. (MOI) approaching one free spectral range (FSR) per several microseconds. To achieve those results we used in Multilink/LANL test bench special high-speed MOI's FFP-TFs and a novel LANL's stabilizing driver.

**Structure of FFP-TF**

The FSR of an ideal FFP-TF is related to cavity length (or distance between mirrors), $l_C$, by

$$\text{FSR} = \frac{c}{2nl_C},$$

where $c$ is the speed of the light in vacuum, and $n$ is the index of refraction of the cavity material.

The finesse, $F$, of an ideal, lossless FFP-TF is related to mirror reflectivity, $R$, by:

$$F = \frac{R^{1/2}}{(1-R)}.$$
Figure 2-33
The Timing Diagram of the Clock and Data Recovery-based SAW Filter
The bandwidth, NW, or wavelength resolution of the FFP-TF is simply

\[ BW = \text{FSR/F}. \]

A sketch of the inner optical configuration of FFP piezo-tunable filter is shown in Figure 2-34. Low voltage piezoelectric (PZT) actuators are used to position two highly reflective mirrors. The air gap between the mirrors is only about 1-3 micrometers. The cavity is aligned in the piezoelectric fixture, and tuning is achieved with PZT actuators that are capable of positioning accuracy of atomic dimensions. The construction of the FFP tunable filter with the single-mode optical fibers inside the cavity allows it to avoid the need for lenses, collimated beams, eliminates the "walk-off" tendency, and provides single-mode guidance and low-loss coupling.

Figure 2-34 also shows a sketch of overall FFP-TF structure consisting of PZT, mounting hardware, and optical-fiber components. Such a structure is inherently small and low mass, thus lending itself to the possibility of high-speed tuning. The steps taken to obtain high-speed performance specifically focused on reducing the mass of the PZT and its load that consists of the alignment hardware and optics. Initially, the alignment technology was designed into the mounting hardware much like the standard FFP fixture, except the length and the outer diameter were reduced in order to reduce the mass. Later in an alternative approach, the cavity alignment was carried out using external transition stages. This, in turn, allowed significant reduction in hardware mass. The mass of the optical components was also reduced by reducing their physical size.
Figure 2-34
Fiber Fabry-Perot Tunable Filter
Experiments with new high-speed FFP-TF.

As shown in Figure 2-35, in earlier experiments, the fastest tuning speed for the new small FFPs without optical was 50 μs. A 50 MHz pulse generator (HP 8112A) was used to drive the filter with a 1 V swing from approximately 1.8 V to 2.8 V. A single laser source with wavelength corresponding approximately 2.8 V is used to monitor the optical throughput of the filter. The rise and fall times of the drive voltage are controllable. Figure 2-35(a, b, c) shows the drive voltage overlaid on the optical power transmitted for 50, 10 and 5 μs rise and fall times, respectively. In Figure 2-35b, the rise time applied starts oscillations in both the driving voltage across the piezo and the optical throughput. In Figure 2-35c, the ringing becomes very strong. This may be due to exciting a PZT resonance.

The square-wave scan and the optical response of the filter are shown for single laser source: a) 50 μs, b) 10 μs, c) 5 μs rise and fall times, respectively.

As one can see, the switching speed of the new filter used in the fast mode is limited by acceleration of the mechanical motion and electrical loading of the drive voltage. A further increase in the driving slew rate induced extensive optical ringing. There are also oscillations on the top of the square waveform that increases with the driving slew rate. The optical ringing is a combination of the driving waveform ringing and internal effects. It was suggested that it may be possible to improve the shape of a driving pulse and the response of the filter by proper design of the stabilizing electrical driver, but the resonance of the piezo element must be taken into account.
Characterization of high-speed FFP-TF

The five critical performance parameters of high-speed FFP-TF include tuning time per FSR, mechanical resonance, response linearity, and overall switching and settling time. Correlation between the mechanical resonance and optical response of the filter is important for the optimal high-speed tuning designs and for mounting hardware and control circuitry optimization. That is why one of our major efforts was focused on raising the mechanical resonance to beyond 100 kHz. FFP-TF mechanical fixtures were characterized, differing in PZT, mounting-hardware, optics, load mass, and PZT length, as listed in Table 1.

<table>
<thead>
<tr>
<th>PZT length (mm)</th>
<th>PZT type (V/m)</th>
<th>PZT Mass (g)</th>
<th>Hardware Mass (g)</th>
<th>Optics Mass (g)</th>
<th>Load Mass (g)</th>
<th>First Res. (kHz)</th>
<th>TF0 (μsec)</th>
<th>TF (μsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TF1</td>
<td>16</td>
<td>12</td>
<td>4.4</td>
<td>5.2</td>
<td>0.5</td>
<td>5.7</td>
<td>40</td>
<td>7.00</td>
</tr>
<tr>
<td>TF2</td>
<td>10</td>
<td>18</td>
<td>3.0</td>
<td>5.2</td>
<td>0.5</td>
<td>5.7</td>
<td>52</td>
<td>9.40</td>
</tr>
<tr>
<td>TF3</td>
<td>10</td>
<td>18</td>
<td>3.0</td>
<td>3.0</td>
<td>0.5</td>
<td>3.5</td>
<td>59</td>
<td>5.90</td>
</tr>
<tr>
<td>TF4</td>
<td>16</td>
<td>12</td>
<td>4.4</td>
<td>3.0</td>
<td>0.5</td>
<td>3.5</td>
<td>34</td>
<td>7.00</td>
</tr>
<tr>
<td>TF5</td>
<td>10</td>
<td>18</td>
<td>3.0</td>
<td>1.2</td>
<td>0.5</td>
<td>1.7</td>
<td>68</td>
<td>3.90</td>
</tr>
<tr>
<td>TF6</td>
<td>10</td>
<td>18</td>
<td>3.0</td>
<td>0.1</td>
<td>0.3</td>
<td>0.4</td>
<td>75</td>
<td>2.68</td>
</tr>
<tr>
<td>TF7</td>
<td>10</td>
<td>18</td>
<td>1.8</td>
<td>0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>113</td>
<td>2.44</td>
</tr>
</tbody>
</table>

Table 1
High-speed FFP-TF test result

A network analyzer revealed a series of resonant frequencies in the fixtures’ impedance transfer functions (Figure 6-7). The table shows the improvement gained by reducing of FFP-TF's structural mass. For example, TF3 exhibits resonances at 59, 123, 172, 400, and 980 kHz, though the last two resonances are very weak (Figure 2-36b). By reducing the load mass from 3.5 g in TF3 to 0.4 g in TF6, this set of resonances moved out to 75 and 152 kHz, respectively (see Figure 2-37b). Furthermore, the magnitude of the first resonance decreased significantly. PZTs in TF1-TF6 have intrinsic resonances above 100 kHz; however, mechanical loading produces a first resonance below 100 kHz as shown in Table 1.
Next by reducing the load mass to 0.2 g in TF7, a dramatic improvement is obtained where the first resonance moved beyond 100 kHz, reaching 113 kHz (see Figure 2-37c). With regard to the PZTs, a smaller size PZT was specially fabricated for TF7. This small PZT has a mass of 1.8 g and a capacitance of 0.25 μF. The previous standard PZT has a mass of 3.0 g, and a capacitance of 0.5 μF. The PZT length dictates its intrinsic resonance, while the overall size and mass dictate its capacitance. The 10 mm PZT length has the first intrinsic resonance at ~150 kHz, and a comparison among TF2, TF3, TF5, TF6, and TF7 demonstrated that the lower load mass indeed contributed significantly to the increase in the mechanical resonance frequency and reduction in magnitude. On the other hand, the lower capacitance is very desirable for easing driving and control requirements.
Figure 2-37
Impedance transfer characteristics for a) TF5, b) TF6, and c) TF7
Next by reducing the load mass to 0.2 g in TF7, a dramatic improvement is obtained where the first resonance moved beyond 100 kHz, reaching 113 kHz (see Figure 2-37c). With regard to the PZTs, a smaller size PZT was specially fabricated for TF7. This small PZT has a mass of 1.8 g and a capacitance of 0.25 μF. The previous standard PZT has a mass of 3.0 g, and a capacitance of 0.5 μF. The PZT length dictates its intrinsic resonance, while the overall size and mass dictate its capacitance. The 10 mm PZT length has the first intrinsic resonance at ~150 kHz, and a comparison among TF2, TF3, TF5, TF6, and TF7 demonstrated that the lower load mass indeed contributed significantly to the increase in the mechanical resonance frequency and reduction in magnitude. On the other hand, the lower capacitance is very desirable for easing driving and control requirements.

Driver for High-Speed FFP-TF

The switching speed of the FFP-TFs used in the fast mode is limited by acceleration of the mechanical motion and electrical loading of the drive voltage. An increase in the driving slew rates induces extensive optical ringing. There are also oscillations on the top of the square waveform that increases with the driving slew rate. The optical ringing is a combination of the driving waveform ringing and internal effects. It was suggested that it may be possible to improve the shape of the driving pulse and the response of the filter by proper design of the stabilizing electrical driver, but the resonance of the piezo element must be taken into account.

All of the FFP-TF’s features together with its high capacitance (~0.25-0.5 μF) were folded into building a special high-speed stabilization controller to get a ‘clean’ square waveform of the driving electrical signal and decrease the PZT’s resonance. The driver is designed to drive a single large capacitance piezo element, though maximum values of capacitance should not exceed 0.5 μF. Depending on the FSR of the filter under test, up to three drive levels can be selected by digital control. Normally two levels are used for FFP-TF evaluation. These levels are manually adjusted between 1.5 volts and 5 volts, then applied to a gain of 5 driver to provide a 7.5 to 25 volt range to match the FSR of the piezo element. Levels below 7.5 volts are obtainable by changing circuit constants. This DC level is then applied to a variable bandwidth 8-pole Bessel filter, adjustable from 1 Hz to 100 kHz with a user operated control/readout. To decrease the PZT’s resonance the Bessel filter smoothes the edge transitions of the DC voltages before applying them to the output stage final circuit. The control of the variable bandwidth filter is managed by digitizing a zero to 5 volt signal to provide an 8 bit digital control word to the filter. The control word invokes one of the 256 bandwidths the filter can provide. Ringing and overshoot are thus controlled at the output when the filter drives the final stage with the amplified DC voltage.

In order to drive large capacitive loads successfully, a special output stage is required. This driver uses an Apex PA-51 device. It can drive over the full temperature range of -
55 to +125 degrees C. Current limiting resistors of 0.8 ohms were chosen to prevent damage to the device when subjected to very large capacitive loads. Additional current drive above the 1 amp level is available. Typical slew rate is 1.5 V/μs. There is a feedback feature that was not enabled yet but can use a DC "carrier present" voltage provided by an optical receiver. This input would enable the filter driver to make minute changes needed to track temperature drift in the laser source, or aging effects, such that optical carrier strength is always optimized at the receiver. Such a circuit would be needed in any commercial telecommunications system.

The resultant controller substantially improves the shape of the driving signal and the response of the filter. It helps to enable tuning of the high-speed FFP-TF three-orders-of-magnitude faster than that possible with standard commercial FFP-TFs.

**FFP-TF's performance evaluation**

In our experiments we evaluated the response time (TF) of the filter over the FSR for different FFP-TF's constructions.

**Scanning regime.**

A triangle wave is the easiest regime for the filter. The fast rising and falling edges of a low-frequency square-wave electrical signal were used to rapidly scan the filter for the speed response. Initially, the driving slew rates and amplitudes were carefully adjusted to minimize the optical resonance due to electrical waveform ringing and internal effects.
Figure 2-38
(a) Fastest response time for TF5 without excess optical ringing with $T_{F0} = 3.9$ μs; (b) Fastest response time for TF5 with $T_F = 1.1$ μs (note the two sets of traces of different time scales).

The fastest response times ($T_{F0}$) thus achieved without optical ringing for one reference are generally <10 μs. As an example, the fastest response for TF5 is shown in Figure 2-38a, where $T_{F0} = 3.9$ μs. Further increase in driving slew-rates induces strong parasitic signals. The "ringing" is due to excessive voltage level as well as to internal effects such as excitement of PZT mechanical resonance. When the driving electrical signal is almost a step function, and then sharp stopping at a desired wavelength excites back and forth motion and it periodically changes the small air gap inside of the filter. It causes periodical opening and locking of the filter. The results of that are shown in Figure 2-38b, where $T_F = 1.1$ s.
Results in Table 1 show all response times reaching 1-2 μs and the clear advantage gained by using the low-mass MO’s FFP-TFs and LANL’s driver. Tuning speed versus driving slew rate plotted in Figure 2-39 reveals an ideal linear relationship for low-speed operations and a nonlinear, dramatic increase in tuning speed for high speed operations.

![Figure 2-39](Image)

*Figure 2-39*

Dependence of Tuning Speed on Driving Slew Rates for TF1, TF2, TF3, and TF5

We were able to compare the performance of LANL driver and an old MO’s FFP-TF controller. LANL’s driver substantially reduced the electrical oscillations of the driving signal and optical ringing in the filter thereby improving the response of the MO’s FFP-TFs by a factor of two to three orders of magnitude compared to the response obtained with the MO’s FFP-TF controller.

We also experimented with other tunable PZT Fabry-Perot filters. All of them had either substantially heavier mass or couple times higher than MO FFP-TF capacity. These reasons did not allow to tuning faster than at 100-200 μs even with use of LANL’s driver. Figure 2-40 shows the fastest response time achieved for E-TEK, Inc. Tunable optical Fabry-Perot Filter (TOFF) with $T_{PO} = 189.9$ μs.
'Off-on' and 'on-off' tuning regime.

'Off-on' and 'on-off' tuning experiments were performed for TF5. A single laser source with 1565 nm wavelength corresponding approximately 4.6 V for the first maximum and 21.9 V for the second maximum of the Airy function was used to monitor the optical throughput of the filter. Wavetek 80250 MHz pulse generator and LANL's driver were used to drive the filter.

The fastest 'off-on' switching time obtained for TF5 and 1565 nm source without the ringing was 44.0 μs when the filter was operating in the second FSR from 5.8 V to 21.9 V (Figure 2-41).

Using the same 1565 nm source in 'on-off' switching regime from 4.6 to 26.7 V (filter operated in the first FSR) reveals 13.7 μs fastest switching (Figure 2-42). Note that the peak on plot corresponds to the second maximum of the airy function when the scanning regime is applied.

Also a single laser source with shorter 1545 nm wavelength corresponding approximately 1.4V was used to monitor the optical throughput of the filter in 'on-off' regime. The same filter was driven from 1.84 V to 24.5 V. In this case the filter was able to switch as fast as in 8.4 μs without any ringing (Figure 2-43).
'Off-on' Optical Switching. Optical Response Achieved for TF5 and 1565 nm Source without Ringing $T_{F0} = 44.0 \, \mu s$.

Figure 2-41

'On-off' Optical Switching. Optical Response Achieved for TF5 and 1565 nm Source without Ringing $T_{F0} = 13.7 \, \mu s$.

Figure 2-42
Figure 2-43
‘On-off’ optical Switching. The Fastest Optical Response Achieved for TF5 and 1545 nm Source without Ringing $T_{F0} = 8.4 \mu s$

The experiments show that for the same mechanical loading, the low voltage PZT has a better overall performance compared to the higher voltage PZT in both the speed and voltage requirements.

**Tuning time versus wavelength separation**

Another set of experiments was carried out to measure tuning time, $T_t$, versus wavelength separation ($\Delta \lambda$) for (1) constant bias ($V_b$) and varying slew rate (SR), (2) constant SR, varying $V_b$. 
Figure 2-44

$T_t$ vs. ?? for (a) constant $V_b=12$ V, varying SR; (b) constant SR=2.95 V/μs, varying $V_b$.

Figure 2-44a shows the results for three different SR's: 1.95, 3.60, and 5.17 V/μs. The $T_t$ decreases with a higher SR. The $T_t$ also decreases with higher $V_b$ as shown in Figure 2-44b. In this filter the PZT has 15V/FSR tuning characteristics at 1550 nm wavelength. The tuning response at 1.5V bias reflects the nonlinear characteristics of the PZT at low voltage. On the other hand, at higher $V_b$, where PZT has more linear behavior, the tuning response becomes independent of the bias voltage. Over all, the tuning time over 23 nm is well below 10 μs.
3.0 CONCLUSION

In this program, we have accomplished many technical, packaging, and commercialization developments. In specific:

1. We have understood the fiber optic network requirements of HEP experiments and performed a joint experiment with Los Alamos National Laboratory, integrating Multilink's components into All Optical Packet Switching Networks developed by LANL. The obtained results had been presented at the CLEO conference in San Francisco.

2. We have analyzed the advantages and constraints of WDM based packet switching systems. These analyses have permitted us to find a good market niche for the developed components.

3. We have successfully developed next generation electrical components such as ATDM, novel architecture 10 Gb/s, and 2.5 Gb/s clock and data recovery, VCSEL driver, fully monolithic OEIC, and highly parallel (12-channel) OEO array.

4. We have developed a couple of opto-electronic transceiver interfaces. These interfaces have provided Multilink with several complete fiber optic WDM data links prototypes for demonstration.

5. We have also constructed an Optical in-Optical out transceiver prototype which allows us to regenerate optical data at a data rate of 9.953 Gb/s. This prototype not only demonstrates the potential of the developed technology, but also allows us to penetrate commercial markets at an accelerated pace.

6. We have studied the needs of current product markets and have directed our product development efforts to these niche market areas.
More importantly, within this program we have achieved two critical milestones that promise a greater opportunity for a successful product family based on the developed technology. These milestones are:

1. Based on a prototype developed during this program, Multilink Technology Corporation presented a detailed business plan to TRW, CTI, and Finisar Inc. to receive external funding and development support. CTI, and Finisar Inc., have submitted commitment letters to Multilink. Those companies are willing to provide more than $400,000.00 in external funding in order to support development and marketing during Phase II.

2. We have also demonstrated an OEEO prototype to MCI, located in Richardson, Texas. MCI expressed a high level of interest. Multilink had performed a preliminary prototype test at MCI’s facilities and prepared a complete system test. Assuming that Multilink will be able to satisfy all additional requirements, MCI is willing to make a purchase to integrate more than 1000 systems in 10 Gb/s networks at MCI during 1999.

To summarize, in this program we have not only achieved the many technical objectives, but also have addressed and aligned with Multilink’s business direction. Multilink will bring a product family based on the technology developed from this program into the Telecom and Datacom product markets with a strong market niche emphasis.