SAN098-1780 C
SAND--98-1780C

INGAAS/INP HETEROJUNCTION BIPOLAR TRANSISTORS FOR ULTRA-LOW POWER CIRCUIT APPLICATIONS

CONF-981108--

P. C. Chang, A. G. Baca, M. J. Hafich, and C. I. Ashby
Sandia National Laboratories, Albuquerque, NM 87112

For many modern day portable electronic applications, low power high speed devices have become very desirable. Very high values of f_T and f_{MAX} have been reported with InGaAs/InP heterojunction bipolar transistors (HBTs), but only under high bias and high current level operating conditions. An InGaAs/InP ultra-low power HBT with f_{MAX} greater than 10 GHz operating at less than 20 μA has been reported for the first time in this work. The results are obtained on a on a $2.5 \times 5 \mu m^2$ device, corresponding to less than 150 A/cm² of current density. These are the lowest current levels at which $f_{MAX} \geq 10$ GHz has been reported.

RECEIVED
AUG 10 1998
OSTI

INTRODUCTION

The increased demand for portable electronics has lead to the need for higher performance and portability. This requires low power consumption in addition to high device performance, and low-power, high-speed electronics becomes very desirable. However, the performance of semiconductor transistors deteriorate with decreasing current and voltage, forcing compromise between low power consumption and high device speed. Heterojunction bipolar transistors (HBTs) have shown good potential for low power applications, and they are the devices been investigated in this work. The goal of this work is a conventionally dimensioned ultra-low power HBT that would operate at less than 20 μA with a low supply voltage (less than 3 V). Operation of HBT devices below 100 μA is typically not reported, and the few devices that have been reported for low current operation have had emitter size less than 5 μm^2 for high current density operation.

Compared with conventional GaAs-based HBTs, InGaAs-based HBTs have lower turn-on voltages because the band gap of InGaAs is smaller than that of GaAs. Therefore, InGaAs-based HBTs have been chosen for this work. Both InP and InAlAs can be used as the emitter material. InP is chosen for this work for its low surface recombination velocity, and its low conduction band offset with InGaAs. The highest maximum oscillation frequency (f_{MAX}) with low operating current conditions that has been reported for InGaAs-based HBTs is 37 GHz for 35 μA using a 2.3 μm^2 emitter, corresponding to a current density of 1.5×10^3 A/cm² [1]. The highest f_{MAX} with the lowest current density reported is 50 GHz at 6.7×10^2 A/cm² on a 15 μm^2 emitter, corresponding to a current level of 100 μA [2].

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

MASTER

EXPERIMENTS

A matrix of different HBT structures have been fabricated and tested for optimization of the HBT structure for low power applications. The optimization parameters include emitter doping level (N_{DE}), collector doping level (N_{DC}), emitter thickness (H_E), and collector thickness (H_C). The most optimized layer structure obtained to date is shown in Figure 1.

Contact Layer	$n^+:\text{InGaAs}$	$4 \times 10^{19} \text{ cm}^{-3}$	50 nm
Emitter Layer	$n^+:\text{InP}$	$2 \times 10^{19} \text{ cm}^{-3}$	50 nm
	$n:\text{InP}$	$7 \times 10^{17} \text{ cm}^{-3}$	150 nm
Base Layer	InGaAs	undoped	25 nm
	$p^+:\text{InGaAs}$	$4 \times 10^{19} \text{ cm}^{-3}$	50 nm
Collector Layer	$n:\text{InGaAs}$	$3 \times 10^{16} \text{ cm}^{-3}$	500 nm
Subcollector	$n^+:\text{InGaAs}$	$2 \times 10^{19} \text{ cm}^{-3}$	600 nm
S. I. InP Substrate			

Figure 1 : The HBT layer structure used for this work.

The samples were grown by an AIXTRON MOVPE system. Arsine and phosphine gas were used as sources for arsenic and phosphorus. Triethylgallium and trimethylindium were used to supply gallium and indium. Disilane and dimethylzinc were used to provide the Si and Zn as n-type and p-type dopants, respectively. Due to the excessive nonequilibrium group III interstitials produced by the heavy n-type doping in the subcollector, abnormal Zn outdiffusion from the base would occur as these group III interstitials diffuse into the subsequently grown base layer [3]. To suppress the Zn diffusion, a 30 minutes growth interrupt under arsine flow was used at the end of the subcollector layer to anneal out the excessive group III interstitials before the growth of the base layer. To further reduce the Zn diffusion, the substrate growth temperature ~~were~~ ^{was} lowered to 550°C from 600°C after the growth of the collector and subcollector layers. The resulting Zn profiles were examined with secondary ion mass spectroscopy (SIMS),

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

and with the base-emitter diode turn on voltage (V_{BEon}). Large improvements were obtained with diffusion-minimizing procedures; however, some Zn diffusion still occurred. A 25 nm undoped spacer layer was needed to accommodate it. The spacer layer reduces the device's speed, but it is desirable to achieve the low turn on voltage for low power applications.

The devices were fabricated using a self-aligned process. WSi was used as the emitter metal instead of GeAuNiAu because wet etching was used for the emitter mesa etch. The use of WSi avoided the excessive undercutting caused by the electrochemical effects. Wet etching was also used for the formation of the base and collector mesa. Phosphoric acid and hydrochloric acid solutions were used for selective etching of InGaAs and InP, respectively. TiPtAu and PdGeAu were used to form non-alloyed ohmic contacts to the base and subcollector layers, respectively. For surface passivation, a room-temperature ECR silicon oxynitride (SiN_xO_y) was developed. It was found that excessive surface and junction damage occurs during the conventional SiN_xO_y deposition, which is performed at 250°C under high plasma power. High temperature process produces excessive surface recombination currents that deteriorate device performance [4]. The room-temperature ECR SiN_xO_y process combined with a buffered oxide pretreatment suppressed the excess surface recombination current significantly. This is particularly important for small area devices in which surface recombination current is a more dominant factor.

The DC performance of these devices were tested using the HP4145B semiconductor parameter analyzer, while the RF characteristics were tested using Cascade probes connected to the HP8510 network analyzer. The s-parameters of these devices were measured from 0.5 to 50 GHz for different bias condition. The RF characteristics were then extracted from the measured s-parameters to obtain the values of f_T and f_{MAX} . The results of all the samples were then compared and the optimized HBT structure was determined.

RESULTS

Gummel plots and common-emitter I-V data for the optimized HBT structure are shown in Figure 2. This structure has a maximum common emitter current gain (β) of 24 at approximately 10 mA, and at low current level of 10 μ A, the β is approximately 3, as shown in Figure 2. The ideality factor for base current (I_B) and collector current (I_C) are 1.05 and 1.1, respectively, indicating minimal base-emitter junction damage from the SiN_xO_y deposition. The turn on voltage is less than 0.3 V, indicating the Zn dopants are confined in the base layer. The common emitter I-V plot shows the offset voltage is less than 0.2 V, and the saturation voltage is around 0.3 V. Both the offset and saturation voltate are low and suitable for low power applications.

Figure 2 : Gummel plot and common emitter I-V plot for the HBT structure used in this work.

The RF characteristics were extracted from the s-parameter measurement. The ultra-low power HBT was tested at $18 \mu\text{A}$, corresponding to a current density of 147 A/cm^2 , and the collector bias is set at 1.5 V . Under these bias conditions, f_T of 1.7 GHz and f_{MAX} of 10 GHz were obtained. This result is shown on the chart in Figure 3. This is the lowest current density at which f_{MAX} as high as 10 GHz has ever been reported, making this the first ultra-low power component suitable for portable RF electronics.

Figure 3 : A summary chart of the value of f_{MAX} of the low power InGaAs/InP reported by different groups [5-10].

CONCLUSION

An InGaAs/InP technology has been developed ultra-low power electronics. The resulting f_{MAX} of 10 GHz at 18 μA or 147 A/cm 2 , at a supply voltage less than 2.1 V represents the lowest power operation reported, suitable for ultra-low power RF electronic circuits.

ACKNOWLEDGEMENT

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

REFERENCES

- [1] H. Ito, S. Yamahata, N. Shigekawa, and K. Kurishima, Jpn J. Appl. Phys., **35** (12A), 6139 (1996).
- [2] T. Iwai, H. Shigematsu, H. Yamada, T. Tomioka, K. Joshin, and T. Fujii, Jpn J. Appl. Phys., **36** (2), 648 (1997).

- [3] K. Kurishima, H. Nakajima, S. Yamahata, T. Kobayashi, and Y. Matsuoka, Appl. Phys. Lett., **64** (9), 1111 (1994).
- [4] A. Ouacha, M. Willander, B. Hammarlund, and R. A. Logan, J. Appl. Phys., **74** (9), 5602 (1993).
- [5] M. Ida, S. Yamahata, K. Kurishima, H. Ito, T. Kobayashi, and Y. Matsuoka, IEEE Transactions on Electron Devices, **43** (11), 1812 (1996).
- [6] M. Hafizi, IEEE Transactions on Microwave Theory and Techniques, **45** (12), 2549 (1997).
- [7] Y. Matsuoka, S. Yamahata, K. Kurishima, and H. Ito, Jpn J. Appl. Phys., **35** (11), 5646 (1996).
- [8] J.-I. Song, M. R. Frei, J. R. Hayes, R. Bhat, and H. M. Cox, IEEE Electron Device Letters, **15** (4), 123 (1994).
- [9] Y. Miyamoto, J. M. M. Rios, A. G. Dentai, and S. Chandrasekhar, IEEE Electron Device Letters, **17** (3), 97 (1996).
- [10] U. K. Mishra, J. F. Jensen, D. B. Rensch, A. S. Brown, W. E. Stanchina, R. J. Trew, M. W. Pierce, and T. V. Kargodorian, IEEE Electron Device Letters, **10** (10), 467 (1989).

Keywords

HBT 1, 2, 3, 4, 5.

InGaAs 1, 2, 3, 5.

InP 1, 2, 3, 5.

ultra-low power 1, 3, 4, 5.

RF 3, 4, 5.