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## Stress Voiding During Wafer Processing

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## **Stress Voiding during Wafer Processing**

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### **Abstract**

Wafer processing involves several heating cycles to temperatures as high as 400°C. These thermal excursions are known to cause growth of voids that limit reliability of parts cut from the wafer. A model for void growth is constructed that can simulate the effect of these thermal cycles on void growth. The model is solved for typical process steps and the kinetics and extent of void growth are determined for each. It is shown that grain size, void spacing, and conductor line width are very important in determining void and stress behavior. For small grain sizes, stress relaxation can be rapid and can lead to void shrinkage during subsequent heating cycles. The effect of rapid quenching from process temperatures is to suppress void growth but induce large remnant stress in the conductor line. This stress can provide the driving force for void growth during storage even at room temperature. For isothermal processes the model can be solved analytically and estimates of terminal void size and lifetime are obtained.

## **Acknowledgment**

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## Introduction

Growth of voids in Al metallization has been observed to occur upon cooling from elevated temperature processing such as deposition of the passivation layer. Schroeder and Heinen (1) reported that with slow cooling from 450°C, voids first appeared at about 400°C. The voids appeared most often at passivation side walls and the void density remained constant throughout cooling. These observations are consistent with the suggestion by Flinn and others (2-4) that void nucleation is associated with a very small activation energy and this is most likely due to patches of organic contamination left by plasma etching. Schroeder and Heinen also observed that upon subsequent heating, above 150°C, the entire void population began to shrink and disappeared at approximately 350°C. Shrinkage of stress voids was first observed by Cuddihy et al. (5). Shrinkage by a stress-driven diffusive mechanism would necessarily involve a reversal of the metallization stress from tensile to compressive. This would be the case if, for example, the part was heated to a temperature higher than the passivation temperature of approximately 400°C. It would also happen if relaxation of tensile stress were to occur at a low temperature, over an extended period of time, followed by heating to a temperature lower than the passivation temperature. Local relaxation might occur if dislocations could glide and annihilate or if the passivation layer could slip over regions of metallization. The observed shrinkage of voids is compelling evidence that their growth and shrinkage is due to a stress-driven process.

The purpose of this report is to construct a model of stress voiding that could be used to simulate voiding behavior during and after wafer processing which involves several high temperature thermal excursions. It will be shown that void shrinkage can occur as an aftermath of significant stress relaxation. While direct comparison of void growth kinetics has proven difficult, certain symptoms of stress voiding have been observed and can be compared with model predictions. These symptoms include an asymptotic limit to growth, void closure, correct total volume fraction of void, void location at grain boundaries, and a correlation between average void size and average void spacing. Previous models of stress voiding (6-9) have been derived from solutions of the diffusion equation which are based on the assumption that void growth occurs isothermally. The model to be described is adaptable to any thermal treatment profile and only incorporates parameters that are available in the literature or easily measured. Quenching from process temperatures will be shown to suppress void growth but induces large stress. The model will be solved analytically for isothermal processes and estimates of life are obtained.

## Experimental

The correlation between average void size and average void spacing is very important because it relates to the nature of the interface between conductor and passivation. Measurements of void size and average spacing were made by B. McKenzie-1822 on three batches of as received parts obtained from Northrop-Grumman (NG). A total of 5991 voids on 20 parts were sized and averaged. A plot of the data is shown in Figure 1 and demonstrates a distinct correlation between void size and spacing. Voids that are widely spaced must provide more mass to relax stress in surrounding conductor line than

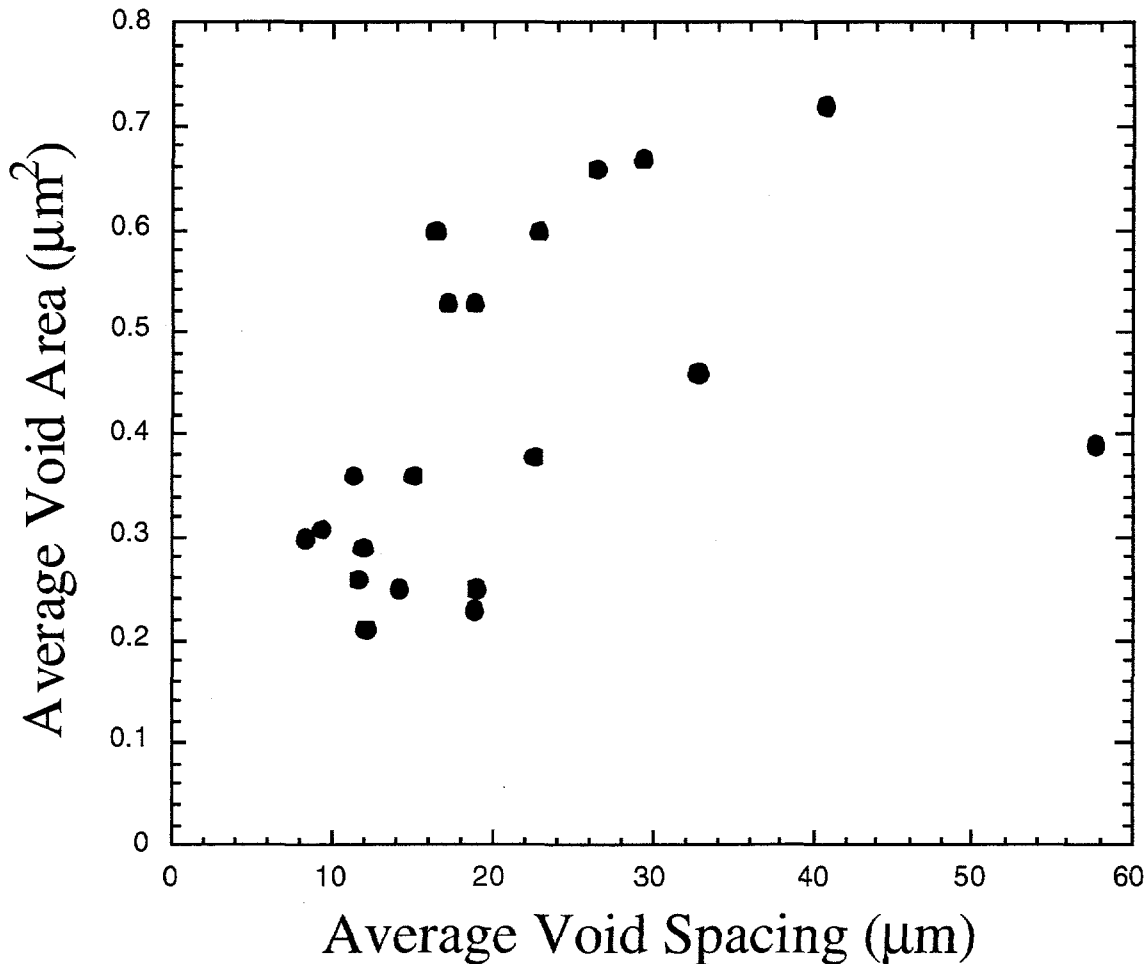


Figure 1. Average void area versus average void spacing. This correlation provides compelling evidence that stress voiding has occurred in these NG parts.

voids that are closely spaced. This yields a larger asymptotic limit to growth of widely spaced voids. This critical dependence on void spacing, which is ultimately determined by nucleation conditions, will be investigated with the model. Model calculations for the NG



thermal profile during wafer processing will also show why it proved unfeasible to induce void growth experimentally.

### Development of the Model

Although it is not currently possible to measure stress in conductor lines, thermal stress will be assumed to exist and will be incorporated in the model to follow. Consider a void of size  $a(t)$ , as shown in Fig. 2, in a conductor having a thickness much smaller than  $a(t)$ , and a width,  $b$ . The area of this void would, within a constant multiple, be equal to  $A(t) = a^2(t)$ . The conductor line is assumed to be under tensile stress due to the passivation layer which lies over it. Mass from the void surfaces is transported into a grain boundary to relax the local tensile stress. To ensure mass conservation in this process, an increment of mass removed from the void surfaces must equal that added to the grain boundary. From Fig. 3, this conservation yields

$$2a(t)da(t) = \{b - a(t)\}dy(t)$$

or

$$\frac{dy(t)}{dt} = \frac{1}{b - \sqrt{A(t)}} \frac{dA(t)}{dt} \quad 1.$$

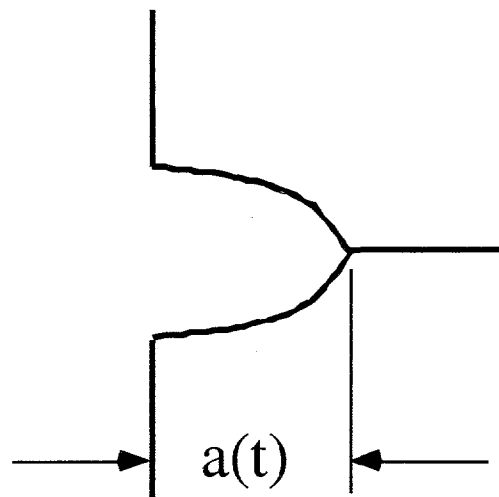


Figure 2. Illustration of a void growing from the side of a conductor line into a grain boundary.

The void population will be assumed to nucleate on contamination patches, as discussed above, and because the activation energy for this process is very small, all voids will appear at roughly the same time after the commencement of thermal treatment. This is consistent with the observation by Schroeder and Heinen that void density remains constant

throughout cooling. Further, it will be assumed that voids are uniformly distributed over the length of the conductor line such that

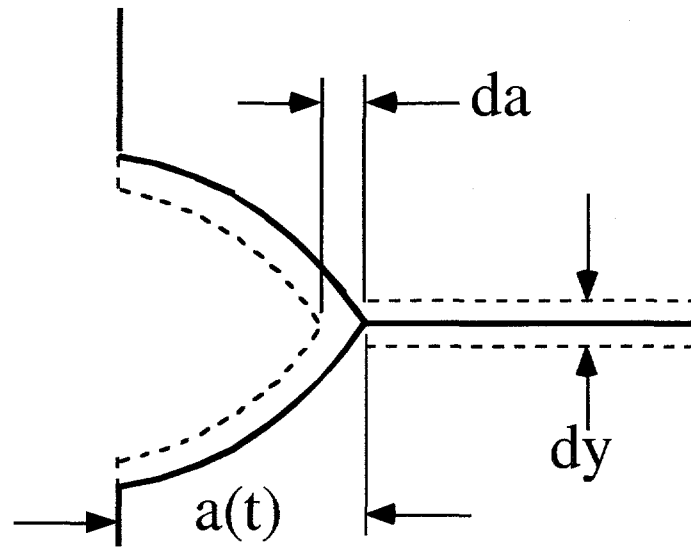


Figure 3. Mass transported from the void surfaces must equal that added to the grain boundary.

an average void density and spacing can be defined. The average void spacing is illustrated in Fig. 4.

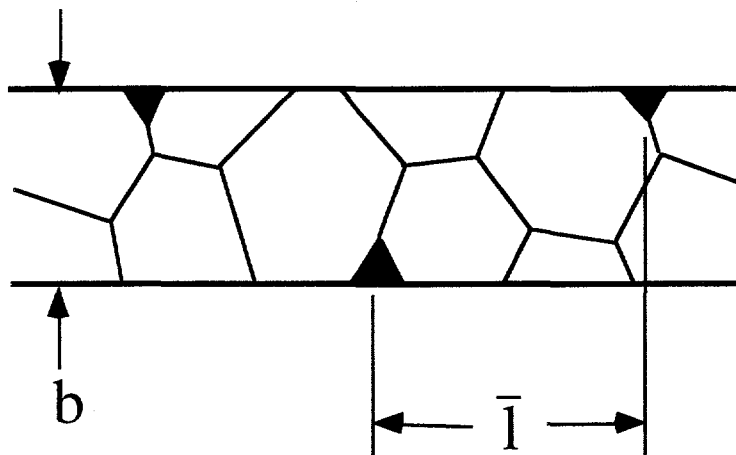


Figure 4. Illustration of voids in a polycrystalline conductor line that are assumed to exhibit an average spacing,  $\bar{l}$ .

The local strain rate can be written

$$\dot{\epsilon} = \frac{1}{\bar{l}} \frac{dy(t)}{dt}$$

and substitution into eq. 1 yields

$$\frac{dA(t)}{dt} = \bar{l} \{b - \sqrt{A(t)}\} \dot{\epsilon}. \quad 2.$$

It is important to recognize that this strain rate must be comprised of only those mechanisms which are capable of effectively adding mass to the grain boundary so that the void will grow. Stress driven mass transport and plastic deformation will both affect a void growth process but purely elastic deformation will not. This strain rate will be assumed to consist of diffusion and plastic deformation components and takes the form

$$\dot{\epsilon} = \dot{\epsilon}_d + \dot{\epsilon}_p \quad 3.$$

where the first term on the RHS is diffusive and the second represents the plasticity component. The diffusive component of the strain rate is the sum of Herring (volume diffusion) (10) and Coble (grain boundary diffusion) (11) strain rates given by

$$\dot{\epsilon}_d = \frac{10}{L^2} D_v + \frac{148}{L^3} \alpha D_b \frac{W s(t)}{kT} \quad 4.$$

where  $L$  is grain size,  $s(t)$  is conductor line stress,  $t$  is time,  $W$  is atomic volume,  $D_v$  and  $\alpha D_b$  are diffusion coefficients discussed in detail in Appendix A,  $T$  is absolute temperature, and  $k$  is Boltzmann's constant. The plasticity component, in the form of power-law creep, is provided by Frost and Ashby (12) as

$$\dot{\epsilon}_p = L \frac{D_v m v_b}{kT} \frac{s(t)^m}{L m} \quad 5.$$

where  $L$  and  $m$  are experimentally obtained constants,  $m$  is the shear modulus, and  $v_b$  is the magnitude of the Burger's vector (for Al  $v_b = 4.05 \times 10^{-8}$  cm). The effective stress is given by a constitutive relation of the form

$$\frac{ds}{dt} = -D\alpha(T)E(T) \frac{dT}{dt} - M_1(T)E(T)s(t) - M_2(T)E(T)s^m(t) \quad 6.$$

where the first term represents evolution of elastic stress and the second and third terms correspond to the strain rate terms in eqs. 4 and 5. The quantity  $D\alpha(T)$  is the thermal expansion coefficient of Si subtracted from that of Al and  $E(T)$  is Young's modulus for Al. The coefficients of thermal expansion were obtained from the Purdue series (13) for the temperature range 293-700 K and fitted to a fourth order polynomial in temperature. Young's modulus data for Al in the range 300-700 K was obtained from the compilation edited by J. A. King (14) and fitted to a linear function of temperature. The results are

$$D\alpha(T) = 19.9912 + 0.0286T - 0.0001707T^2 + 5.7294 \times 10^{-7}T^3 - 5.6222 \times 10^{-10}T^4 \text{ (K}^{-1}\text{)}$$

and

$$E(T) = 71393 - 39.922T \text{ (MPa)}.$$

The shear modulus was taken to be  $3E(T)/8$  and the values  $L=3.4 \times 10^6$  and  $m=4.4$  were found in (12). Equations 2-6 constitute the model for void size and conductor line stress evolution.

### Results

Each process during wafer manufacture is characterized by a certain thermal history. If the temperature rate of change is expressed algebraically as a function of time this equation can be solved simultaneously with eqs. 2-6 to obtain the temperature, void size and stress as a function of time. This set of solutions can be obtained for each specific manufacturing and test process, including such simple processes as a constant temperature anneal or storage period. The final states of any given process can be used to provide initial conditions for the subsequent process. The passivation, sinter, and aging temperature profiles are shown in Fig. 5-7.

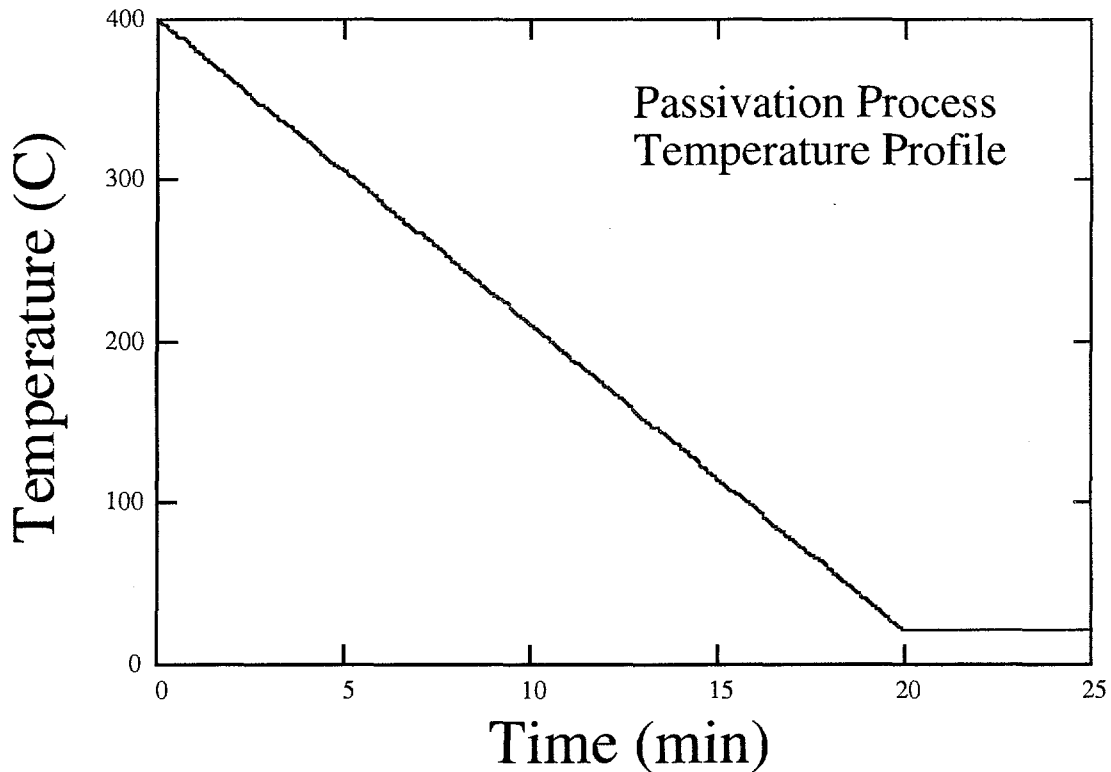


Figure 5. The temperature profile directly following the 400°C passivation deposition process.

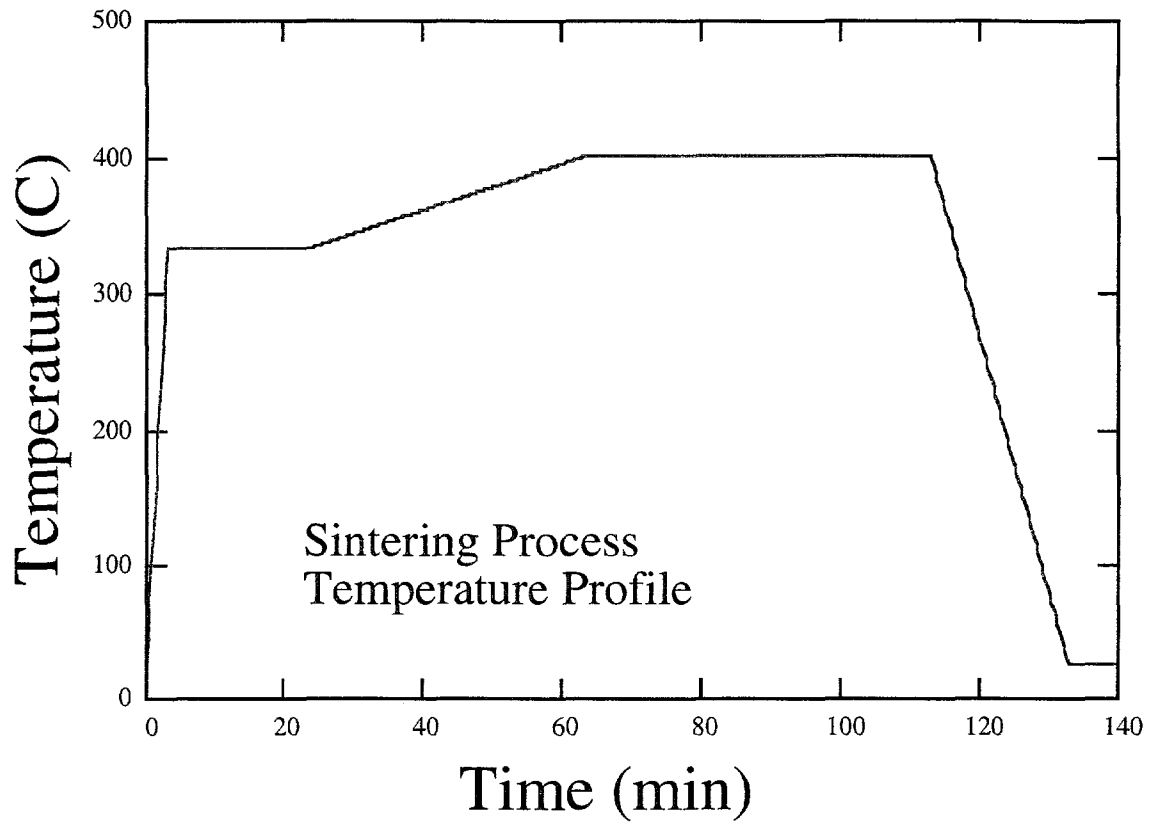


Figure 6. The temperature profile during the sintering process.

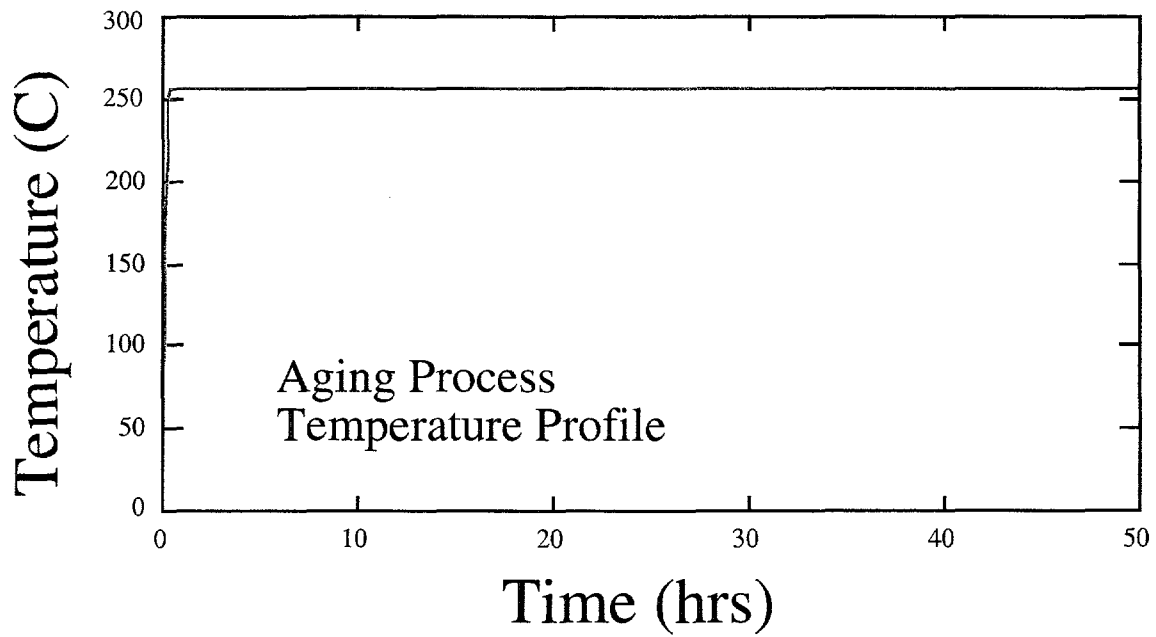


Figure 7. The temperature profile during the aging process.

The temperature profile for passivation, shown in Fig. 5, excludes the constant temperature (400°C) deposition process during which no stress or void growth can evolve. These profiles are close approximations to those used in the NG processes.

In all cases to be described in the following, Mathcad Plus 6 software was used to solve the rate equations. At small grain size, hence small activation energy (see Appendix A), such as that measured on NG product, the equations are stiff and the software did not perform well. Consequently, only grain sizes of 2  $\mu\text{m}$  and above will be discussed in the following. Alternative software would easily eliminate this problem so that void growth kinetics could be modeled for any reasonable grain size. It was also determined that the Herring component of the diffusive creep rate and the plastic component of the creep rate were both negligible compared to the Coble component.

#### *The Passivation Process*

The rate equations were first solved for the cooling stage of the passivation process. For this example, the conductor line was assumed to be 2 microns wide and the average void spacing was taken to be 20, 40, and 60 microns. The results of these computations are shown in Figures 8 and 9. Because there is more elastic energy to be relaxed, voids that are more widely separated grow faster and to larger extent than do narrowly spaced voids.

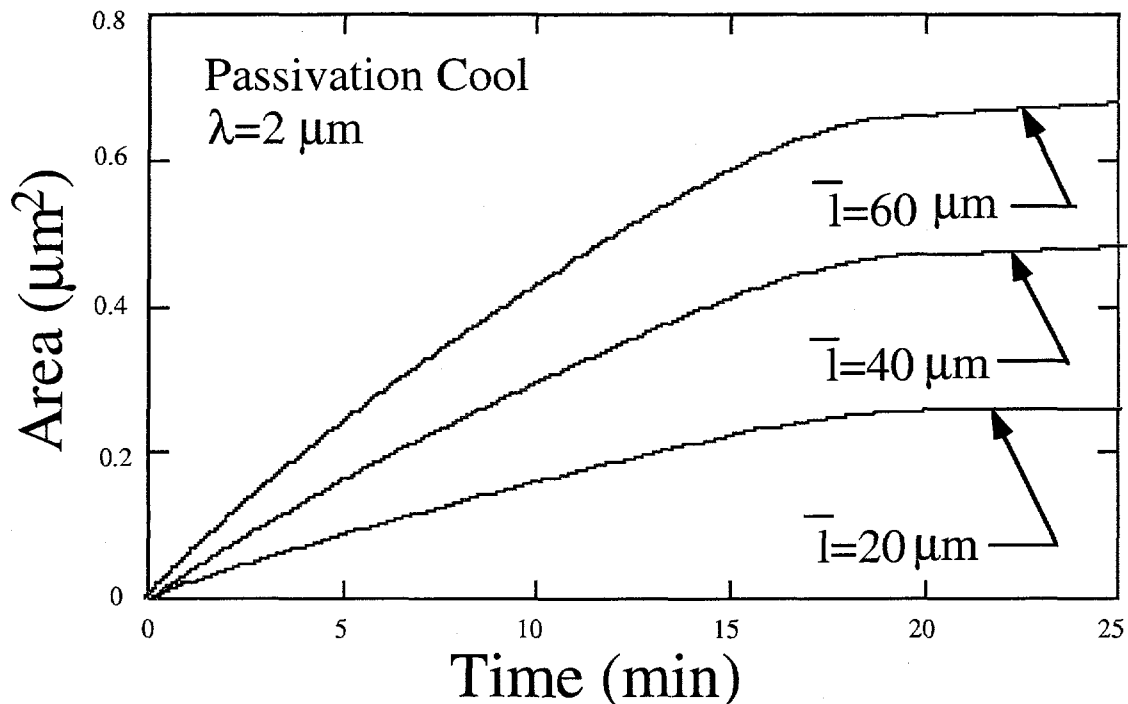


Figure 8. Void growth during the cool from the passivation temperature. Widely spaced voids grow faster and to a larger extent than narrowly spaced voids.

Void growth is seen to asymptotically approach a limit due to the slowing of diffusion as temperature approaches room temperature. Figure 9 demonstrates that the remaining stress relaxes very quickly during void growth, even when cooling is complete at room temperature. These stress relaxation kinetics were found to be independent of void spacing. At larger grain sizes and activation energies for grain boundary diffusion, these kinetics were much slower as shown in Figure 10. In addition, the stress relaxation rate

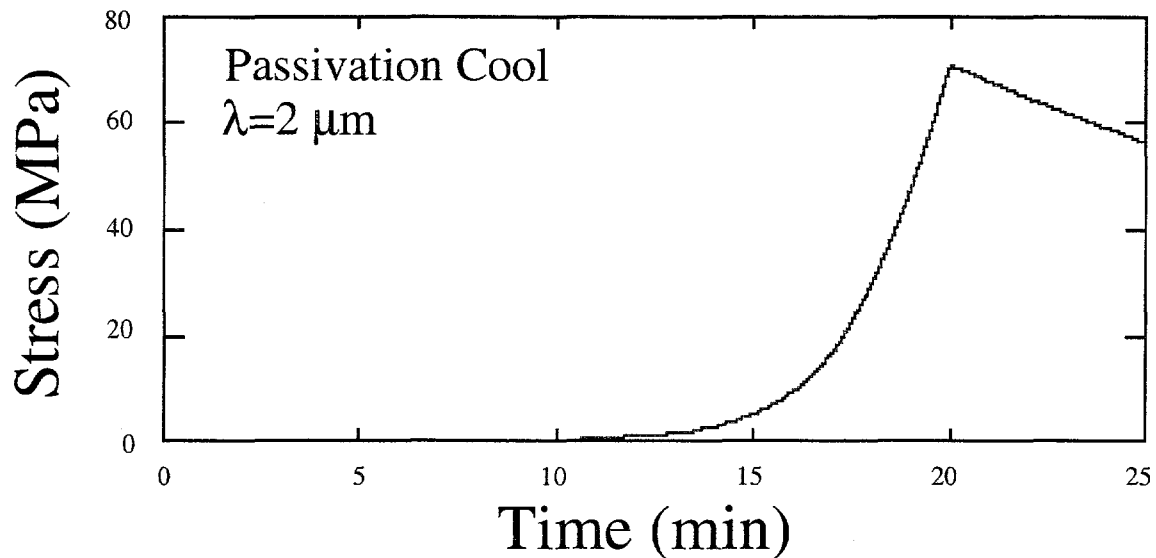


Figure 9. Evolution of stress during the cool from the passivation temperature. Note that the stress increases in a nonlinear way due to the simultaneous relaxation that occurs as a result of void growth.

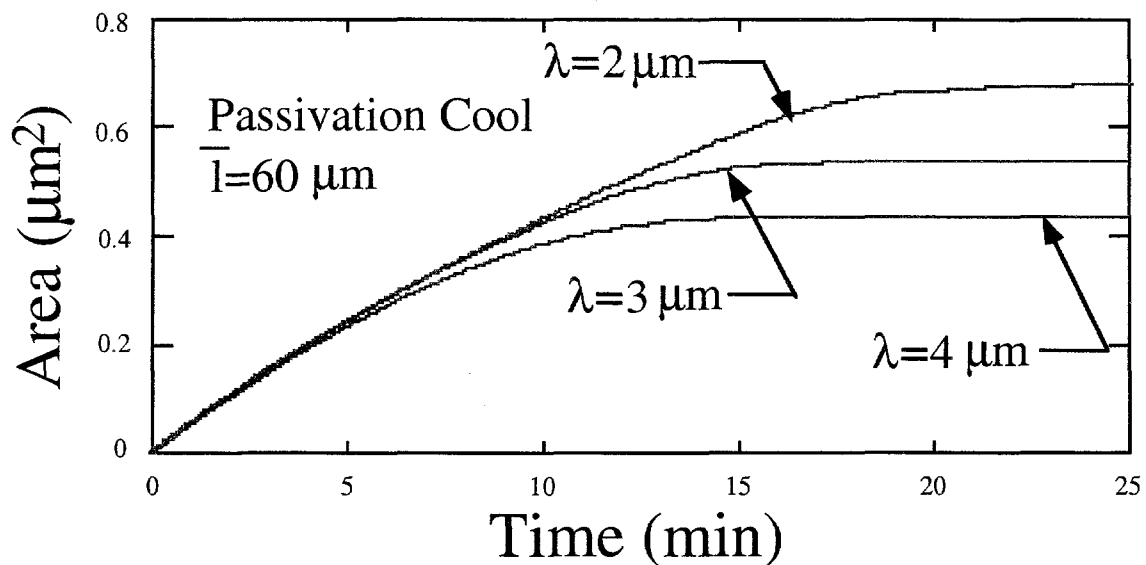


Figure 10. Void growth rate and extent depends sensitively on grain size.

was found to depend upon grain size as can be seen in Figure 11. At a grain size of 2  $\mu\text{m}$ , stress relaxed to approximately 12 MPa after 45 minutes at room temperature while for  $\lambda=4$   $\mu\text{m}$ , stress relaxation was barely perceptible after the same length of time and temperature.

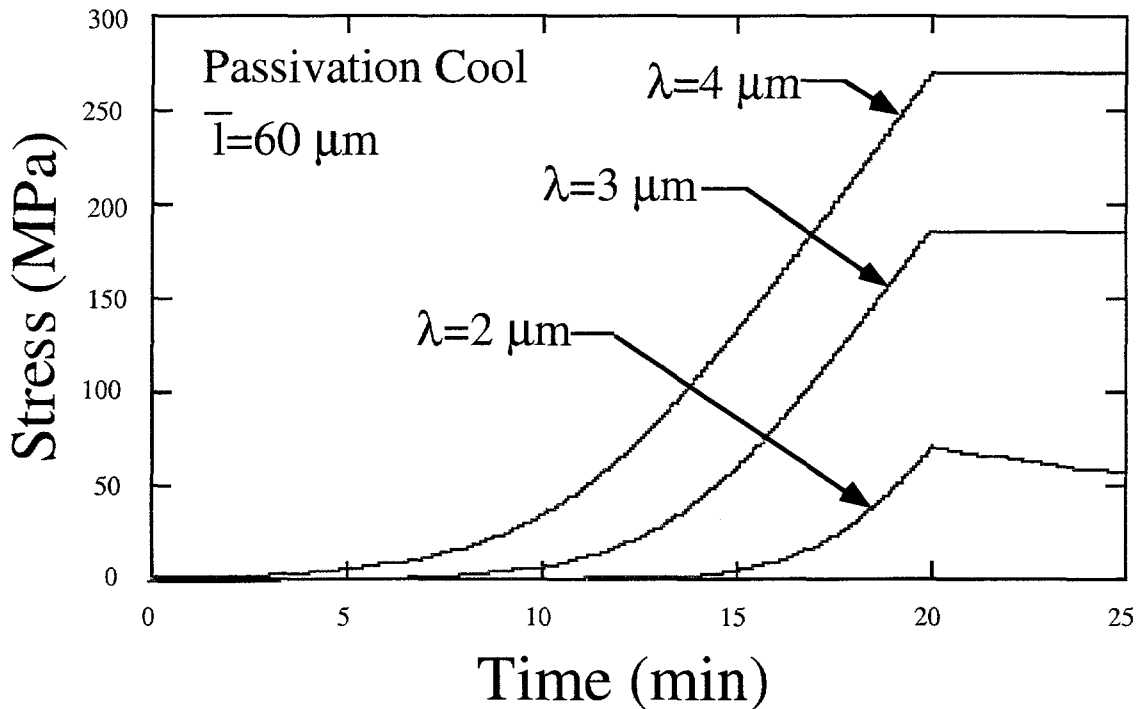


Figure 11. Stress evolution and room temperature relaxation kinetics depend sensitively upon grain size.

#### *The Sinter Process*

It was shown above that, depending on grain size or activation energy, stress relaxation can be very rapid. It is conceivable that for small grains, stress can relax to zero during some short period of time following the passivation process. This will mean that the initial conditions for the sinter process will involve zero stress. During the heating stage of the sinter process the conductor line metallization would be expected to go into a compressive stress state, thus reversing the diffusion direction such that void shrinkage will occur as was observed by Schroeder and Heinen (1) and by Cuddihy et al. (5). At larger grain sizes, stress relaxation during the passivation cool will be slower and, in most cases, stress will not go to zero. Upon heating during the sinter process, stress will eventually become compressive and void shrinkage will occur. To simulate void shrinkage, the first 5 minutes of the sinter process was examined with an assumed grain size of 3.5  $\mu\text{m}$  and an average void spacing of 60  $\mu\text{m}$ . Void shrinkage and stress relaxation are illustrated in Figure 12.



From 23 minutes into the sintering schedule until 63 minutes there is a slow temperature rise during which voids continue to shrink to zero size. Stress goes slightly compressive then relaxes to zero again. During the isothermal span between 113 minutes to 133 minutes void size and stress remain at zero. The cool from approximately 250°C induces void growth and evolution of tensile stress similar to that during the passivation cool.

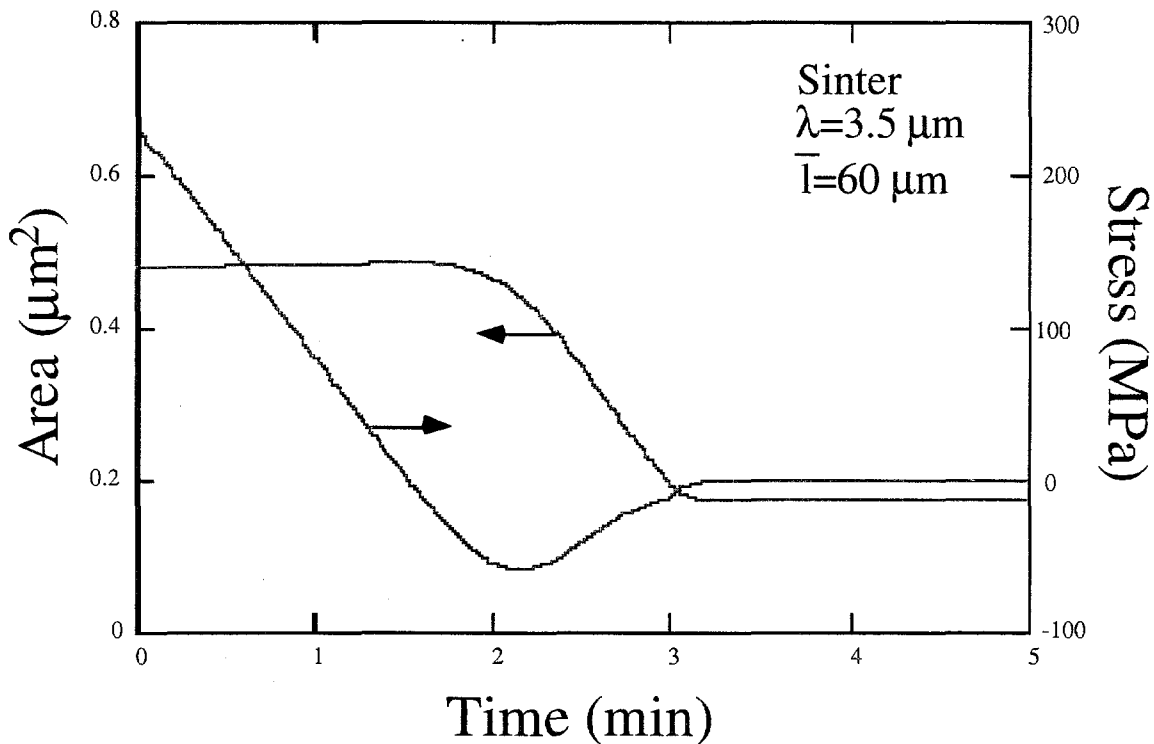


Figure 12. Heating during the initial stage of the sinter process induces void shrinkage as a result of prior stress relaxation. It also induces stress relaxation and evolution of compressive stress.

#### *Quench Rate Effect*

In their studies of void growth and shrinkage, Cuddihy et al. (5), discovered that by heating and then quenching voided parts all traces of the pre-existing voids were eliminated and all conductor lines were left completely intact. This phenomenon can be explained in the context of the model developed here. During the heating portion of the Cuddihy experiment, compressive stress evolved and caused void shrinkage as discussed above. To investigate the effect of the quench, the passivation cool process was modified by increasing the rate of cooling from the process temperature of 400°C. Void size and stress after quench rates as high as  $10^4$  °C/min are plotted versus quench rate in Fig. 13. From this figure it can be seen that while heating and quenching “heals” conductor lines it is

surely not a problem remedy as was suspected at the time of the Cuddihy discovery. Since tensile stress is restored by the quench, voids are able to begin growing once again given sufficient time and temperature.

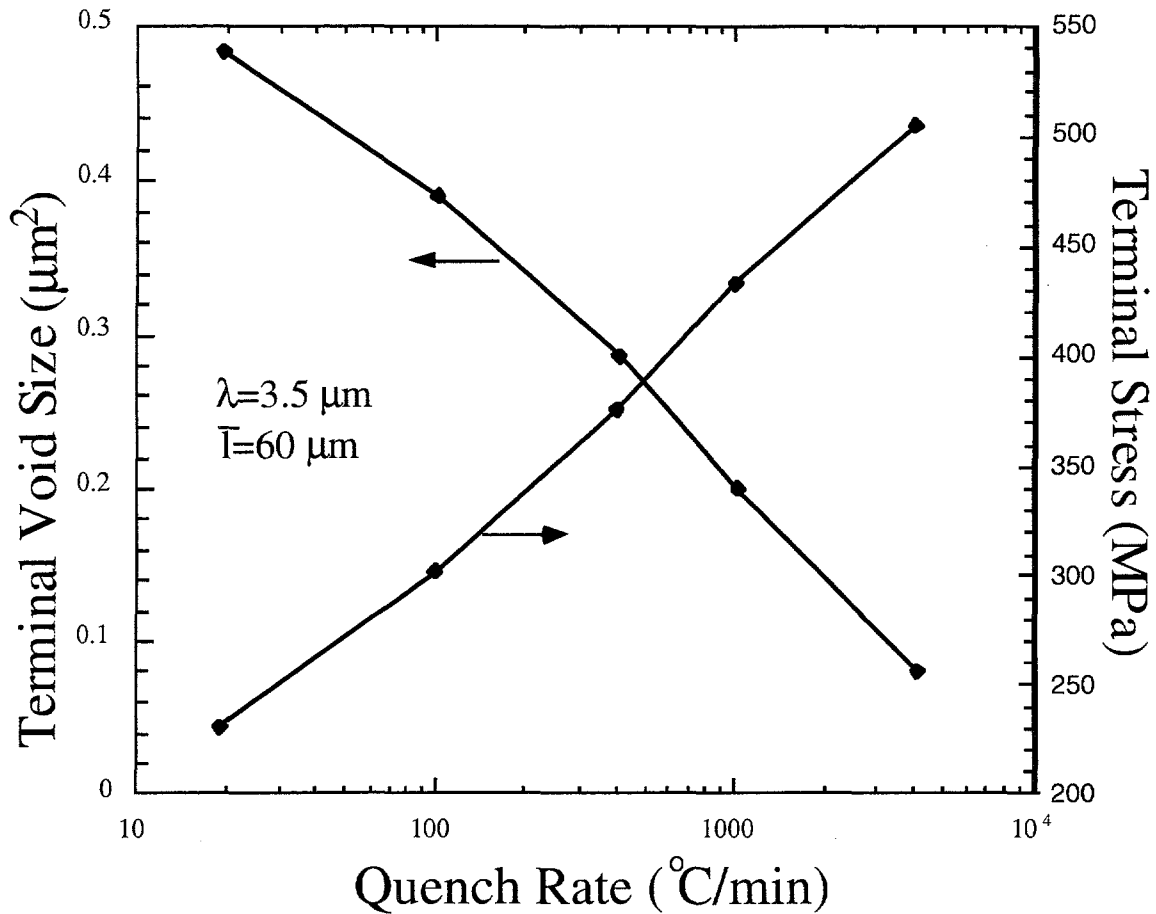


Figure 13. Quenching from 400°C at increasing rates results in smaller voids since there is less time available for growth to occur during the cooling process. It also results in larger tensile stress that can lead to void growth if stress is not relaxed in some other manner.

#### Isothermal Processes

If circumstances allow existence of an initial tensile stress,  $s_o$ , during the isothermal portion of the sinter process, Eqs. 2-6 become decoupled and can be solved analytically. The solutions are

$$\sqrt{A_o} - \sqrt{A(t)} - b \ln\left(\frac{b - \sqrt{A(t)}}{b - \sqrt{A_o}}\right) = \frac{\bar{I}s_o}{2E}(1 - \exp(-Y Et)) \quad 7.$$

$$s(t) = s_o \exp(-Y Et) \quad 8.$$

where

$$Y = \frac{148cD_bW}{l^3kT} 10^7 (\text{MPa s})^{-1}.$$

These equations can also be applied to any other isothermal process. One very important isothermal process is storage at room temperature. If it is assumed that a part is cooled after the passivation process and the conductor lines exposed to a tensile stress of 575 MPa, Eq. 7 can be used to compute the final void size after a very long time at room temperature. Letting the initial void size equal zero, and with use of the same parameters as were used in the calculations above, the final void size was computed as a function of average void spacing and shown plotted in Fig. 14. Superimposed on the curve are the data obtained from NG parts and discussed earlier. The data compares quite favorably with the model

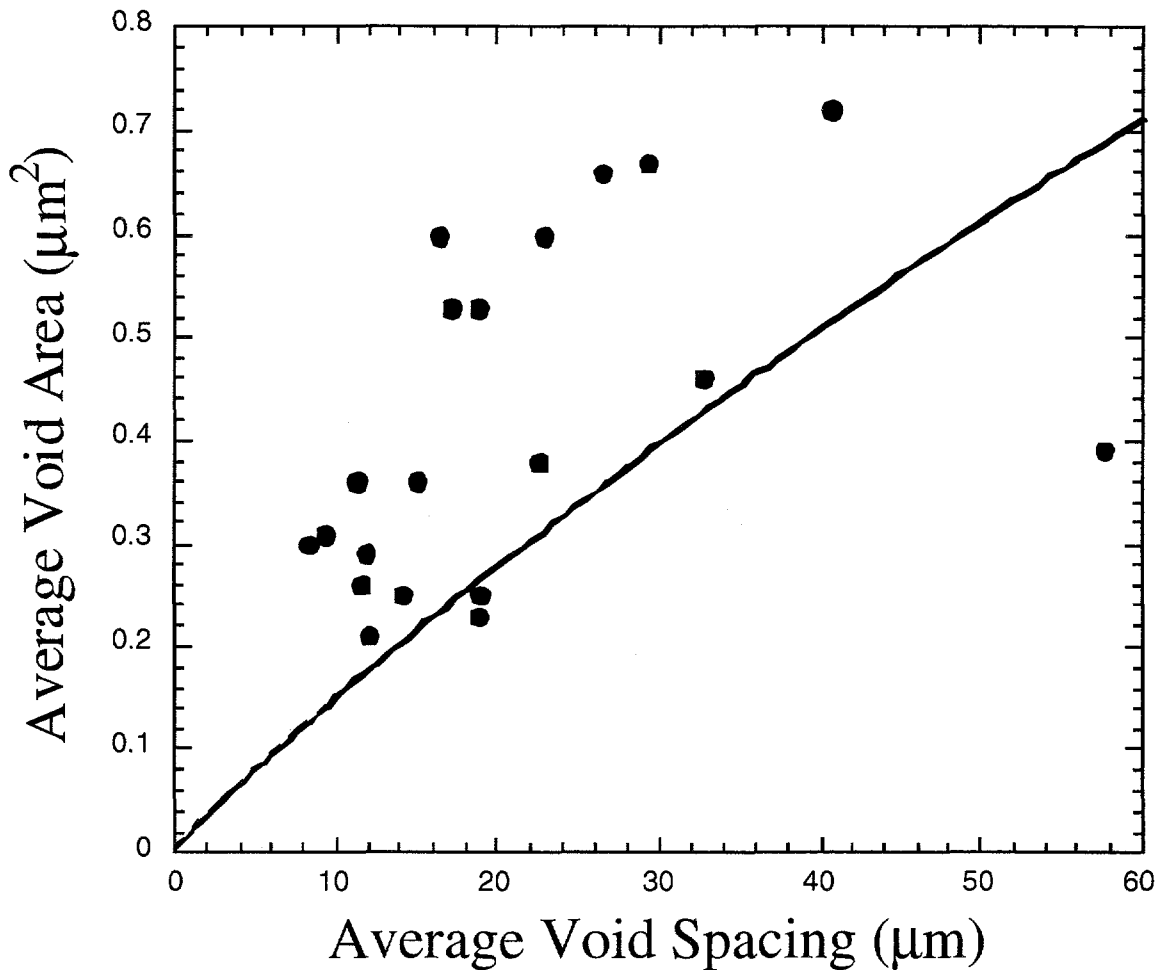


Figure 14. Void size measurements taken from NG parts compare favorably with prediction obtained from the isothermal void growth model.

prediction given that no adjustable parameters were used. Equation 7 can also be used to provide an estimate of lifetime if failure is defined as void growth to a certain critical size. If, for example, failure is defined as growth to 90% of the conductor line width,  $b$ , then the time necessary to reach this size is the failure time.

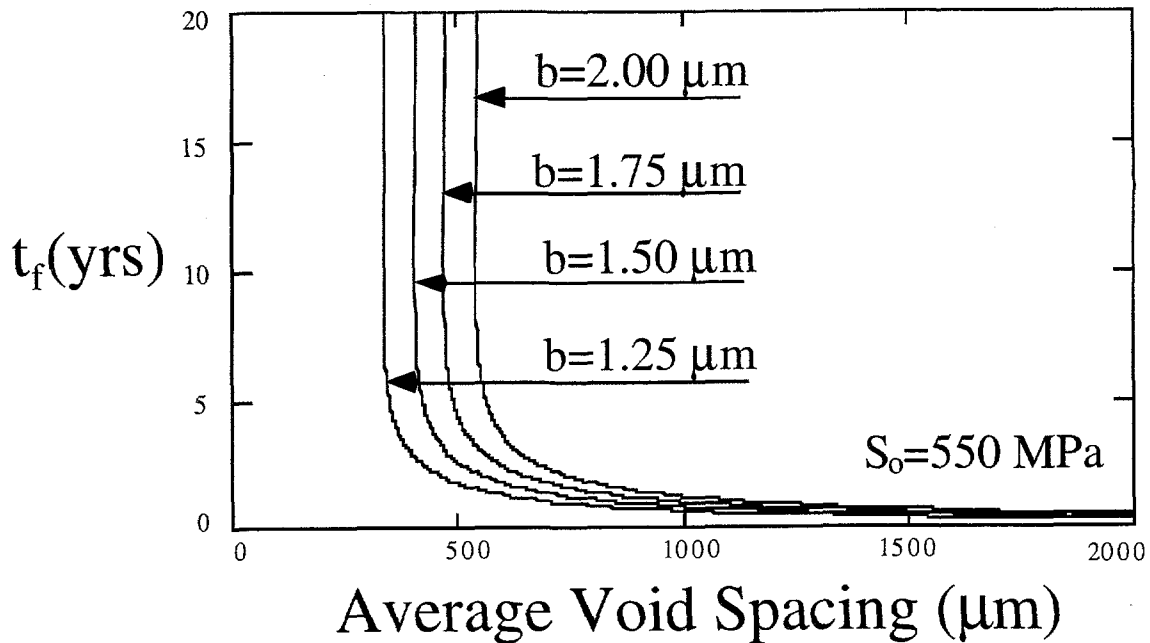


Figure 15. Lifetime in years plotted versus average void spacing for different conductor line spacings and an assumed initial stress of 550 MPa.

It can be seen from Figs. 15 and 16 that below a critical value of conductor line width and initial stress the lifetime is infinite. Above these critical values it can be extremely short.

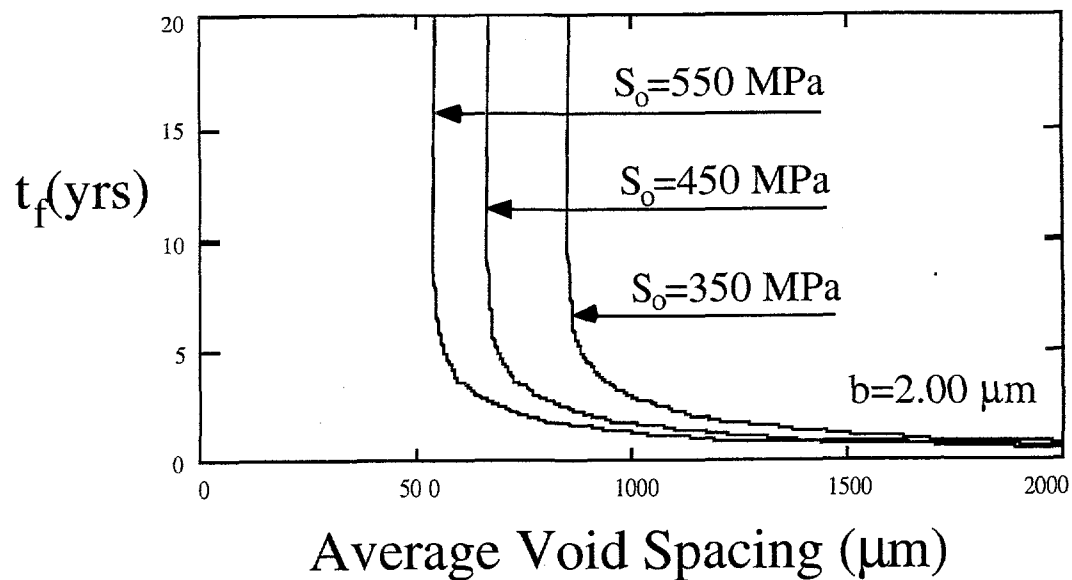


Figure 16. Lifetime in years plotted versus average void spacing for different initial stresses and an assumed conductor line width equal to that in NG parts.

### Discussion and Conclusions

The source of stress/strain in aluminum metallization is the mismatch of thermal expansion coefficients at metal/glass interfaces. Calculations have shown that if these interfaces were totally bonded the energy barrier for void nucleation would be too high and voids would never be observed. This suggests that defects of many types, such as local debonding of the interface, act as nucleation sites for voids. These debonds may, for example, be due to residues from etch processes or small cracks in the glass passivation. Given the existence of these debonds it is natural to question if regions of debonding can be extended during subsequent processing, designed or accidental. Glass/metal interfaces are typically susceptible to damage caused by thermal excursions. It is likely that this damage will accumulate to some saturation level. Processes such as severe quenching and rapid cycling may be so effective in extending this damage that stress voiding is not observed, since thermal stress will be largely alleviated. Virtually all models of stress voiding in conductor lines assume that the metal/passivation interface remains intact throughout the life of the chip. This leads to large thermal stresses and consequent voiding with stress relaxation occurring only as a result of void growth itself. It would be useful to reconsider mechanical coupling of the interface by assuming that it can exhibit frictional slip and that the extent of slipping can increase as interface damage accumulates. A simple model was constructed with use of a statement for conservation of mass and a constitutive equation for conductor line stress. The model was used to study void growth and shrinkage behavior during wafer process thermal treatments at NG. Although it was determined that power law creep did not lead to significant stress relaxation other mechanisms, for example easy glide, may provide sufficient stress relaxation to further limit voiding behavior.

The initial temperature and cooling time from the passivation process is sufficient to grow voids in agreement with the observations of Schroeder and Heinen (1). The importance of void spacing on both the growth kinetics and ultimate void size was demonstrated. A result of void growth is stress relaxation which can occur rapidly even at room temperature if the activation energy for grain boundary diffusion is small. This relaxation may be the reason that experimental efforts to grow voids have proven difficult.

Stress relaxation occurs during void growth but also as a result of dislocation motion and interfacial slip. Upon heating the relaxed structure, a state of compressive stress is established. This results in void shrinkage and closure as observed by Schroeder and Heinen (1) and by Cuddihy et al. (5). Quenching from elevated temperature restores tensile stress but does not allow sufficient time for void growth. It would be tempting to begin a void growth experiment immediately following a rapid quench and before stress relaxation by other mechanisms destroys the driving force for void growth.

A void growth experiment, employing quenched specimens, could most conveniently be done isothermally. An isothermal treatment effectively decouples the model equations such that they can be solved analytically. These analytical solutions were used to compute the terminal void size as  $t_{fi} \approx$  at room temperature and an initial stress of 575 MPa (i.e. quenched from 400°C). The trend of the prediction agreed well with experimental void size determinations. The expected lifetime of a part was also determined by defining failure as growth of a void to 90% of the conductor line width. It was shown that lifetime is a very sensitive function of void spacing, conductor line width, and initial stress. Since these parameters can be viewed as stochastic, especially void spacing, it would be useful to modify the model to include such stochastic effects and to record local void spacing with each and every void size measurement.

A surprising result of this work was the apparent dependence of activation energy for grain boundary diffusion (electromigration) upon grain size which was found by combining IBM data from the literature (see Appendix A Reference 13) with data from work done by S. Yazzie-1728. It is to be expected that as grain size approaches the conductor line width, the activation energy for electromigration would change from that for grain boundary diffusion to that for volume diffusion. While the grain size of both the IBM and the Yazzie data were smaller than their respective conductor line widths, the possibility of a transition can not be ruled out. It is a result that begs experimental resolution.

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## Appendix A

### *Volume Diffusion Coefficient for Aluminum*

The volume or bulk diffusion coefficient has been measured or estimated by several workers (1-9). This coefficient is typically defined as

$$D_v = D_0 \exp\left(-\frac{Q_v}{RT}\right)$$

where  $D_0$  is referred to as the pre-exponential factor and  $Q_v$  as the activation energy. The results of these works are shown in TABLE A1.

TABLE A1 Published Volume Diffusion Data for Aluminum.

Reference	Activation Energy ( $Q_v$ , cal/mole)	Pre-exponential ( $D_0$ , cm <sup>2</sup> /s)
1	33909	1.6
2	29480	not given
3	34000	1.71
4	30650	not given
5	33190	not given
6	32270	not given
7	29480	0.047
8	28790	not given
9	31720	0.5

The most reliable technique for this measurement utilizes the isotope Al<sup>26</sup>. The first and third reference used the isotope method, provided both  $Q_v$  and  $D_0$ , and were in very good agreement with each other. The data provided in Table III of Reference 1 was the measured diffusion coefficient as a function of test temperature. This data was plotted and least squares fitted (by the authors) to an Arrhenius relation to obtain the data listed above as Reference 1. This was the data selected for use in model computations discussed in this report.

### *Grain Boundary Diffusion Coefficient for Aluminum*

Grain boundary diffusion measurements are much more scarce and indirect, being associated with electrotransport studies. The Handbook by Kaur et al. (10) provided several references, of which (11) was considered best in that it reviewed the available literature and referenced considerable work by IBM researchers. The grain boundary diffusion coefficient is generally described with an equation of the type

$$cD_b = cD_{ob} \exp\left(-\frac{Q_b}{RT}\right)$$

where  $D_b$  is the grain boundary diffusion coefficient and  $Q_b$  is the grain boundary diffusion activation energy, and  $c$  is referred to as the grain boundary thickness. Note that the  $c$  can be algebraically canceled from the above expression but grain boundary diffusion data are typically quoted in this form.

The IBM work demonstrated that the activation energy for electrotransport in thin Al films is dependent on temperature, grain size, and the extent and type of alloy addition, e.g. Cu (11-16). d'Heurle and Gangulee (11) found that the pre-exponential factor,  $cD_{ob}$ , is on the order of  $10^{-10}$  cm<sup>3</sup>/s. Attardo and Rosenberg(13) noticed an important correlation between grain size of thin film Al conductors and the activation energy for electromigration. For conductor lines having an average grain size of 2 μm they observed an activation energy of 0.51eV whereas for an average grain size of 8 μm they found 0.73 eV. This was shown to have important consequences in the electromigration lifetime of circuits they studied. Understandably, parts with larger grains showed longer life. Since electromigration occurs predominantly by grain boundary diffusion the observed activation energies are good approximations to that for grain boundary diffusion. Their observation points out the importance of measuring the average grain size and the distribution of "blocking grains" which are those that are as wide as the conductor line itself. To this end, transmission electron micrographs, taken in plan view of NG product, were obtained from T. Headley-1822 and used to make grain size measurements with the grain boundary intercept method(17). Grain size measurements were taken from 21 different conductor lines and yielded an average grain size of 1.19 μm. The activation energy for electromigration in NG parts was measured by S. Yazzie-1728 and found to be 0.39 eV. These activation energy and grain size measurements are plotted in Figure A1 and fitted to an empirical equation.



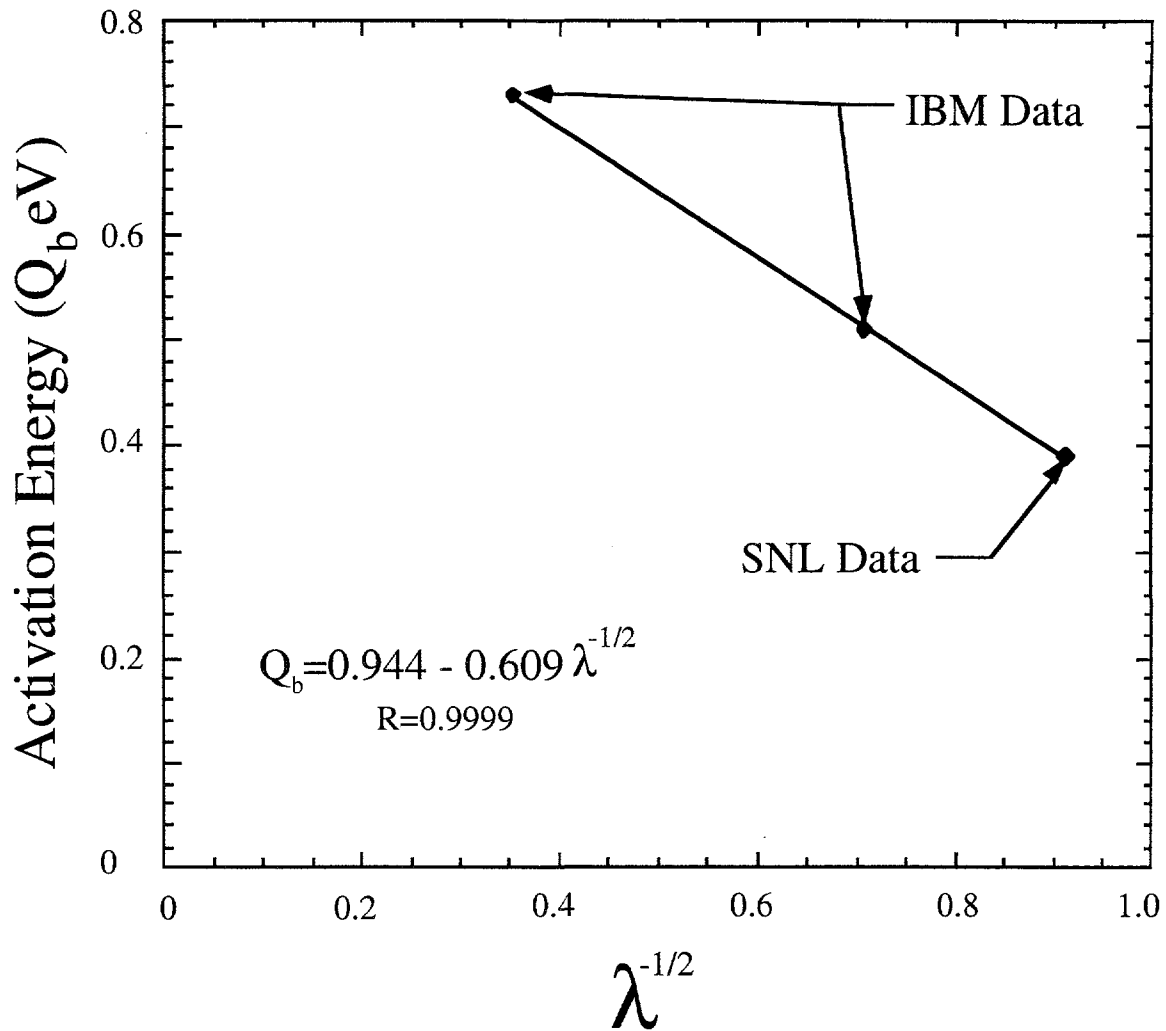


Figure A1. Measured activation energy for electromigration versus a simple function of average grain size of IBM and NG parts.

An excellent fit that empirically relates the grain boundary diffusion activation energy with grain size was found as

$$Q_b = 0.944 - 0.609 I^{-1/2}$$

where the units of  $Q_b$  are eV per atom and  $I$  is in microns. At this time no explanation is offered for this behavior. All model computations discussed in the report will utilize the above activation energy grain size functionality and a pre-exponential factor of  $10^{-10}$  cm<sup>3</sup>/s.

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