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GaAs Series Connected Photovoltaic Converters for High Voltage Capacitor Charging Applications

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GaAs Series Connected Photovoltaic Converters for High Voltage Capacitor Charging Applications

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Abstract

This report describes the design features of series connected photovoltaic arrays which will be required to charge capacitors to relatively high (400V) voltages in time periods on the order of 1 microsecond. The factors which determine the array voltage and the capacitor charge time are given. Individual element junction designs, along with an interconnect scheme, and a semiconductor process to realize them are presented. Finally, the input laser optical power required to meet the requirements is determined.

Acknowledgments

Support for this investigation was provided by the Advanced Fireset project, with the funding under the management of Scott Holswade, 2674. The report is part of a larger project which includes fabrication of proto-type arrays according to the designs contained herein. Semiconductor material layer growth is being done by John Klem (MBE) and Hong Hou (MOCVD) in the Compound Semiconductor Research Laboratory (CSRL) and device processing is being done by Walt Zuberzycki, under the direction of Stanley Kravitz, also of the CSRL. Device testing will be directed by W. J. Kass in Dept. 1235.

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GaAs Series Connected Photovoltaic Converters for High Voltage Capacitor Charging Applications

1.0 Introduction

This report describes the design features of AlGaAs/GaAs, series connected photovoltaic (PV) arrays intended to charge capacitors to relatively high voltages when illuminated with a laser. There are two principal advantages to pursuing this technology. First, placement of photovoltaic converter arrays in electrically isolated regions enables generation of electric power without electrical connection to the region. This prevents use of the system in ways other than that intended, and isolates the region from electromagnetic interference, a safety enhancement. Second, electric power can be generated in a far smaller volume than required by a dc-dc converter, resulting in a very large weight savings. One could use a standard, single junction solar cell, which would generate approximately one volt as the input to a dc-dc converter, and accomplish the same result. However, standard dc-dc converters contain a couple of transistors in a push-pull configuration to cause oscillation, which is input to the primary of a step-up transformer, and the secondary output is rectified by a diode bridge to obtain the dc output. The advantage in use of a monolithic array is apparent when the weight and volume of all these components are compared with a single semiconductor chip which is several mm across and a few hundred microns thick.

Initial exploratory development in this area was done previously and the results are reported in SAND92-1534, Monolithic, Series Connected GaAs Photovoltaic Power Converters for Optoelectronic Component Applications¹. These arrays consisted of a relatively small number of series connected junctions which would generate voltages of approximately 13 volts (12 junctions) at a short circuit current of 30 mA under illumination of about one watt of laser power at a wavelength of 810 nm. The applications for which these devices were intended consist of low voltage, real time electric power generation in a remote region. An example is given in the report. Also contained in the above cited report is a discussion of how a PV converter works, together with a closed form solution of the diffusion model of PV converter operation including loading effects.

These arrays consisted of wedge shaped junctions laid out in circular geometry and connected front to back by novel photolithographic techniques. The individual junctions were electrically isolated from one another by channels etched through the active region layers down to a semi-insulating substrate using standard semiconductor processing techniques. There are two disadvantages to this array geometry for use in high voltage applications. First, since in series connection the individual junction voltages add, high voltage applications require a large number of junctions in the series array. Contact to the back layer was made on the periphery of the device, and because the majority carrier current travels a sizable distance, this is a high series resistance configuration. Second, in any array geometry where the series connection completes a circle, the whole array voltage appears across a single isolation channel. If the array voltage is 400 volts and the channel width is 20 microns, and assuming the electric field is uniform, the field is 200,000 V/cm, clearly a breakdown voltage condition. There are also difficulties in processing at the center where the sharp points of the wedge shapes are located. For all these reasons hexagon shaped junction geometry was chosen. Hexagons are ideal because they can be close packed.

Figure 1. Equivalent circuit of a series connected PV converter wired to the spark gap application.

2.0 High Voltage Capacitor Charging Applications

The fundamental problem to be addressed is shown in Figure 1. It consists of a spark gap switch, a capacitor and a photovoltaic array which is illuminated with a laser, and which will generate approximately 400 volts. From the onset of illumination the capacitor builds up voltage until the spark gap breaks down, completing the switching action. As is shown below the time taken for the capacitor to charge up to the required voltage depends on the current flow generated by the incoming photon flux.

In Figure 1 the equivalent circuit of each individual junction consists of a current generator, whose magnitude is proportional to the input photon flux, in parallel with a dark, forward biased diode and a junction capacitance. This parallel combination is in series with the internal resistance. The

load to be driven is connected across the external terminals. It is important to note that the external terminals lie outside, or to the right in the diagram, of the series resistance. If we had just one of the junctions in Fig. 1 hooked up to a load, it is easy to see that if the series resistance is zero and the load is a short, then all the light generated current, I_L , appears in the external load, but that the voltage across this load is zero. These are short circuit conditions.

Figure 2. Photovoltaic IV and power curves for a GaAs solar cell under 10 suns intensity.

Open circuit conditions obtain when the load is high resistance. Under infinite resistance the voltage at the anode of the dark diode rises to the turn on voltage and all the light generated current is injected back through the junction internally and no current appears in the load. The voltage at the load is essentially the diode turn on voltage, which, for GaAs, is about 1.1 volts. This is called the open circuit voltage of the junction.

This behavior is shown on the I-V curve of Figure 2, which shows the dark diode I-V curve translated into the fourth quadrant by an amount equal to the light generated, or short circuit, current. The short circuit and open circuit points are clearly marked. If we start at the short circuit point and continuously increase the load resistance the load current doesn't change much until we reach a voltage which approaches the equivalent circuit dark diode turn-on voltage. As the load is increased further the load current decreases steeply as more of the light generated current is injected back through the junction internally.

The dashed curve in Fig. 2 is the current-voltage product at each voltage around the I-V curve. As the current decreases and the voltage increases with increasing load resistance, there is a point at the knee of the I-V curve where the IV product is a maximum. This is

called the maximum power point and occurs at $I_{\max}$, $V_{\max}$. If we want to operate the PV converter at this maximum power point, we would load it at the optimum load, $V_{\max} / I_{\max}$. The efficiency of the converter is then the ratio of $I_{\max} V_{\max}$ to the incident optical power. Another characteristic of a PV converter is a measure of the squareness of the I-V curve, called the fill factor, and given by the ratio $I_{\max} V_{\max} / I_{sc} V_{oc}$. This parameter is sensitive to the internal series resistance. Examination of the equivalent circuit of Fig. 1 using a single junction will show why. If the series resistance is significant, then the terminal voltage is smaller than the dark diode anode voltage by the IR_s voltage drop across the series resistance. Thus the diode turns on at a lower terminal voltage and $V_{\max}$ will be smaller, as well as the fill factor. The effect is to produce a slant on the IV curve from the short circuit point to the maximum power point. There is obviously a corresponding decrease in device efficiency.

In order to provide some quantitative perspective, we will eventually want to provide enough photon flux to produce a current generator whose magnitude is on the order of one amp. Thus, we will want to produce junctions in which the series resistance is on the order of 100 milli-ohms, to produce a terminal voltage which is down only 100 mv from the open circuit voltage of 1.1 volts. Since in the series connection the terminal voltages of the individual junctions add we want to make the terminal voltage of an N junction array as close as possible to N volts. Because of the high currents required to produce acceptable charge times for the capacitor, and to maintain each junction terminal voltage to sum to the required voltage, low series resistance is the critical junction parameter which drives the design. This parameter will be analyzed in detail in another section. Another critical design feature for the system as a whole is the uniformity of the illumination. Each of the current generators in the series connected array must be identical, which means that the photon flux intercepted by each hexagon junction must be the same. This requires a uniform flux density over an area containing all the junctions. In the analysis that follows we take this as a given, but point out that actual realization of this condition may not be a trivial matter.

2.1 Capacitor Charging, Series Connection, No Series Resistance

If the load in Fig. 1 is pure capacitance, the onset of illumination will initially produce high current/low voltage conditions and as the capacitor voltage builds up these conditions will change to low current/high voltage conditions. Thus the operating point on the IV curve of Fig. 2 will start out at the short circuit point, representing a sink for the light generated current, and proceed toward the open circuit point around the IV curve. However, since it will take large times, as shown by the analysis below, to obtain the last increment of voltage between the maximum power voltage and the open circuit voltage, we will need to adjust the number of junctions in the series string so that the required voltage is obtained close to the end of the flat part of the array IV curve and before the maximum power voltage.

As we have discussed before, each junction consists of a current generator, whose magnitude is proportional to the input photon flux, in parallel with a dark diode. Also included is series resistance and parallel junction capacitance. There is also parallel resistance, but it is usually large enough to be ignored, which we will do.

For a single junction the current voltage characteristics are described, at least qualitatively, by²⁻⁴

$$I_{\text{LOAD}} = I_L - I_0[\text{Exp}(qV/nkT) - 1]. \quad (1)$$

where q is the electronic charge, V is the junction voltage, n is the diode quality factor, k is Planck's constant and T is the absolute temperature. If we solve Eq. (1) for the voltage, we get,

$$V = (nkT/q) \ln [1 + (I_L - I_{LOAD})/I_o] \quad (2)$$

The quantity I_o is dependent on the minority carrier recombination rate in the junction. It is material parameter related and we want it to be as small as possible. For good silicon junctions this quantity, expressed as a current density, is on the order of 10^{-13} A/cm². For GaAs junctions this recombination current density can be 10^{-15} to 10^{-16} A/cm². For the small junctions of these series connected layouts the area is on the order of 10^{-4} cm², so I_o would be 10^{-19} to 10^{-20} A. As a worst case the calculations below are based on 5×10^{-18} A.

In the series connected capacitor charging application of Fig. 1, the load current is the same in each converter in the string and equal to the capacitor current, I_c . In light of Eq. (1) we can write,

$$I_c = I_{L1} - I_{o1} [\text{Exp}(qV_1/n_1kT) - 1] = \dots\dots\dots = I_{LN} - I_{oN} [\text{Exp}(qV_N/n_NkT) - 1] , \quad (3)$$

and the full capacitor voltage is the sum of the individual junction voltages,

$$V = V_1 + V_2 + \dots\dots\dots + V_N , \quad (4)$$

and where N is the number of junctions in the series connection. Using Eq. (2) with I_{LOAD} equal to I_c , we can write the individual junction voltages as,

$$\begin{aligned} V_1 &= (n_1kT/q) \ln [1 + (I_{L1} - I_c)/I_{o1}] \\ V_2 &= (n_2kT/q) \ln [1 + (I_{L2} - I_c)/I_{o2}] \\ V_N &= (n_NkT/q) \ln [1 + (I_{LN} - I_c)/I_{oN}] . \end{aligned}$$

For identical junctions,

$$n = n_1 = n_2 = \dots\dots\dots = n_N \quad (5)$$

$$I_o = I_{o1} = I_{o2} = \dots\dots\dots = I_{oN} \quad (6)$$

$$I_L = I_{L1} = I_{L2} = \dots\dots\dots = I_{LN} . \quad (7)$$

Equation (5) and Eq. (6) require identical diode junctions, and Eq. (7) requires uniform optical illumination, and is important. Under conditions (5) through (7), Eq. (4) for the capacitor voltage can be written,

$$V = (NnkT/q) \ln [1 + (I_L - I_c)/I_o] . \quad (8)$$

If we now invert Eq. (8) back for the capacitor current we get,

$$I_c = I_L - I_o[\text{Exp}(qV/NnkT) - 1] . \quad (9)$$

The quantity V/N in the exponential is just a single junction voltage, $V_1, V_2, \dots, V_N$, and I_L is the magnitude of a single current generator, $I_{L1}, I_{L2}, \dots, I_{LN}$. With no series resistance, as is the present case, the light generated current is just the array short circuit current, I_{sc} . Thus, when the array output voltage is zero, none of the dark diodes is turned on and there is no current loss internally. Equation (9) tells us that the capacitor voltage builds up in the same way as the voltage output of a single junction. The open circuit voltage of a single GaAs PV junction is about 1.1 volts. Equation (9) tells us that, from the onset of

illumination, a single junction output voltage of, say 0.5 volt, will be reached at the same time that the capacitor voltage reaches $0.5N$.

If we use $I_c = dQ/dt$ and $V=Q/C$, where C is the capacitance value, in Eq. (9) we get a differential equation which is directly integrable in closed form,

$$dQ/dt = I_L - I_o [\text{Exp}(qQ/NnkTC) - 1] \quad (10)$$

If we make the simple substitutions $\alpha = q/NnkTC$ and $u = \text{Exp}(\alpha Q)$ we get down to an equation that looks like,

$$(1/\alpha u) du/dt = I_{sc} - I_o (u - 1) , \quad (11)$$

where I_{sc} has been used for I_L . Separating variables we get,

$$du/[u(I_{sc} - I_o (u - 1))] = \alpha dt . \quad (12)$$

The left side of Eq.(12) can be integrated by partial fractions and the right side is just αt . After determining the proper limits of integration on the variable u , this integration is straightforward and the result is an expression for the time it takes to charge the capacitor to any arbitrary voltage, limited by the open circuit voltage, as will be evident below. This expression is given by,

$$t = (C/I_{sc}) [V + (NnkT/q) \ln \frac{I_{sc}}{I_{sc} - I_o [\text{Exp}(qV/NnkT) - 1]}] . \quad (13)$$

The exponential term in the denominator is just the expression for the dark current in parallel with the current generators, so Eq. (13) can be written as,

$$t = (C/I_{sc}) [V + (NnkT/q) \ln \frac{I_{sc}}{I_{sc} - I_{dark}}] , \quad (14)$$

where it must be kept in mind that the voltage dependence of the second term is in I_{dark} .

Equation (14) consists of a term linear in the voltage and one that is logarithmic. The log term does not contribute much to the charge time until the voltage gets high enough to start increasing the dark current, which is small on the flat part of the I/V curve. So a graph of the charge time as a function of voltage should consist of a linear region corresponding to the flat part of the $I-V$ curve followed by a sharp increase as the denominator of the $\ln$ term approaches zero. As the voltage approaches the open circuit voltage, where, by definition, $I_{sc} = I_{dark}$, the denominator of the $\ln$ argument approaches zero and the logarithm diverges to a very large number adding large amounts of time. Thus the open circuit voltage of the array is never attained, but only approached asymptotically. As a practical matter we would want our application voltage to be reached at the end of the flat part of the I/V curve and we would include enough junctions in the series string to do so.

Figure 3. Charge time for a 1 nF capacitor using a 241 junction, series connected PV converter with 1 kW optical input at 830 nm.

Several calculations of t vs V have been made using series connected strings of 241 junctions and 417 junctions. The voltage is incremented from 0 to 1.1 volts and each voltage is multiplied by the number of junctions for use in Eq. (13). The calculations have been made for values of short circuit current from 1 mA to 1 A. These would roughly correspond to optical input power levels of 1 W to 1 kW, at a wavelength of 830 nm from a laser. The details of the device designs required to obtain these short circuit currents are

Figure 4. Semi-log plot of charge time for a 1 nF capacitor using a 241 junction series connected PV array with optical input from 1.4 W to 1.4 kW at 830 nm. This input power range produces a range of short circuit current from 1 mA to 1 A.

discussed in a section below. Fig. 3 shows a t vs V curve for an optical power of 1 kW incident on a 241 junction series connection. The graph has the expected behavior. There is a linear region followed by a sharp upturn as the dark current approaches the short circuit current. Note that the voltage reaches the 200 volt level at times on the order of 0.2 microsecond before the curve turns up. Figure 4 is a log plot of charge time for the same array as a function of capacitor voltage for six short circuit current levels corresponding to optical input power values from 1.4 W to 1.4 kW. Note that the 200 volt level is reached in times ranging from 100 microseconds to about 0.1 microsecond at the highest input optical power.

Figure 5. Charge time for a 1 nF capacitor using a 417 junction, series connected PV array with 1 kW optical input at 830 nm.

The results of the calculations for the 417 junction series connection are shown in Fig. 5 and Fig. 6. For the linear plot of Fig. 5, under 1 kW of input optical power, generating 540 mA short circuit current, a capacitor voltage of 400 volts is reached in a little less than 1 microsecond. For the log plot of Fig. 6 capacitor charge times from several hundred microseconds to a few tenths of a microsecond are obtained for input power levels from 2.6 W to 2.6 kW, generating short circuit levels from 1 mA to 1 A.

Figure 6. Semi-log plot of charge time for a 1 nF capacitor using a 417 junction, series connected PV array with optical input ranging from 2.6 W to 2.6 kW at 830 nm. The corresponding short circuit current range is 1 mA to 1 A.

The above analysis is restricted to the zero series resistance case. To take series resistance into account the voltage in Eq. (1) has to be replaced by $V + IR_s$. This places a dQ/dt in the exponential and solution of the differential equation becomes much more difficult. While we don't know the solution we can certainly assume that the charge times will be stretched out somewhat. In this case the flat part of the I-V curves may have at least some slope to them, which will probably cause the first term in Eq. (14) to be something other than linear. However, qualitatively, the charge times should behave in the manner contained in Eq. (14), which tells us that, to first order, the charge times are the product of the capacitance and voltage divided by the short circuit current.

3.0 Photovoltaic Array Designs.

In this section two types of series connected photovoltaic arrays are described. They differ in the number of junctions in the series connection. One has 241 junctions and the other has 417 junctions. The 417 junction converter is intended for direct application in Figure 1. The 241 junction converters are intended to be used in tandem, each with its own illumination and wired in series. However, there are inherent difficulties involving timing of the laser pulses which makes this approach less desirable than using a single series connected converter.

3.1 Individual Junction Designs

Figure 7 shows the semiconductor layers which are grown on a semi-insulating GaAs wafer and Fig. 8 shows three hexagon junction geometry designs. The first layer grown is the n type GaAs buffer layer which is made thick and doped as heavily as possible with Te as the donor.

Metal Grid		
AlGaAs p Type Cap (15% Al)	$1 \times 10^{19} \text{ C}$	5 μm
AlGaAs p Type Window (70% Al)		0.1 μm
GaAs p Type Emitter	$2 \times 10^{18} \text{ C}$	0.5 μm
<hr/>		
GaAs n Type Base	$1 \times 10^{17} \text{ Si}$	5 μm
GaAs: n Type Buffer	$1 \times 10^{19} \text{ Te}$	10 μm
GaAs Semi-Insulating Substrate		350 μm

Figure 7. Semiconductor layer structure for series connected PV converters.

As of this writing J. Klem of the CSRL is doing the research on Te doping and developing the processing required to incorporate this donor in GaAs grown by Molecular Beam Epitaxy (MBE). This layer carries the majority carrier current which will flow laterally to the next junction in the string. The next layer up is the n type GaAs active region, which is called the base. It is grown 5 μm thick to provide maximum attenuation of the beam. The next layer is the heavily doped p type GaAs emitter layer. The light generated minority carrier holes in the base are collected into the p type emitter where they become majority carrier current. In the specific design here this current travels vertically into the AlGaAs cap layer. The next layer is the thin, wide bandgap, AlGaAs window layer which is incorporated to passivate the surface of the GaAs emitter layer. Historically, it has been found that without this layer the rate of carrier recombination at the emitter surface is unacceptably high, resulting in low open circuit voltage. The next layer is the p type AlGaAs cap layer. In this layer the majority carrier current travels laterally. This layer is the lowest conductivity of all the layers and a metal grid is usually incorporated to provide a short current path to metal so the carriers do not have to travel all the way to the periphery of the device through the higher resistivity semiconductor material.

The semiconductor processing required to fabricate these junctions is not conventional because of the deep etches caused by the need for thick material layers to realize low series resistance. The process development required to fabricate these converters is under investigation at this writing by Stanley Kravitz and Walter Zuberzycki in the CSRL. However, the process steps will be roughly as follows. The first step will be ohmic contact metal deposition onto the AlGaAs cap layer. Then the active layer mesa etch removes material down to the upper surface of the n type buffer layer. This etch is through the cap, window, emitter, and base layers, and is about 10 μm deep. The next step is ohmic metal deposition onto the n type buffer layer surface. This is followed by another 10 μm deep etch through the buffer layer to the semi-insulating substrate. This etch step electrically isolates the junctions. Then the whole wafer will be planarized with polyimide and vias will be opened up everywhere there is ohmic metal. The final step is either electroplating or electroless plating of the metal to a thickness of 10 μm . This step includes the gridlines, bus bars, interconnect metal and the bond pads. It is important to realize that the interconnect metal and bond pads rest on the polyimide, as is required to prevent shorting of the junctions.

Figure 8 shows the three individual junctions which are incorporated into the series connected arrays. Figure 8 (a) shows a hexagon junction with an optically active mesa that is 200 μm vertex to vertex. Because these devices are to carry currents approaching one ampere the metal grid that is used on the top mesa surface covers a relatively high percentage of the optically active area. This metal grid consists of 5 μm current collecting lines connected to a 12 μm bus bar, both of which will be electroplated up to a thickness of 10 μm . The photon loss for this device is 44.2%. Although this appears high relative to terrestrial photovoltaic converters, this high percentage is driven by series resistance considerations, as will be discussed below. The approach used here is to design a converter which will carry the current required for acceptable charge times without detrimental internal voltage drops which would cause the array output voltage to be too low for the application at hand. The short circuit current, linear in laser input power, can be increased by raising that laser power.

8 (a)

8 (b)

8 (c)

Figure 8 (a) Hexagon shaped PV junction. The optically active mesa is 200 microns vertex to vertex. (b) Hexagon shaped PV junction with optically active mesa of 300 microns vertex to vertex. (c) 300 micron mesa with narrower bus bar metal around the periphery of the mesas.

A somewhat smaller photon loss fraction is obtained with the 300 μm hexagon junction shown in Fig. 8 (b). Here we have more 5 μm lines with the same size bus bars at the periphery of the mesa. The photon loss percentage for this device is about 38%. As a test of the effect of bus bar width on the series resistance of the device, an array has been laid out using the 300 μm mesa with bus bars that are 6 μm wide instead of 12 μm . This device is shown in Fig. 8 (c). The photon loss fraction for this device is about 30%.

3.2 Series Connected Array Designs

241 Junction Series Connection

Figure 9 contains two array designs, each with 241 series connected junctions which are 200 μm vertex to vertex as shown in Fig. 8 (a). Both of the chips in Fig. 9 are 4.2 mm x 4.2 mm and are intended to be illuminated by a uniform laser beam of diameter 4 mm. The only difference between Fig. 9 (a) and Fig. 9 (b) is the column to column interconnect metal. In Fig. 9 (a) the interconnect metal from the top mesa of one junction to the bottom mesa of the junction in the next column is made with a strap of metal (gold) formed as a right angle. It is well to keep in mind that this interconnect metal, as well as the bond pads are part of the electroplating mask level, and that they sit on top of the polyimide layer. For this design the current flow into the top layer is symmetrical, the holes recombining with the electrons, whose flow is assumed to split equally around each side of the periphery of the top mesa. The majority carrier (electron) current flows out of the n type base at the back in order to maintain charge neutrality at the loss of the positive hole collected into the emitter. Thus the majority carrier current flows primarily laterally in the back heavily doped buffer layer. This current flow would be symmetric except for the fact that we have to break the contact to the lower mesa so as not to short the junction to the interconnect metal. The interconnect metal in this design may represent too much resistance. For example, the longest of the right angle metal interconnects is about 850 μm long, 100 μm wide, and plated to 10 μm thick. Using $2.44 \times 10^{-6} \Omega \text{ cm}$ for the bulk resistivity of gold, the resistance of this interconnect works out to about 20 m Ω .

Figure 9 (b) is an array in which all column to column right angle interconnect metal has been eliminated. Since the individual junctions have hexagonal symmetry they can be rotated through multiples of 30 degrees until the interconnect strap points directly across the junction isolation gap. This would be a strap of gold 100 μm wide by 50 μm long and 10 μm high, resulting in a series resistance of about 1 m Ω per junction. The principal difficulty with this arrangement, if it turns out to be such, is that the symmetry of the current flow through the devices at the column to column interconnect may add series resistance. While it is doubtful that this added series resistance will be as much as is eliminated in using this design, the result will have to await experiments.

9 (a)

9 (b)

Figure 9 (a) Series connected array of 241 junctions using the 200 micron junction. (b) Same array with the short interconnect metal over the isolation channel.

Figure 10 contains three of the 241 junction series connected arrays using the 300 μm hexagons. All are 5.8 mm x 5.8 mm chips and (a) and (b) are designed for a 5.6 mm diameter beam. Chip (c), containing narrower metal lines and bus bars is designed for a 5.3 mm beam. Figure 10 (a) is the design with the interconnect metal as straps which connect one column to the next around right angles. The interconnects are 100 μm wide

10 (a)

10 (b)

10 (c)

Figure 10 (a) Series connected array of 241 junctions using the 300 micron junction. (b) Same array with the short interconnect metal across the isolation channels. (c) Same array as in (a) with narrow bus bar metal.

and 10 μm high, as in the case of the 241 junction design with the 200 μm junction. Figure 10 (b) is the design which eliminates the right angle interconnect metal from one column to the next and replaces it with a short hop over the isolation channels. Figure 10 (c) is the same 241 junction design using the 300 μm hexagon with the 6 μm bus bars

instead of the wider ones. If the performance of arrays (a) and (c) are comparable at the currents required for the application, then we know that (a) contains too much metal coverage.

11 (a)

11 (b)

Figure 11 (a) Series connected array of 417 junctions using the 200 micron junction. (b) Same array using the short interconnect metal.

417 Junction Series Connection

Figure 11 contains series connections of 417 junctions using the 200 μm junction design. Both chips are 5.4 mm x 5.4 mm and are designed for a 5.2 mm diameter beam. Figure 11 (a) is the array with the column to column interconnect metal in the form of a 100 μm right

angle strap. Figure 11 (b) is the array with the shorter interconnect metal at a 30 degree angle across the isolation gap. Figure 12 contains the 417 junction series connection using the 300 μm junction design. These are somewhat larger chips, measuring 7.4 mm x 7.4 mm and are intended for a 7.2 mm diameter beam. Figure 12 (a) is the right angle metal interconnect strap layout and Fig. 12 (b) is the short interconnect metal design.

12 (a)

12 (b)

Figure 12 (a) Series connected array of 417 junctions using the 300 micron junction with the long column interconnect metal. (b) Same array with the short interconnect metal.

4.0 Short Circuit Current Calculations

In this section estimated short circuit current calculations for each array design are presented. These calculations will be carried out with the assumption of one watt of incident optical power at a wavelength of 830 nm, and is assumed to be uniformly spread over a circle whose diameter for each array is different. This circle of uniform optical power will be no larger than necessary to cover all the hexagons in the series connected string. Since we know the beam area, assumed input optical power, individual junction area, metal area, and the number of junctions in a particular array we can calculate the number of photons falling on the active area of each junction per unit time. Then we use the fact that we get one carrier per absorbed photon to calculate the current from the photon flux.

By a wide margin, the single largest effect in determining the short circuit current of an n-junction series connected array is the partitioning of the input beam into n individual pieces, which can be thought of as current generators. For example, if we have one watt of optical power incident on a single GaAs photovoltaic junction which is one square centimeter in area, the short circuit current is calculated as follows: The energy carried by an 830 nm photon is given by,

$$E_{ph} = hc/\lambda = 1.2398/\lambda \text{ (in microns)} = 1.49 \text{ eV.} \quad (15)$$

In Eq. (15) h is Planck's Constant, c is the speed of light in vacuum, and λ is the wavelength. Since one watt is one joule/sec, we need the photon energy in joules. Then, since there are 1.6×10^{-19} joule/eV, the photon energy is,

$$E_{ph} = 2.38 \times 10^{-19} \text{ joule.} \quad (16)$$

Then the photon flux in 1 joule/sec (one watt) is given by,

$$\Phi = (1 \text{ joule/sec}) / (2.38 \times 10^{-19} \text{ joule/photon}) = 4.2 \times 10^{18} \text{ photons/sec.} \quad (17)$$

If we now assume 100% internal quantum efficiency and no reflection losses, the current collected will be,

$$I_{sc} = q\Phi = 672 \text{ mA.} \quad (18)$$

This is the current generator, in reference to Fig. 1 when only one junction is present. If we now imagine that we can somehow partition the one square centimeter area into n equal parts and electrically connect them in series with no losses, the photon flux in Eq. (17) is now divided into n parts, each illuminating one of the n junctions. Since the n junctions are series connected the current is the same as in one junction. Thus the short circuit current is reduced to I_{sc}/n , where I_{sc} is the single, large junction short circuit current. But since the voltage is n times the single, large junction voltage the IV product remains the same. This effect is shown in Figure 13, which includes a line for 90% quantum efficiency and the dashed line is drawn through points calculated from different size junctions. The optical input is one watt at 830 nm. Predictably the points depart from the

Figure 13. Short circuit current as a function of the number of series connected junctions.

no loss curve by increasing amounts as the number of junctions increases. This is due to an increasing fraction of the beam falling on a higher percentage of dead space between the junctions. The 672 mA current from Eq. (18) for a single junction is reduced to 0.672 mA by partitioning the beam into 1000 pieces by the 1000 junctions. It is primarily this decrease in current which must be replaced by increasing the input optical power, with a smaller amount due to photon losses due to blockage by metal and absorption in dead spaces between the junctions.

4.1 Short Circuit Current - 241 Junction, 200 μm Hexagon Array

This array is made up of the 200 μm hexagon junction as shown in Fig. 8 (a). The array itself is shown in Fig. 9 (a). It is designed for a 4 mm diameter beam, resulting in an area of 0.126 cm^2 . The area of a hexagon which is 200 μm vertex to vertex is $2.6 \times 10^{-4} \text{ cm}^2$. The grid lines are deposited 7 μm wide and 158.4 μm long. The cut through the polyimide is made 1 μm in from the edge of the ohmic metal deposition, which will result in a 5 μm plated grid line. So for purposes of calculating the photon blockage we will have to use the full 7 μm width. The sum of the areas of all three of these grid lines is $3.29 \times 10^{-5} \text{ cm}^2$. The bus bars consist of rectangles which are 79.22 $\mu\text{m} \times 15 \mu\text{m}$, plus two right triangles which are 15 $\mu\text{m} \times 8.66 \mu\text{m}$. Thus one bus bar area is $1.32 \times 10^{-5} \text{ cm}^2$, and since there are six of these bus bars, the area is $7.91 \times 10^{-5} \text{ cm}^2$. There is an additional small rectangle 3 $\mu\text{m} \times 96.54 \mu\text{m}$ which shadows part of the junction mesa under the interconnect metal. The area of this rectangle is $2.90 \times 10^{-6} \text{ cm}^2$. The total metal area on this mesa is $1.15 \times 10^{-4} \text{ cm}^2$. Then the ratio of metal area to the mesa area gives the fraction of the incident photon flux which is blocked from the device active area, or 44.2%. So the fraction of active area for this mesa is 55.8%, or $1.45 \times 10^{-4} \text{ cm}^2$. Now the photon flux incident on a single junction is obtained by multiplying this active area by the photon flux density in the incoming beam. So the flux density is $4.2 \times 10^{18} / 0.126 = 3.33 \times 10^{19}$ photons/sec/cm². With the $1.45 \times 10^{-4} \text{ cm}^2$ active area the photon flux available for generating current is 4.6×10^{15} photons/sec. If we use $\eta q \Phi$ for the short circuit current, as in Eq. (18), where we have added the quantum efficiency, η , of 0.9, we get 0.696 mA for an incident intensity of one watt. If we now increase the input intensity by a factor of 1000, to an input power of 1 kW, and keeping in mind that we use a pulsed laser with pulses only a few microseconds long to eliminate thermal effects, then the current, linear in the input photon flux, will be 0.696 A. If we now calculate the charge time using the first term of Eq. (14), CV/I_{sc} , we find that this current will charge the 1 nF capacitor to 200 volts in 0.29 μSec .

4.2 Short Circuit Current - 241 Junction, 300 μm Hexagon Array

There are two types of 300 μm hexagon arrays. One has 12 μm bus bars around the periphery of the mesa and the other has 6 μm bus bars. Since the percentage photon blockage is significantly different for the two cases we calculate the estimated short circuit current for both.

Wide Bus Bars

These arrays are shown in Fig. 10 (a) and (b), where the only difference is in the interconnect metal. The percentage shadowing for both is the same because they both have the same metal grid. Using the same approach as above, we find the total metal area on the mesa is $2.21 \times 10^{-4} \text{ cm}^2$, and with a mesa area of $5.85 \times 10^{-4} \text{ cm}^2$, the fraction of the incident photon flux that is blocked from the active area is 37.8%. Then the active area is 62.2%, or $3.64 \times 10^{-4} \text{ cm}^2$. This chip is 5.8 mm $\times$ 5.8 mm and is designed for a 5.6 mm diameter input beam. This makes the beam area 0.246 cm^2 , and the photon flux density in one watt of optical power is 1.71×10^{19} photons/sec/cm². Then multiplying this by the active area of the mesa gives the photon flux available for generating current, or 6.21×10^{15} photons/sec. Then, as before, using 90% for η , and $\eta q \Phi$ for the short circuit, we get

0.895 mA. Again using CV/I_{sc} , with $C = 1$ nF and $V = 200$ volts, we get 0.22 μ Sec for the charge time.

Narrow Bus Bars

With the narrow bus bars the total metal area of this grid is 1.73×10^{-4} cm² and when divided by the mesa area of 5.85×10^{-4} cm² gives the photon blocking fraction of 29.6%. Then the active area is 4.12×10^{-4} cm². The smaller bus bar width on the lower mesa n contact allows a smaller back mesa and thus a more compact array. This array can be fully illuminated by a 5.3 mm diameter beam. Thus the beam area is 0.22 cm² and the photon flux density in one watt of optical power spread over this area is 1.90×10^{19} photons/sec/cm². Then multiplying this by the active area of the junction gives the photon flux available for generating current, or 7.84×10^{15} photons/sec. Then using $\eta = 0.9$, and $\eta q \Phi$ for the short circuit current we get 1.13 mA. Once again for $C = 1$ nF, and $V = 200$ volts the charge time comes out 0.18 μ Sec.

4.3 Short Circuit Current - 417 Junction, 200 μ m Hexagon Array

We have used the 200 μ m and 300 μ m hexagon junctions in a series connection of 417 junctions so that one chip might be used in the spark gap application. A number of questions need to be answered before it is decided whether to use two 241 junction arrays in series to provide the 400 volts required for the spark gap application, or to use a single 417 junction array. Among these are the following: Since the 417 junction array is a larger chip and requires a larger beam area, can the input photon flux be obtained to generate enough current so that the capacitor charge time is not too long? If two 241 junction chips are used, can the two laser beams illuminating them be synchronized sufficiently to obtain the necessary capacitor charge and voltage? As discussed below, series resistance is the most important parameter that will determine the success of either approach. So the most fundamental question is whether or not we can fabricate either array with sufficiently small series resistance per junction that the required voltage will be obtained. The working rule here is that if a single GaAs junction voltage is 1.1 volts and we have 100 m Ω series resistance, then at a current of one ampere the terminal voltage for a given junction is down from the junction voltage by 0.1 volt. In the next section we will make estimates of the array series resistance for the devices that have been designed and we intend to fabricate. However, in this section we continue our estimates of short circuit current.

The 200 μ m junction for this array is the same as that used in the 241 junction arrays. So the photon blocking fraction is the same, at 44.2%, and the junction active area is the same at 1.45×10^{-4} cm². However, the photon flux density is smaller for the larger array. The incident beam for this array is 5.2 mm in diameter, so the beam area is 0.212 cm². So the one watt (4.2×10^{18} photons/sec) photon flux density is 1.98×10^{19} photons/sec/cm². Then the product of this and the junction active area gives the photon flux available for generating current, or 2.87×10^{15} photons/sec. Again using $\eta = 0.9$ and $\eta q \Phi$ for the short circuit current we get 413 μ A. As before, if we increase the input optical power by a factor of 1000, and assuming the current increases linearly, the 413 mA would charge the 1 nF capacitor to 400 volts in 0.97 μ Sec.

4.4 Short Circuit Current - 417 Junction, 300 μm Hexagon Array

In the 417 junction, 300 μm array we use only the wide bus bar junction design on the ground that the narrow bus bar design will probably have too much series resistance to be useful. From section 4.2, the photon blocking percentage is the same at 37.8% and the active area of the junction mesa is $3.64 \times 10^{-4} \text{ cm}^2$. This chip is designed to be 7.4 mm x 7.4 mm and the beam diameter is 7.2 mm. This gives a beam area of 0.407 cm^2 and thus, a one watt (4.2×10^{18} photons/sec) photon flux density of 1.03×10^{19} photons/sec/ cm^2 . Then multiplying by the junction area gives 3.75×10^{15} photons/sec available for current generation. Using the same quantum efficiency of 90% the short circuit current is found to be 541 μA . Then repeating the calculation with 1 kW input power, and 541 mA short circuit current, 400 volts is reached at 0.74 μSec .

Table 1 summarizes the short circuit current and charge time calculations for the 1 nF capacitor. The short circuit currents result from input optical power of 1 kW.

Table 1

Array	Chip Size (mm)	Beam Dia. (mm)	Beam Area (cm^2)	Photon Flux Density (photons/sec/ cm^2)	Mesa Active Area (cm^2)	Short Circuit Current (mA)	Charge Time (μS)
241-200	4.2	4.0	0.126	3.34×10^{19}	1.45×10^{-4}	696	0.29
241-300	5.8	5.6	0.246	1.71×10^{19}	3.64×10^{-4}	895	0.22
241-300n	5.8	5.3	0.221	1.90×10^{19}	4.12×10^{-4}	1130	0.18
417-200	5.4	5.2	0.212	1.98×10^{19}	1.45×10^{-4}	413	0.97
417-300	7.4	7.2	0.407	1.03×10^{19}	3.64×10^{-4}	541	0.74

5.0 Junction Series Resistance

In Figure 1 it can easily be seen that the series resistance is the most important parameter determining the array voltage and current. For example, if the current generators are such that we have current on the order of 1 amp in the circuit and each junction has 1 ohm resistance then the voltage drop across this series resistance is 1 volt per junction. Since the voltage on the knee of the GaAs junction I-V curve is about 1.1 volts, it is clear that under these circumstances almost all the junction voltage would be dropped across the series resistance. On the other hand if the series resistance is 100 milli-ohms, the same one amp current would cause this voltage drop to be 0.1 volt, a voltage drop which could probably be tolerated. In the 241 junction array this would be a voltage loss of 24 volts and for the 417 junction array the voltage drop would be roughly 42 volts. So the target series resistance for each of the hexagon junctions will be 100 m Ω .

Using the semiconductor layer diagram in Fig. 7, estimates of the components of the series resistance can be made. There are three types of resistance in this structure, bulk resistance which arises from carrier transport in the volume of each layer, contact resistance arising

out of metal-semiconductor contacts to the top AlGaAs p type cap layer and contacts made to the thick n type buffer layer, and bulk resistance in the metal lines. In the cap layer and the buffer layer the current is majority carrier transport and is lateral current flow. In the emitter region the current is majority carrier flow and in the n type base the current is minority carrier flow (holes). In both the current flows vertically through a large cross sectional area.

5.1 Bulk Semiconductor Resistance

If the base layer is doped to $5 \times 10^{17} \text{ cm}^{-3}$, the resistivity of the material will be $4 \times 10^{-3} \Omega\text{-cm}$. Then using the standard resistance formula, $R = \rho L/A$, where ρ is the material resistivity, L , the current path length, and A , the cross-sectional area, the resistance of the base layer for the $200 \mu\text{m}$ junction is $8 \text{ m}\Omega$. For the $300 \mu\text{m}$ junction it is $3 \text{ m}\Omega$. For the emitter layer at a doping density of $2 \times 10^{18} \text{ cm}^{-3}$, the resistivity will be about $.02 \Omega\text{ cm}$. With this resistivity, and a path length of $0.5 \mu\text{m}$, the resistance for the $200 \mu\text{m}$ junction is $4 \text{ m}\Omega$, and for the $300 \mu\text{m}$ junction it is $2 \text{ m}\Omega$. The current flow in the p type AlGaAs window is vertical also but the path length is so short that it will not contribute much resistance. For example at $2 \times 10^{18} \text{ cm}^{-3}$ the resistivity of GaAs is about $.02 \Omega\text{ cm}$, but let's use a number five times as high, or $0.1 \Omega\text{ cm}$ because it is AlGaAs. With this higher resistivity and a path length of $0.1 \mu\text{m}$, the resistance of this layer in the $200 \mu\text{m}$ junction is $4 \text{ m}\Omega$, and for the $300 \mu\text{m}$ junction it is $2 \text{ m}\Omega$.

The majority carrier current flow in a PV converter circuit is controlled by collecting minority carriers generated in the base layer. When electron/hole pairs are generated optically in the n type GaAs base layer, carrier concentration gradients are set up which cause both electrons and holes to diffuse in the direction of the p-n junction. The requirement for local charge neutrality means that the concentration gradient for both carriers is the same. However, at the junction only the minority carrier hole is collected into the p type emitter as a majority carrier. The majority carrier (electron) concentration in the base layer is in electrical contact with the back contact. The loss of the hole in the base means the base is one positive charge short of charge neutrality and thus for every hole collected an electron is ejected into the back contact to restore it. The electrons injected into the back contact and the holes collected in the p type emitter differ in energy by an amount related to the built in voltage at the junction. Thus the electrons do work in the external circuit before recombining with the collected holes at the emitter layer contact.

In the top cap layer and the buffer layer the majority carrier current flows laterally. In order to estimate the resistance of these layers we will use the results of Wyeth⁵. In this paper Wyeth showed that the process of collecting current vertically out of a cross-sectional area and then conducting it radially in a relatively thin layer can be described as a continuous distribution of current generators at the interface between the thick and thin layers. If the layers are circular the resistance is found to be independent of radius and depends only on the sheet resistivity of the thin layer. Specifically, $R = (1/8\pi)\rho/t$, where ρ is the material resistivity and t is the layer thickness. Thus, the approach to minimizing this resistance is to dope the layer as heavy as possible, and if this resistance is still too high, then the thickness is increased.

Referring to Fig. 8, the buffer layer contact is the outside bus bar and is placed on five of the six sides of the hexagon mesa. The top of this mesa stands $10 \mu\text{m}$ above the semi-insulating material. This layer will be grown by John Klem of the Compound Semiconductor Research Laboratory (CSRL) using MBE. The remaining layers will be grown by Hong Hou in the CSRL using Metal Organic Chemical Vapor Deposition (MOCVD). To get some estimate of the resistance let us assume a circular mesa and ignore

that fact the current collection will be somewhat crowded to the open end. This mesa layer is to be grown heavily doped with Te to a doping density of $1 \times 10^{19} \text{ cm}^{-3}$ and will produce a carrier mobility of $1350 \text{ cm}^2/\text{V-sec}$.⁶ To get the resistivity to use in Wyeth's formula, we use the fact that $\rho = 1/ne\mu$, where n is the carrier concentration, e is the electronic charge, and μ is the carrier mobility. The result is $\rho = 4.6 \times 10^{-4} \Omega \text{ cm}$, and using this in Wyeth's formula with $t = 10 \mu\text{m}$, we get, $R = 18 \text{ m}\Omega$.

For a carbon doped top layer doped at $1 \times 10^{20} \text{ cm}^{-3}$ the mobility is $30 \text{ cm}^2/\text{V-sec}$,⁷ so the resistivity works out to $2.1 \times 10^{-3} \Omega \text{ cm}$, and for a $5 \mu\text{m}$ thickness Wyeth's formula gives $166 \text{ m}\Omega$. This resistance is clearly unacceptable, but this number was calculated assuming no metal grid, just the bus bars around the periphery of the junction mesa and radial current flow. This number can be lowered significantly by use of metal grid lines so the current does not have to flow all the way to the periphery of the mesa to be collected. Figure 8 (b) and (c) show 12 grid lines covering the top surface of the $300 \mu\text{m}$ mesa. How much this will lower the resistance contained in the top layer is difficult to calculate. If we have 12 equivalent current paths one could hope that these parallel paths would reduce this resistance by a factor of $1/12$. If this is the case then the resistance in this layer is down to about $14 \text{ m}\Omega$.

Table 2 is a summary of estimated resistance due to carrier flow in the bulk material of the various layers.

5.2 Contact Resistance

We will calculate metal contact resistance by dividing a specific contact resistivity of $5 \times 10^{-6} \Omega \text{ cm}^2$ by the contact area. The resistance associated with collecting current from a semiconductor layer into a metal line is not always an area effect. When the semiconductor layer is thin the current is not collected uniformly into the metal along the contact length, L . Referring to Fig. 14 with the direction of current shown, there are conditions which cause the current collected into the metal line to be larger on the left side than the right. This is the ideal case and is similar to collecting current from the emitter layer into the grid lines and busbars and from the buffer layer into the n bus bars. Using the results of Berger⁸, as published by Schroder⁹, we can determine to some degree whether or not our PV converter case is an area effect or not.

For the three terminal contact resistance measurement, as shown in Fig. 14, the contact resistance, as given by Berger⁸, is,

$$R_c = ((\rho_s \rho_c)^{1/2} / Z) \text{Coth} (L/L_T) = (\rho_c / (L_T Z)) \text{Coth} (L/L_T) , \quad (19)$$

where ρ_s is the sheet resistivity of the semiconductor layer, ρ_c is the specific contact resistivity, Z is the contact width, L is the contact length, and L_T is called the transfer length, given by $(\rho_c / \rho_s)^{1/2}$. Two cases lead to simplification, first for L less than or equal to $0.5L_T$, the contact resistance is given by

$$R_c = \rho_c / LZ = \rho_c / A_c , \quad (20)$$

where A_c is the contact area. This is the case we are using to estimate the contact resistance for the PV converters. The second case is for L greater than or equal to $1.5L_T$, in which the contact resistance is given by,

$$R_c = \rho_c / L_T Z. \quad (21)$$

So to determine which case applies we calculate the transfer length and compare its value with the contact length. We need to keep in mind here the contact length is the line widths on our PV converters and not the line lengths. In our analysis ρ_c is taken to be $5 \times 10^{-6} \Omega \text{ cm}^2$, and since we have values for doping densities and layer thicknesses we can calculate the sheet resistivity values. The two layers in which current is collected into metal are the buffer layer at the back of each junction and the top cap layer, and these layers are identical for all junctions and arrays.

From Table 2 the buffer sheet resistivity can be calculated as the ratio of the bulk material resistivity to the thickness, and when divided into the specific contact resistivity, ρ_c , we get $33 \mu\text{m}$ for the transfer length. For the top, or cap layer the transfer length works out to be $11 \mu\text{m}$. If we now look at Table 5, it can be seen that the n bus bar width is on the order of, or less than half the transfer length for all devices except the 2 mm test device. So for the n contacts we are justified in using the contact area in calculating the contact resistance. For the metal grid lines on the p-type material the transfer length is $11 \mu\text{m}$ and the $7 \mu\text{m}$ grid line width is only a small amount greater than half the transfer length. However, if one uses Eq. (19) rather than the approximation the equivalent contact

Figure 14. Ideal three terminal contact resistance measurement.

resistance works out to be $51 \text{ m}\Omega$ instead of $25 \text{ m}\Omega$ for 12 radial grid lines on the $300 \mu\text{m}$ mesa calculated on the basis of contact area. The difficulty with the estimated resistance values for the p-type cap layer is both the bulk resistivity and the thickness of $5 \mu\text{m}$, which makes the sheet resistivity of the layer high. This, in turn, makes the transfer length for the layer small. However, even if we could double the thickness, it would only add a factor of 1.4 to the transfer length, resulting in $15.4 \mu\text{m}$ instead of $11 \mu\text{m}$. If this were the case the approximation would apply with a $7 \mu\text{m}$ line width. We have the same difficulty with the p busbars, where the contact length is greater than half the transfer length by a factor of between two and three. If these estimates are correct, and there is a second generation of devices fabricated, it will be the resistance in the contacts to the p-type layers that will have to be addressed.

200 μm Mesa

The grid lines on the 200 μm mesa are deposited 7 μm wide and are of such length that the area of each is $1.1 \times 10^{-5} \text{ cm}^2$. If we multiply this by three and divide it into the specific contact resistivity we get 152 $\text{m}\Omega$. But all the current doesn't flow through a single resistor of this magnitude. We expect to get equal current collection from any one of the six spokes, so we divide this value by six as the equivalent resistance of the metal grid, or 25 $\text{m}\Omega$. Thus the first number of the fourth column in Table 3 under p Contact Resistance is the equivalent parallel resistance of the six 150 $\text{m}\Omega$ resistors. Placing the metal grid on the semiconductor mesa reduces current collection by the metal bus bars. We will neglect the contact resistance of the p mesa bus bar contact resistance. Including it would create another current path in parallel with the grid lines, so the estimate above is purposely left high. This is the opposite for the n type mesa contact. All the current in the lower mesa flows in this bus bar contact resistance.

For the n-mesa contact resistance we assume that the current splits evenly into two current paths in parallel. A feature in the photomask layout software dw2000 is that it will calculate the area of a given layer structure. The n-mesa contact structure area is $7.65 \times 10^{-5} \text{ cm}^2$, which includes both current paths. If we divide half of this number into the specific contact resistivity of $5 \times 10^{-6} \Omega \text{ cm}^2$, we get 130 $\text{m}\Omega$. Since this represents one of two equivalent current paths in parallel, the parallel equivalent resistance is 65 $\text{m}\Omega$. These values are listed in column 6 of Table 3. The last column in Table 3 is the sum of the n and p contact resistances.

300 μm Mesa

The grid lines for the p-mesa of this design consist of two types of lines of slightly different length. The contact area for the two types of lines are $9.10 \times 10^{-6} \text{ cm}^2$ and $9.13 \times 10^{-6} \text{ cm}^2$. If we call these numbers equal and divide it into the specific contact resistivity we get 550 $\text{m}\Omega$. We have twelve of these resistors in parallel, so we divide by 12 to get the equivalent contact resistance of the grid lines of 46 $\text{m}\Omega$. For the n-mesa contact the design program calculates the area to be $1.10 \times 10^{-4} \text{ cm}^2$. If we divide half this area into the specific contact resistivity we get the contact resistance of one of two equivalent current paths, 90 $\text{m}\Omega$, or a parallel equivalent resistance of 45 $\text{m}\Omega$. Alternatively, we could divide the whole area into the specific contact resistivity, getting 45 $\text{m}\Omega$ as the equivalent parallel resistance directly. Then the sum of the p and n contact resistance is 91 $\text{m}\Omega$, as shown in Table 3.

300 μm Mesa with Narrow Bus Bars

The grid lines for this structure with the narrower bus bars are of slightly different length than the previous case. Again there are two different lengths of lines. The design program calculates the area of these lines (lengths are radii to a vertex and to a flat side) at $9.611 \times 10^{-6} \text{ cm}^2$ and $8.323 \times 10^{-6} \text{ cm}^2$. If we divide each of these numbers into the specific contact resistivity and divide by six to get the equivalent parallel resistance of the six equal current paths, we get 87 $\text{m}\Omega$ and 100 $\text{m}\Omega$. If we now consider these two values as parallel connection, the equivalent resistance is 47 $\text{m}\Omega$. For the n-mesa contact the program tells us that the area is $6.25 \times 10^{-5} \text{ cm}^2$ and since this represents the area of two equivalent current paths, dividing this into the specific contact resistivity gives the equivalent parallel resistance of 80 $\text{m}\Omega$, or 160 $\text{m}\Omega$ for each parallel path.

1 mm Mesa

The 1 mm junction mesa was included in the mask design in order to have an array with a small number of fairly large junctions. So there is a seven junction series connection included. For the p-metal grid lines the program calculates the area of the two different lengths of lines as $2.9 \times 10^{-5} \text{ cm}^2$ and $3.37 \times 10^{-5} \text{ cm}^2$. Dividing these area numbers into the specific contact resistivity gives the resistance of a single line of length equal to a radius. Then dividing each by six gives the equivalent resistance of the six in parallel. This gives 29 m Ω in parallel with 25 m Ω , for an

Table 2

Resistance Component	Resistivity $\Omega\text{-cm}$	Thickness μm	Resistance m Ω
Buffer (Back)	4.6×10^{-4}	10	18
Base	4×10^{-3}	5	8 (200 μm) 3 (300 μm)
Emitter	2×10^{-2}	0.5	4 (200 μm) 2 (300 μm)
Top (Cap)	2.1×10^{-3}	5	166 (no grid) 14 (grid)

equivalent resistance of 13.4 m Ω . The n-mesa contact area is $3.66 \times 10^{-4} \text{ cm}^2$, and dividing this into the specific contact resistivity gives 13.7 m Ω for the parallel equivalent resistance of the two current paths. The sum then gives 27 m Ω for the total contact resistance.

2 mm Mesa

This large device was included in the mask design to provide a single junction device to measure and compare with known GaAs solar cell operating parameters. Using the same procedure as in the previous section we get 4 m Ω as the equivalent resistance of the grid lines. Using the n-mesa contact area of $1.34 \times 10^{-3} \text{ cm}^2$, we calculate 3.7 m Ω for the equivalent resistance of the parallel combination of the two current paths.

A summary of the contact resistance for each structure is shown in Table 3.

Table 3

Mesa Diameter (μm)	Mesa Area (cm^2)	p Contact Area (cm^2)	p Contact Resistance ($\text{m}\Omega$)	n Contact Area (cm^2)	n Contact Resistance ($\text{m}\Omega$)	Total ($\text{m}\Omega$)
200	2.6×10^{-4}	3.35×10^{-5}	25	7.65×10^{-5}	65	90
300	5.85×10^{-4}	1.02×10^{-4}	46	1.10×10^{-4}	45	91
300n	5.85×10^{-4}	1.08×10^{-4}	47	6.25×10^{-5}	80	127
1000	6.5×10^{-3}	3.77×10^{-4}	13	3.66×10^{-4}	14	27
2000	2.6×10^{-2}	1.31×10^{-3}	4	1.34×10^{-3}	4	8

Calculations assume specific contact resistivity, $r_c = 5 \times 10^{-6} \Omega \text{ cm}^2$, with $R = r_c/A$

5.3 Bulk Metal Resistance

Grid Line Resistance

The final resistance calculations are those for the bulk metal resistance for the grid lines and the bus bars. For the grid lines the electro-plating mask defines the grid lines one micron inside the ohmic metal deposition so the plated linewidth will be $5 \mu\text{m}$. One of the ways that the series resistance in these structures can be lowered is in the choice of metal to be used. Since there is an in-place process in the CSRL for plating gold, this will be the metal chosen. The bulk resistivity of gold is $2.44 \times 10^{-6} \Omega \text{ cm}$. Since the bulk resistivity of silver is $1.46 \times 10^{-6} \Omega \text{ cm}$, 40% less than gold, silver would be the optimum choice. Indeed, during the Si concentrator solar cell development at Sandia in the 1980s silver was the metal which was plated to carry high currents. So in making these calculations we will include both metals and assume that the lines will be plated to a thickness of $10 \mu\text{m}$. Since we know the width, length and thickness of the metal lines the calculations are similar to that used for the bulk semiconductor material, where the resistance is given by, $\rho L/A$. Table 4 contains all the parameters necessary to make the calculations. For all but the $200 \mu\text{m}$ mesa there are 12 grid lines, meaning there are six whose length is measured from the center to a hexagon side and six whose length is measured from the center to a hexagon vertex. Six of each type are in parallel, and in turn reduces to two resistors in parallel. Specifically, to get the $5 \text{ m}\Omega$ for Au on the $300 \mu\text{m}$ mesa, divide the $64 \text{ m}\Omega$ by six to find an equivalent resistance for these six in parallel, getting $10.67 \text{ m}\Omega$ and divide the $56 \text{ m}\Omega$ by six to find the equivalent resistance of six of this line in parallel configuration, getting $9.33 \text{ m}\Omega$. Finally we consider the $10.67 \text{ m}\Omega$ in parallel with the $9.33 \text{ m}\Omega$, getting $4.98 \text{ m}\Omega$. Since these calculations are very straightforward we leave it to the reader to verify them from the parameters in Table 4, if desired.

Bus Bar Resistance

The bus bar resistances are calculated the same as the grid lines using resistivity values for both gold and silver. Here we assume that the current splits evenly into two equivalent current paths.

All the relevant parameters and results are gathered in Table 5. Since these calculations are also straightforward we leave verification of them to the reader, if interested.

Table 4

Mesa Diameter (μm)	Mesa Area (cm^2)	# Radial Grid Lines	Grid Line Length (μm)	Grid Line Resistance ($\text{m}\Omega$)		Parallel Equivalent Resistance ($\text{m}\Omega$)	
				Au	Ag	Au	Ag
200	2.6×10^{-4}	6	80.4	39	23	7	4
300	5.85×10^{-4}	12	131.5 114	64 56	38 33	5	3
300n	5.85×10^{-4}	12	138.5 120	135 117	81 70	10	6
1000	6.5×10^{-3}	12	240 208	234 203	140 121	18	11
2000	2.6×10^{-2}	12	420 485	171 197	102 118	15	9

Calculations assume plating to a thickness of $10 \mu\text{m}$.

Table 5

Mesa Diameter (μm)	Mesa Area (cm^2)	p-Bus Bar Length (μm)	p-Bus Bar Width (μm)	n-Bus Bar Length (μm)	n-Bus Bar Width (μm)	Equivalent Parallel Resistance ($\text{m}\Omega$)			
						p-Bus Bars Au	Ag	n-Bus Bars Au	Ag
200	2.6×10^{-4}	263	13	269	12	25	15	27	16
300	5.85×10^{-4}	415	12	394	12	42	25	40	24
300n	5.85×10^{-4}	426	6	388	6	86	52	79	47
1000	6.5×10^{-3}	488	13	1309	12	138	83	133	80
2000	2.6×10^{-2}	2985	22	2543	22	165	99	141	84

Calculations assume plating to a thickness of $10 \mu\text{m}$.

Table 6

Mesa Diameter (μm)	Mesa Area (cm^2)	Total Series Resistance Estimate ($\text{m}\Omega$)	
		Au	Ag
200	2.6×10^{-4}	193	169
300	5.85×10^{-4}	215	180
300n	5.85×10^{-4}	339	269
1000	6.5×10^{-3}	353	238
2000	2.6×10^{-2}	366	237

6.0 Input Optical Power Requirements

Table 1 and Table 6 contain encouraging information in that for input laser power of 1 kW, and with high photon blocking percentages, the 417 junction arrays will generate short circuit currents on the order of 0.5 amp, which results in capacitor charge times close to 1 μSec . Then Table 6 indicates that using plated Au the series resistance is on the order of 200 $\text{m}\Omega$, and taken times the short circuit current results in an internal voltage drop of 100 mV. Thus the array voltage under these conditions will be 417 volts. Table 6 contains the estimate of the sum of all the contributions to the series resistance from the other Tables.

For the 241 junction arrays the short circuit currents are between 0.7 amp and 0.9 amp giving charge times of 0.3 μSec and 0.2 μSec , respectively. These short charge times indicate that the input laser power could be reduced by a factor of 1/4, to 250-300 watts and still meet the 1 μSec requirement. However, as discussed before, two of these arrays would have to be used in series to develop the required voltage. With the higher short circuit currents and the same series resistance per junction the internal voltage drops become 140 mV for the 0.7 amp current and 180 mV for the 0.9 amp current. With the junction voltage of 1.1 volts, the terminal voltage per junction would be 0.96 volt and 0.92 volt, respectively. Then multiplying by the number of junctions in the array we get 231 volts and 222 volts, indicating that with two in series we may have some margin if 400 volts are required.

Summary

Series connected converter arrays containing 241 junctions and 417 junctions have been designed for capacitor charging applications. The charge time target for charging a 1 nF

capacitor to 400 volts was 1 μ Sec. A simple calculation shows that a current of 400 mA flowing in that 1 μ Sec would produce the required voltage. Since the junction voltage of any GaAs PV junction is about 1.1 volts, and since each junction voltage in the series adds to the array terminal voltage, the number of junctions in the series must be close to 400. The 417 junction array is designed to meet the requirements as a single chip and the 241 junction array is designed to be used as a pair wired in series, each with independent illumination. Because the photon losses for the 241 junction arrays are smaller than for the 417 junction arrays, and because the beam is partitioned into fewer pieces, the required input optical power for each laser is estimated at 250-300 watts instead of 1 kW required by the single 417 junction chip. Thus, the total required laser power of 500-600 watts for the two chip approach is somewhat less than the total required for the single chip approach. However, this lower required power must be weighed against increased total complexity in system design.

The approach used in designing these converters was to incorporate enough series connected junctions so that the required voltage would be obtained before the operating point moved past the knee of the I-V curve. In order to obtain the required voltage the series resistance of each junction must be low. With the junction voltage for each at about 1.1 volts the target resistance was 100 m Ω , which, when multiplied by a current of 1 amp, would result in an internal voltage drop of 100 mV, leaving the terminal voltage for each junction at 1 volt. Since the capacitance, voltage, and charge time are fixed, the required current is easily calculated. Thus PV junctions have to be designed that are large enough to absorb enough photons to produce currents on the order of 1 A, and yet small enough that a series connection of 417 junctions produces a chip of usable size. The 417 junction array using the 300 μ m hexagon junction produced a 7.4 mm x 7.4 mm chip with a beam diameter of 7.2 mm. Given space constraints in the application this chip size was considered a maximum. So it was decided to design arrays of 241 junctions and 417 junctions using 200 μ m and 300 μ m hexagon junctions and to put large enough current collecting metal lines on them to carry 1 A with small resistance losses. This approach will clearly produce converter junctions with high photon losses but these losses can be regained by increased input optical power, whereas high internal voltage drops due to high series resistance per junction cannot be reduced once the chip is fabricated.

In comparing the results in Table 1 for the two types of arrays using the different junction sizes the charge times are not a very strong function of the size of the individual junctions. However, it must be kept in mind that the charge times in this Table were calculated assuming no series resistance. For example, the 0.18 μ Sec charge time for the array 241-300n is lower than the other two 241 junction arrays. However, this array was purposely designed with narrow bus bars and will likely have high series resistance as indicated in Table 6. The shorter charge time just reflects the fact that the short circuit current is somewhat higher due to less photon blockage. Also, from Table 6, it is seen that the estimated series resistance for the two junction sizes are not greatly different. The higher resistance for the 300 μ m array is likely just due to complex interplay between the length of metal lines, contact area, and resistance of the bulk semiconductor material, which is area dependent.

Finally, from these calculations it is to be concluded that, based on known properties of PV converters and the semiconducting materials, the requirements for the capacitor charging application can, in principle, be met. Two caveats apply. First, it will take high input optical power, on the order of a kilowatt for the single chip. And second, the junctions must be fabricated with internal series resistance less than 200 m Ω .

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