A HIGH POWER LINEAR SOLID STATE PULSER

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Abstract

Particle accelerators usually require high voltage and high power. Typically, the high voltage/power generation utilizes a topology with an energy store and switching mechanisms to extract that stored energy. The switches may be active or passive devices. Active switches are hard or soft vacuum tubes, or semiconductors. When required voltages exceed tens of kilovolts, numerous semiconductors are stacked to withstand that potential. Such topologies can use large quantities of crucial parts that, when in series, compromise a system's reliability and performance. This paper describes the design of a linear, solid state amplifier that uses a parallel array of semiconductors, coupled with unique transmission line transformers. This system can provide output signals with voltages exceeding 10 kV (into 50-ohms), and with rise and fall times (10-90 percent amplitude) that are less than 10-ns. This solid state amplifier is compact, modular, and has both hot-swap and soft-fail capabilities.

1 INTRODUCTION

Development of the High Power Linear Solid State Pulser (HPLSSP) is a continuation of kicker modulator work at Livermore, CA. The present hybrid solid state and planar triode kicker modulator [1] is being upgraded; the solid state complimentary stage hybrid microcircuit (HMC) will replace the first stage (YU-176 planar triodes) that drives the grids of the Y-820 output tubes.

Recent advances in high power impedance "matchers" [2], [7] (Transmission Line Transformers or TLTs) encouraged us to develop an all, solid state, linear pulser. This pulser uses Coplanar Kelvin leaded MOSFETs [3] in an open loop, delayed feedback architecture, and relies upon distortion compensation [4] to assure an acceptable output. Figure 1 is a simplified block diagram of that system. All of the signal paths from the 84X splitter to the 50-ohm load are in transmission line configurations.

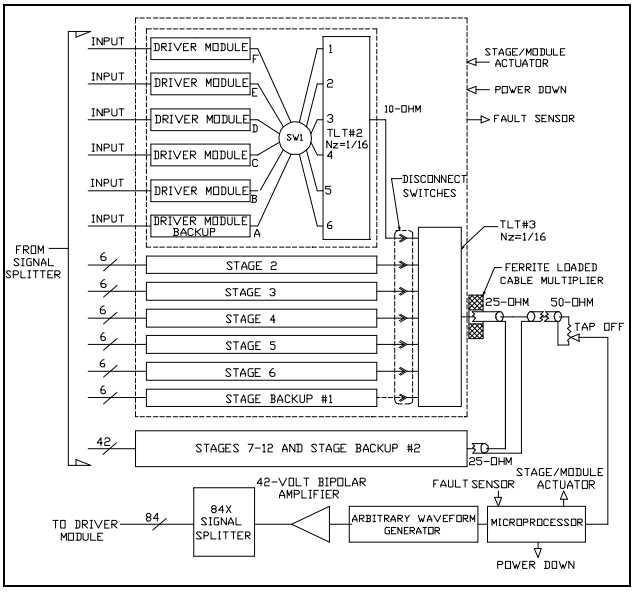

Figure 1: Simplified HPLSSP system block diagram

2 SYSTEM RELIABILITY

Key to the success of any system is reliability; reliability is dependent upon operating time and failure rate. Failure rate is related to the number of crucial parts that must function in order for the system to perform its mission. For applications (such as beam splitting) in large scientific machines, down time translates into wasted expenditures. Reliability can be enhanced by 1) Pre-screening components. 2) Pre-testing components and modules, 3) Reducing the quantity of critical serial parts, 4) Designing redundancy into the operating system, and 5) Using passive components when possible.

A parallel, modular system with passive voltage multiplying TLTs is especially attractive for highly reliable systems. Such a system's reliability or probability of success can be expressed mathematically [5] as:

$$P_N = 1 - (1-P_o)^N$$

Where: P_N = Success Probability of N parallel systems.
P_0 = Success Probability for one system.
N = Number of parallel systems.

The current HPLSSP system has a 20% redundancy. There are six parallel channels in each module (five active and one backup) and 14 modules (12 active modules) in this system. This topology, however, will adapt to any number of parallel modules/systems, limited only by time and cost constraints.

Should one of a module's active five channels fail, the system computer will inhibit the defective channel, activate that module's backup channel through an impedance-matched switch, SW1. If a second channel fails in that same module, the computer will power down the entire module and disconnect it from the system (by disengaging its transmission line edge connector). One of the system's two redundant modules will then be put into service (see Figure 1). With each configuration change due to component/module failure, new predetermined distortion compensating information is downloaded to the computer to compensate for any

differences between the failed and the backup components/modules. This modular system will tolerate failures in any two of its twelve modules without service interruptions. The system also has hot swapping capabilities for servicing and maintenance.

Compactness and weight advantages of the HPLSSP make it attractive for airborne and space applications. These advantages are possible because of parallel-ground referenced modules, open loop architecture and high ratio impedance TLTs that use less magnetic material than conventional TLTs. See section 4 for TLT descriptions.

3 SOLID STATE MODULE

A simplified block diagram of the solid state module is shown in Figure 2. It has three stages; 1) An Operational Trans-conductance Amplifier (OTA), 2) A TLT, and 3) The MOSFET pair.

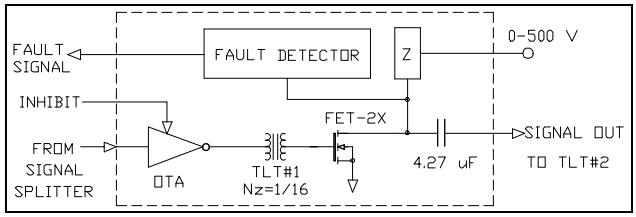

Figure 2: Solid State Module simplified circuit.

Within the OTA stage is a voltage-to-current (V/I) converter, video amplifier, two bipolar transistors and a high bandpass RF transistor. A current source is necessary because of the large dynamic changes to the video amplifier's input impedance during its operation. The V/I converter can supply ±75 ma. The OTA's video amplifier is biased from the dc rails (to avoid signal saturation) and has a fixed voltage gain of about 20. Its output signal swings from 5 to 75 volts. The ac coupled final stages of the OTA (the complimentary pair and R.F. transistor) are all in emitter-follower configurations. Their rise and fall times (10-90%) are less than 3-ns. The maximum linear output from the OTA is about 2.4-amps into 25-ohms.

RF techniques are used in the PC board's layout and in its construction. The output of the OTA's is through two edge-launched, 50-ohm connectors whose center conductor merge to provide a 25-ohm input to TLT1.

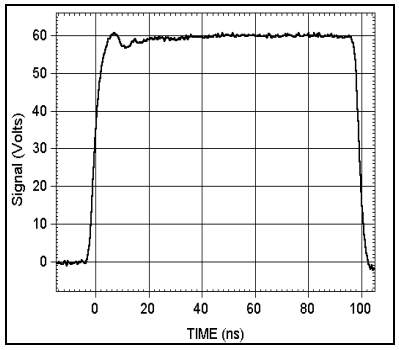

Figure 3: OTA Signal Output

The OTA stage is driven by a 500-mV signal from the system's 84-way splitter. Figure 3 depicts the display of a typical output signal from the OTA.

TLT1 has a 16:1 impedance ratio (25-ohms input, 1.6-ohms output). See section 4 for more details on TLT1. The low impedance from TLT1 is used to charge and discharge the gate capacitance of two parallel MOSFETs (from Directed Energy, Inc). This particular MOSFET is chosen specifically because of its physical and thermal attributes that are conducive to high speed and power applications [3]. The MOSFET parallel combination will deliver over 400-volts into a 3.2-ohm load. The MOSFET footprint (excluding leads) is 1.80-cm x 2.54-cm.

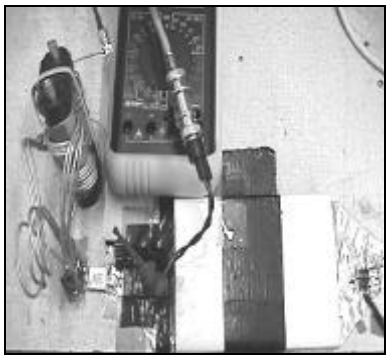

Figure 4: Single channel setup of Solid State Module

The MOSFET operates at less than 450-volts (it is a 500-volt device). A 4.27-μF signal coupling capacitor isolates the 450-volts from all components downstream of the MOSFET. Figure 4 is a photograph of the test setup used to dup-licate one of the Solid State Module's five active channels. The TLT for this experiment is oversized, but the output impedance is the same as that of TLT1. Figure 5 graphically depicts the signal output from that simulated channel. The data were acquired by driving the gates of the MOSFET pair to about 15-volts with a series, 0.5-ohm gate resistor while having a 450-volt drain voltage, and a 3.2-ohm load. The signal's fall time is about 5-nanoseconds. This test clearly demonstrates the Solid State Module's ability to deliver an acceptable input to TLT2.

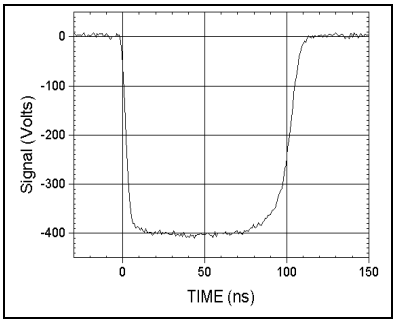

Figure 5: Single channel output of Solid State Module

4 NEW TLTS

The TLTs described in this paper differ significantly from traditional TLTs [6] by combining both strip and semi-rigid transmission cables so that signal propagation is uninterrupted by segmented, coaxial connectors or lines. Moreover, not all of the new TLT's transmission lines need magnetic cores. These improved TLTs can have impedance ratios as high as 250:1 with sub-nanosecond response even at relatively high power levels. They use balanced windings of both strip and semi-rigid coaxial transmission lines on cores of Mn-Zn ferrite.

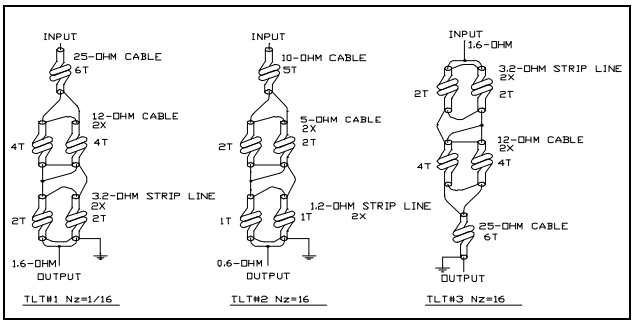

Figure 6: Single channel setup of Solid State Module

Figure 6 shows the general winding diagrams of TLT1, TLT2 and TLT3. The winding turns, T, are relative opposed to absolute numbers. The core's physical dimensions are 2.54 x 3.18 x 0.64 cm. for TLT1 and 6.45 x 8.08 x 2.40 cm for both TLT2 and TLT3.

TLT1 provides a 1.56-ohm drive from the OTA. This low impedance allows a rapid charge and discharge of the FET gate capacitance (includes the Miller effect). Rise and fall times of TLT1 are less than 600-ps, i.e. TLT1 has only minor effects on the system's overall bandpass. This is also true for TLT2 and TLT3.

TLT2 increases the 400-volt signal from the FET to about 1.6 kV. TLT2's input and output characteristic impedance is 0.6 and 10.0-ohms respectively. A TLT similar to TLT2, but with a 16:1 impedance ratio, was evaluated relative to signal droop caused by core non-linearity and/or saturation. Figure 7 (input) and Figure 8 (output) show the experimental results. Note that this particular TLT inverts the input signal. Without core biasing, its output signal follows the input signal for almost 800-ns before core effects become evi-dent.

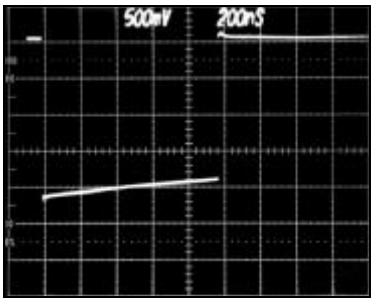

Figure 7: TLT Input Signal

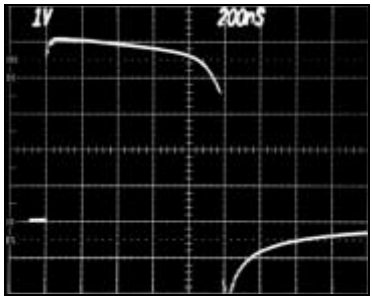

Figure 8: TLT Output Signal

TLT3 steps up the 1.6 kV signal output from TLT2 to about 6.4 kV. This signal amplification is possible because of the TLT's characteristic impedance change from an input of 1.6-ohms to a 25-ohms output.

A cable multiplier sums the two TLT3 output signals into 50-Ohms resulting in a final output of about 12 kV.

5 COMPUTER CONTROL

The front end of the Solid State Module needs optimizing to bring the temporal behavior of its signal into acceptable parameters – to "linearize" the signal. We implement defined, pre-distortion to the input signal to obtain sharp rise and fall times of the solid-state module's output signal. A similar algorithm [1], [4] is used to linearize the main amplifier. The parameters for these algorithms are predetermined and stored for access by the HPLSSP's computer. Whenever the HPLSSP is operated, the main input signal controlling the arbitrary waveform generator is initiated only after the correct parameters are accessed for the solid state modules, and the overall system.

The same computer that provides predetermined input distortions to the input signals of the HPLSSP will also repeatedly check for the operational integrity of the Solid State Modules. Shown in the block diagram of Figure 1 (of section 1) is a fault sensor network for each module of the HPLSSP. As describe in section 2, if components or modules malfunction within the system, the computer will sense the problem and replace the faulty components or modules with their spares through electrical inhibitors and actuators.

6 SUMMARY

We have presented the description and supporting data for an ultra reliable, computer-controlled, HPLSSP. With proper linearization the HPLSSP performs as a high powered (10-kV, 200-amp), fast rise and fall time (<10-ns) arbitrary waveform generator with the following features:

1) A ground referenced, low voltage, parallel component, modular system
2) A low cost, easily fabricated/maintained system using state-of-art components.
3) A passive, high bandpass (sub-nanosecond rise time), V/I multiplying TLT design.
4) A graceful degrading system with low component count.
5) An open loop, computer controlled pulser.

7 ACKNOWLEDGMENTS

We acknowledge the BN/LLNL ETA II team for their valuable support and express appreciation to Mr. J. Pigg (Project Manager) for his encouragement and guidance.

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