Technology Support for Initiation of High-Throughput Processing of Thin-Film CdTe PV Modules

**Phase II Technical Report
14 March 1996 - 13 March 1997**

R. Sasala, R. Powell, and G. Dorer
Solar Cells, Inc.
Toledo, Ohio

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NREL technical monitor: H.S. Ullal

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Contents

Figure List.....	ii
Abstract	iii
Introduction.....	1
CdTe Deposition.....	1
Chloride Treatment.....	7
Interfacial Layer	8
Interconnection	12
Electrode materials	13
Contact resistivity.....	14
Fabrication	16
Efficiency Improvements.....	16
Stability	21
Light soaking.....	22
Discussion.....	22
Outdoor array.....	23
Summary	26
FUTURE PLANS	26
References	27

Figure List

Figure		Page
Figure 1	Sequence of depositions by VTD made at increasing pressures	3
Figure 2	CdTe thickness for new deposition system for both the cross-web (a) and down-web (b) directions	4
Figure 3	Typical micrographs of an as-deposited surface of VTD CdTe film	5
Figure 4	Example of pinholes in a CdTe film made by VTD, which has been subjected to an abrasion test.	6
Figure 5	I-V curve for CdTe deposited with new deposition apparatus onto CSS CdS	6
Figure 6	Schematic of vapor CdCl ₂ treatment apparatus	7
Figure 7	I-V data for a cell which was subjected to a two step HCl heat treatment	9
Figure 8	Near record mini-module (record = 10.7%) which has a Te IFL which was deposited using rf-sputtering	10
Figure 9	I-V data for a device made with a vapor transport Te IFL.	10
Figure 10	I-V data for a device made with back contact materials consistent with vapor transport deposition techniques	11
Figure 11	Schematic diagram of dot matrix interconnection	12
Figure 12	Efficiency vs. time for four alternate back contact metals which are compatible with dot matrix interconnection and high throughput manufacturing	13
Figure 13	Efficiency vs. time data for composite metal structure used for dot matrix interconnection	14
Figure 14	I-V data for highest efficiency dot matrix interconnected module produced to date	15
Figure 15	Separation of current loss mechanisms for a standard device with thick CdS. (From Gunther Stollwerck's MS thesis from Colorado State University.)	17
Figure 16	I-V curve for record 1 cm ² SCI device. The device has an i-SnO ₂ buffer layer on the TCO and a 400 Å CdS thickness	18
Figure 17	Quantum efficiency from SCI's record 1 cm ² device deposited on 3mm soda lime glass. Note the large increase in blue response and the slightly higher red response due to thinner CdS and glass respectively	19
Figure 18	I-V curve for record small area SCI device. The device was deposited on 1mm soda lime glass with TCO deposited by Asahi Glass	20
Figure 19	Quantum efficiency from SCI's record small area device deposited on 1 mm soda lime glass. Note the relatively flat red response due to the thin substrate	21
Figure 20	Efficiency of minimodules made with the standard process and subjected to continuous light soak while being held near the maximum power	22
Figure 21	Comparison of device performance between standard wet process and dry Te IFL when held at open-circuit under continuous illumination	23
Figure 22	Power output of SCI Westwood 1.2 kW array normalized for intensity variations but not for temperature fluctuations	24
Figure 23	Power output of SCI Westwood 1.2 kW array normalized for intensity variations and corrected for temperature variations from 25 °C	25
Figure 24	Power output (normalized for intensity variations) of the SCI 1-kW array installed at NREL in June 1997	

Abstract

Research at Solar Cells Inc. is focused on developing processes which will lead to high volume and low cost manufacturing of solar cells and to increase the performance of our present technology. The process research has focused on developing vapor transport deposition of the semiconductors, eliminating wet chemistry steps while minimizing the chloride treatment time, forming a low-loss back contact using only dry processing, and an improved interconnection technique. The performance improvement work has focused on the increase of the photocurrent by a combination of more transparent glass substrates and a thinner CdS window layer deposited on an i-SnO₂ buffer layer. SCI record 13.0% 1 cm² devices have been fabricated using these techniques. Stability monitoring continues and shows minimal degradation for over 20,000 hours of continuous light soak at 0.8 sun illumination.

INTRODUCTION

The goal of Solar Cells Inc. is to develop the technology to produce photovoltaic modules in volumes sufficient to compete with the economics of conventional electric technologies. CdTe is the material of choice due to its demonstrated good performance both in the laboratory and in pilot production manufacturing. Furthermore, the deposition methods under development are consistent with eventual integration with a commercial scale glass float line. This approach shapes both the direction of research and the priority that experiments are performed. SCI is investigating processes which shorten and/or simplify deposition and post-deposition procedures, flow in a logical manufacturing sequence and permit in-situ processing of all deposited layers. A specific example is the chloride treatment which is used by most CdTe workers to optimize device performance. The standard chloride treatment is typically 30 minutes long and requires several wet processing steps. Therefore, either a long in-line treatment chamber or a batched oven is required, both of which are undesirable for manufacturing. A second area is the development of a low-loss back contact formed with strictly dry processing and applied either under vacuum or at atmospheric pressure continues. Optimization of the performance and stability of devices made by processes altered for scale or speed remains an active area.

The focus of this report will be to review the advances towards commercialization of CdTe photovoltaics that SCI has made over the past year with the assistance of funds from NREL. The two areas to be addressed are device processing and device performance. The processing includes improved semiconductor deposition, chloride treatment, back contact formation and interconnection. Performance improvements include increases in device efficiency and an update on continuing stability testing.

CdTe DEPOSITION

SCI has developed a system for large area coating of CdS/CdTe films that can operate for the extended intervals required in production. The system features on-demand raw material supply, reliable vapor generation, uniform vapor distribution, high deposition rates and controlled film coverage. Previously SCI had employed a large-scale modified close-spaced sublimation vacuum deposition process operating at pressures near 1 Torr. The transport of material from the array of batch-loaded, powder-filled source trays to the substrates is diffusion controlled. Likewise in laboratory close-spaced sublimation depositions, the transport of material is diffusion controlled but pressures of 10 to 30 Torr can be used due to smaller source-to-substrate distances.

Material transport in the gas phase due to total pressure gradients can also be used. Pressure gradients can be created using sublimation pressure or carrier gas or both. For example, using inert carrier gas, Tuller et al. (1) and Chu et al. (2) have deposited CdTe at high pressure, and SCI has patented a vacuum deposition modification of close-space sublimation using carrier gas.(3) We have also deposited CdS and CdTe on a small scale at pressures up to 600 Torr using N₂ carrier gas (4). The high vapor pressures of CdS and CdTe at temperatures above 700 C are favorable for creating usable total pressure gradients by sublimation. Thus, a metal laden gas stream can be generated, transported, distributed, and directed

towards a stream of moving flat glass. We will designate coatings deposited in this manner as vapor transport deposition coating (VTD).

SCI has tested a full-scale VTD apparatus. Films have been deposited at pressures between 2 and 50 torr with growth rates exceeding 5 $\mu\text{m}/\text{min}$. At high supersaturations and high pressures, homogeneous nucleation can occur resulting in poorly bonded coatings. Figure 1 shows a sequence of depositions made at increasing pressures. The darker areas are poorly bonded regions resulting from homogeneous nucleation. At lower pressures well-bonded uniform films can be formed.

Film thickness uniformity in the direction of glass travel has been excellent, typically $\pm 5\%$. Cross web thickness uniformity can be controlled to within acceptable limits with the proper combination of operating parameters. Figure 2 shows the thickness uniformity of the plate shown in Figure 1a in both the cross web and down web directions. Note the well-defined boundary of the coating along the long glass edges evidenced in both Figures 1 and 2. The boundary demonstrates control of "overspray" and thus absence of material waste at the web edge. Also note the rapid turn-on and off of the deposition in the down web direction and the uniformity of the film during deposition. All of these depositions were performed at target line speeds for 10 MW/year/shift production.

The VTD CdTe films have been deposited at rates exceeding 5 $\mu\text{m}/\text{min}$. Figure 3 shows a typical micrograph of an as-deposited surface. Although the VTD method is quite different from CSS, the microstructure features of the films can be similar. The dependence of microstructure on growth parameters is under investigation for both CdS and CdTe. Subtle differences have been noted but microstructures adequate for 10% devices has already been achieved.

Pinhole number densities are also an area of study. We have found that there are differences amongst various injector designs. In addition, we have found that, in some films, the pinhole number density can be substantially increased with a mild abrasion test. In higher quality films, few, if any, additional pinholes are formed by the abrasion test. Thus, this test is more stringent than pinhole counts on as deposited films. For example, figure 4 displays a photo of pinholes in a poor VTD CdTe film. The increased number of pinholes in the center of the photo was formed with the mild film abrasion test. This test consists of moving the coated superstrate at 1 to 5 cm/s underneath a spring loaded plunger. The tip of the plunger is a rubber foot usually covered with a felt pad. 5 to 20 psi loading is used.

Normal microstructure and low pinhole counts allowed devices to be made from some films. The first small-area devices were made using CSS CdS and VTD CdTe. (To date we have not yet configured the system to deposit CdS and CdTe sequentially using VTD.) An example I-V curve from a cell with over 10% efficiency is shown in Figure 5. Device parameters are comparable with standard cells made on similar thickness CdS/CdTe layers deposited by CSS. Thus, we have demonstrated the existence proof of good devices made from VTD films coated at high rates.

The new deposition equipment provides a new level of control over film growth, particularly the local deposition rate, material utilization and film uniformity. The system has been used to deposit onto a intermittent stream of glass. Even under these conditions, films of both CdTe and CdS with microstructures similar to standard CSS material have been deposited. Initial electronic properties assessment has been promising. Methods to reduce pinhole number densities to levels similar to standard CSS have also been established. Therefore, we expect that upon finishing the present system re-configurations, full-size modules with VTD CdS and VTD CdTe can be made with a high probability of high efficiency.

Figure 1 Sequence of depositions by VTD made at increasing pressures (lowest pressure at top). Homogeneous nucleation leads to poorly bonded films at higher pressures. Areas of poor bonding appear dark

Figure 2. CdTe thickness for new deposition system for both (a) the perpendicular to direction of glass travel (cross-web) and (b) parallel to direction of glass travel (down-web) directions.

(a)

(b)

Figure 3 Typical micrographs of an as-deposited VTD CdTe film; (a) surface (b) cross section.

Figure 4. Example of pinholes in a poor VTD CdTe film which has been subjected to an abrasion test. The photographed area measures 35x25 mm.

I-V data for new CdTe deposition apparatus

Figure 5. I-V curve for CdTe deposited with new VTD apparatus onto CSS CdS.

CHLORIDE TREATMENT

Work on implementing the chloride treatment for manufacturing has focused on elimination of wet processes and reduction of treatment time. Successful use of HCl vapors as a chloride treatment agent has previously been reported using similar treatment temperatures and times as the conventional treatment (5). Recent work has examined the potential of treatment with either CdCl₂ vapors and HCl vapors for shorter duration.

The CdCl₂ vapor experiments were conducted in a quartz tube furnace which has separate heating zones for the CdCl₂ source material and the substrate. The furnace also has provisions for the use of a carrier gas to assist the transport of the CdCl₂ vapors. A functional schematic is shown in Figure 6. Nitrogen gas is introduced through quartz tube at A. The gas is preheated by passing through a helical heating element (C). The preheated N₂ gas then flows through a graphite enclosure (E) containing a charge of CdCl₂ which has been heated to a predetermined temperature by a collar heater (D). The temperature of the CdCl₂ charge is selected to yield a desired partial pressure. The mixture of CdCl₂ and N₂ vapor is then transported into a graphite sample holder (G) where it passes over the surface of a CdTe film sample (F). The CdTe sample and holder are heated to a predetermined temperature by external elements (I) and (J). Finally, the N₂/CdCl₂ vapor stream is then pumped from the system through exhaust tube (H).

Figure 6. Schematic of vapor CdCl₂ treatment apparatus.

The process parameters that were investigated include the source temperature (i.e. the partial pressure of the CdCl_2 vapor), the substrate temperature, total pressure, carrier gas flow rate and treatment time. Variations of the combinations of the process control variables were dictated by using design-of-experiment methods. This allowed a significant reduction in the number of experiments that needed to be conducted before trends can be evaluated and refinements made to the process.

The initial goal of the vapor CdCl_2 experiments was to determine the minimum treatment time required to produce the effect of a full standard wet CdCl_2 treatment. While there were some 9% efficient devices made with a treatment time as low as 60 seconds, consistent results required a minimum treatment time of 5 minutes. The 5 minute treatment consistently produced devices in the 10 % range but did not produce open-circuit voltages as high as the standard treatment. The V_{oc} was typically less than 800 mV. One advantage of the vapor CdCl_2 treatment is the potential of performing the treatment without leaving a residue. Wet CdCl_2 processing leaves a residue which must be rinsed prior to contacting. Prevention of residue formation is accomplished by maintaining a sufficiently high substrate temperature during or after treatment so as to prevent condensation.

Experiments have also been conducted to explore the reduction of process time for the vapor HCl treatment in a similar manner as was found for the vapor CdCl_2 treatment. The vapor HCl treatments were conducted at atmospheric pressure with a mostly inert ambient. The process control variables for the experiment include the substrate temperature, the HCl concentration and treatment time. HCl treatments tended to produce devices with higher V_{oc} 's than the vapor CdCl_2 method with 800 to 820 mV being typical. Device efficiencies over 10% were routinely produced. Similar to vapor CdCl_2 treatments we find 5 minutes to be the approximate minimum treatment time for reproducible high quality devices. We have found that optimum treatment substrate temperatures vary with the treatment medium. Vapor CdCl_2 treatments were found to work best with substrates between 420 °C and 440 °C. HCl, however, seems to require a somewhat lower substrate temperature, typically 380 °C to 400 °C.

Success has also been achieved using a two step HCl process in which the substrate is exposed to concentrated HCl gas for less than 60 seconds and subsequently annealed for 1 to 5 minutes in a N_2 atmosphere at temperatures in the 400 °C range. Cells with efficiencies above 10% have been made using this technique. An I-V curve for such a device is shown in Figure 7. Since this device has a thick layer of CdS, the 10.4% efficiency is considered to be good.

INTERFACIAL LAYER

Formation of a low-loss contact to p-type CdTe requires special processing. It has been found that surface preparation of the CdTe is critical for fabrication of high quality devices and that, because of the polycrystallinity of these films, the contacting procedure can often affect the "bulk" properties of the films. These bulk effects have their most profound effect on the open-circuit voltage and the shunt resistance.

Most of the traditional surface treatments have included wet etch steps, such as a bromine ethanol mixture, which create a Te-rich layer on the CdTe surface. SCI has developed it's own proprietary surface treatment which also involves wet processing. However, dry vapor processing is preferred for manufacturing. Thus, work has been performed on replacing the wet processing with direct deposition of Te. Initial efficiencies similar to standard wet treated devices have been observed in devices on which Te has been deposited with a variety of techniques including RF diode and DC magnetron sputtering, e-beam evaporation, and close-space sublimation. In fact, near record mini-module performance has been achieved with a deposited Te interfacial layer (IFL). Data for this device is shown in Figure 8.

I-V for two step HCL anneal

Figure 7. I-V data for a cell which was subjected to a two step HCL heat treatment.

Most of the work performed to date has been with RF diode sputtered Te. The Te thickness is generally greater than $100\text{\AA}$, which is consistent with the required thickness reported by Niles et. al.(6). Greater thicknesses with proper treatment can be used without significant performance variations. Studies have shown some performance variation with thickness from $1,000\text{\AA}$ to $5,000\text{\AA}$ when annealed in air or nitrogen at temperatures ranging from $100\text{ }^{\circ}\text{C}$ to $325\text{ }^{\circ}\text{C}$. The results of these studies indicate that increasing the thickness of as-deposited Te indicate a lower incidence of shunts and an improvement in stability but at the expense of higher series resistance. It appears that thickness in the range of $1,500\text{\AA}$ to $2,500\text{\AA}$ is adequate. Annealing in air had the effect of lowering the series resistance; the optimum temperature being in the $275\text{ }^{\circ}\text{C}$ to $325\text{ }^{\circ}\text{C}$ range.

Recent work has focused on CSS deposition of Te. Because of the relatively high vapor pressure of Te, high deposition rates are readily achieved by simple sublimation. Deposition rates as high as $500\text{\AA/s}$ have been observed and have been used to produce 10% efficient devices, as shown in Figure 9, with characteristics similar to devices with sputtered Te films. Consequently, it appears that Te can be easily deposited in a manner similar to our CdS and CdTe deposition technology (VTD) and will not require more costly sputtering or e-beam evaporation.

Solar Cells Inc. CdS/CdTe

Sample: B14322D5
Feb 1, 1995 8:18 AM
ASTM E 892-87 Global

Temperature = 25.0°C
Area = 63.77 cm²
Irradiance: 1000.0 Wm⁻²

$V_{oc} = 6.568$ V
 $I_{sc} = 0.1438$ A
 $J_{sc} = 2.255$ mAcm⁻²
Fill Factor = 71.17 %

$V_{max} = 5.210$ V
 $I_{max} = 0.1291$ A
 $P_{max} = 672.3$ mW
Efficiency = 10.5 %

Figure 8. Near record mini-module (record = 10.7%) which has a Te IFL which was deposited using rf-sputtering.

I-V data for VTD Te IFL

Figure 9. I-V data for a device made with a vapor transport Te IFL.

Tests have been conducted to determine the ability of the Te IFL to withstand elevated temperatures which it may be subjected to during subsequent processing. The experiment was to simply heat, in air, substrates with RF sputtered Te to temperatures from 200 °C to 325 °C for 30 minutes and then complete the devices in the standard manner. There was no observable difference in the performance of these devices which was outside the normal experimental variation. If the Te deposition is performed prior to the chloride treatment, the device performance will be extremely poor. Thus the preferred sequence is semiconductor deposition, chloride treatment and then Te deposition. We have found that the best depositions of Te onto CdTe using close-space sublimation are for substrate temperatures below 400 °C and therefore processing sequence and temperature requirements flow naturally. This is convenient for a in-line process as the Te can be deposited onto the chloride treated CdTe without requiring any additional heat to achieve the required substrate temperature.

In addition, use of a Te IFL leads to a notable improvement in the stability of devices tested under open circuit conditions in continuous light-soak. More will be discussed on this in a later section. Another important advantage of the Te IFL is that it permits the use of a greater variety of metallic back contacts. This is important from a manufacturing perspective because it opens the opportunity to deposit metals under similar deposition conditions as used for the semiconductors. These conditions have been chosen because of their compatibility with low-cost high-throughput manufacturing. I-V data for a device made with a metal that can easily be deposited under these conditions is shown in Figure 10. The performance is similar to what is expected with the standard contact.

I-V data for alternate back contact

Figure 10. I-V data for a device made with back contact materials consistent with vapor transport deposition techniques.

The Te IFL also exhibits excellent adhesion as demonstrated with standard tape tests (a 3M #600 tape no effect on the adhesion of Te to the CdTe). Furthermore, the use of Te allows the use of adhesion promoting layers to increase the adhesion of subsequent back metals which actually carry the bulk of the current. The increased adhesion further bolsters the confidence of the durability of modules. Furthermore, the excellent adhesion is important for some of the processing step required in our next generation interconnection as will be discussed next.

INTERCONNECTION

The present technique to isolate and interconnect adjacent cells in a module includes three separate laser scribes which must be precisely registered to each other. The pilot production laser system is a single beam Nd:YAG based laser system which requires more than one hour to complete the series of scribes. To transfer this technology onto a continuous manufacturing line will require multiple lasers each of which are split into multiple beams. This will undoubtedly be an expensive and challenging engineering project.

As an alternative interconnection technique, SCI is refining its patented "dot matrix"(7) interconnect structure. This structure makes use of two metallic electrodes, M1 and M2, on the back of the cell, separated by a dielectric layer in a sandwich arrangement. A schematic diagram of the interconnection technique is shown in Figure 11. The M1 electrode is the rear electrode of the cell. The M2 electrode is connected to the front, transparent, TCO electrode through a matrix of round vias made in a insulating layer and also to the M1 electrode of the adjacent cell through a row of similar vias. In this manner the M2

DOT MATRIX SECTION

Figure 11. Schematic diagram of dot matrix interconnection.

electrode carries the current collected by the TCO electrode to the adjacent cell. Due to the fact that the sheet resistivity of M2 can be made much lower than that of TCO the cells can be made 5 to 15 cm wide, compared with 1 cm for the "line-patterned" modules. The expected benefits of the dot matrix structure are: 1) a 10% to 15% increase in power output due to reduced module area losses and reduced I^2R losses in the TCO, 2) the ability to tailor module outputs to specific market needs and 3) a relaxation on the need for highly conductive expensive TCO layers. The use of less conductive, and hence, more transparent TCO layers might also lead to increased power output. An additional advantage of the dot matrix technique is that it can be made to be self registering.

Electrode materials

Several alternative metals have been tested as possible candidates for M1 and M2 either as stand-alone electrodes or as thin-layer contacts to thicker electrodes, for example, as possible brazing solder layers. The PV performance of the cells using these metals varies, but results similar to the standard contact have been achieved. Figure 12 shows efficiency vs. time for a 700 hour light-soak test using four alternate contact metals. All cells were held at open-circuit conditions during the duration of the light-soaking. Comparing these results to Figure 21, one can see that three of the metals produce similar results to the standard process.

Figure 12. Efficiency vs. time for four alternate back contact metals which are compatible with dot matrix interconnection and high throughput manufacturing.

Estimates of the required thickness of the candidate alternative metals for use as M1 and M2 have been made based on the thickness of the standard electrode layers and on the values of the bulk resistivity of the individual alternate metals. The approximate resulting values of the thickness ranged from 7,000 Å to 110,000 Å. This implies that the alternate metals may need to be used in combination with metals of a higher bulk conductivity to minimize the required thickness. These combinations can be composed of alternative metals which can be deposited in the an environment similar to that used for semiconductor and Te layers deposition. Figure 13 shows plotted curves of up to 1700 hours of light soaking for cells using three different combinations; the fourth set of data is for cells using the standard SCI process. The data for the new metal combinations compare favorably with the standard cell.

The standard procedure calls for annealing of the cells following the metallization. In the case of the alternative metals, discoloration caused by oxidation is observable. In the dot matrix modules the M1 is contacted by an M2 layer in the M2/M1 vias and the presence of an oxide layer may cause an intolerable increase in the series resistance. A study was made of cells having an alternate metal for M1 that were annealed in air and in nitrogen. Initially the cells annealed in air had higher efficiency than those annealed in nitrogen. In 700 hours of light soaking the former decreased and the latter increased in efficiency to about the same value. Thus, the overall performance of the cells is not affected. However, the more important information needed is the determination of the contact resistivity of the M1/M2 interface for air annealed and nitrogen annealed pairs. Experiments to obtain these data are in progress.

Figure 13. Efficiency vs. time data for composite metal structure used for dot matrix interconnection.

Contact resistivity of M2/TCO contacts

In the dot matrix module the desired total area of the M2/TCO vias is less than about 1 % in order to maximize the usage of the cell area. Consequently, the current density in the vias is about 100 times that of

the current density of the cell at maximum power. In order to keep the power loss due to contact resistance below 1 % the contact resistivity must be less than about 0.004 Ohm.cm^2 for a 10 % efficient cell. At this level the contact resistance is difficult to measure. The accuracy of the method that we used to date for measuring contact resistance has been estimated to be about $\pm 0.05 \text{ Ohm.cm}^2$. We have developed an improved method of defining the geometry of the contacts that has an estimated accuracy of $\pm 0.01 \text{ Ohm.cm}^2$. This method involves only laser scribing as opposed to laser scribing, masking and etching. In this method parallel isolation lines are first laser- scribed through the metal and TCO layers. Then the metal is scribed down to the TCO in the perpendicular direction to define the length of the contacts and of the spaces between the contacts. The contact resistance of alternate and standard metal contacts were found to be 0.0099 and $0.0013 \pm 0.01 \text{ Ohm.cm}^2$. These two combinations appear to be satisfactory for the TCO/M2 contacts.

Solar Cells Inc. CdS/CdTe

Sample: 19519B4

Temperature $\sim 25 \text{ C}$
Aperture area = 63 cm^2

$$V_{oc} = 1.6 \text{ V}$$

$$I_{sc} = -575.1 \text{ mA}$$

$$J_{sc} = -18.5 \text{ mAcm}^{-2}$$

$$\text{Fill Factor} = 0.652$$

$$V_{max} = 1.2 \text{ V}$$

$$I_{max} = 0.510.0 \text{ mA}$$

$$P_{max} = 588.4 \text{ mW}$$

$$\text{Efficiency} = 9.28 \%$$

Figure 14. I-V data for highest efficiency dot matrix interconnected mini-module produced to date.

Fabrication of dot matrix devices using deposited M1 and M2 metals

Mini-modules with two cells connected in series, having a total active area of $\sim 63 \text{ cm}^2$ have been fabricated by using either grit-ablation or etching as a means of removing the component layers from the M2/TCO vias. The best aperture-area conversion efficiency obtained thus far with these devices was 9.3% (Figure 14) for the device made by grit-ablation and 8.4 % made by etching.

Fabrication of standard-size dot matrix modules (120 cm x 60 cm) consisting of 44 cells and having aperture area of 6620 cm^2 has also been accomplished. A module made using the grit-ablation process yielded efficiency of 4.5 % and one done by etching yielded a value of 4.2 %. In both cases considerable shunting was experienced in the M2/TCO vias following the M2 metallization. This problem has been partially alleviated by improved ablation of M1 and repairing the dielectric in the vias.

EFFICIENCY IMPROVEMENTS

Analysis has shown that increased photocurrent could substantially increase device efficiency. SCI supplied substrates before and after each deposition step to researchers at Colorado State University to permit the separation of photon losses in each layer for a standard device with thick (3,000 Å) CdS. The result is shown in Figure 15 (8). The figure clearly shows that the major current losses are due to absorption in glass and low collection of carriers from light absorbed in the CdS (wavelengths below 520 nm). Since there has been little success in improving the collection efficiency of the CdS, the improvement strategy has been to minimize the window absorption by thinning the CdS. While this approach has resulted in increased current densities, reduced open-circuit voltage has lead to only marginal efficiency improvements. However, similar to results found at the University of South Florida, the deposition of an intrinsic SnO_2 layer on top of the $\text{SnO}_2\text{:F}$ permits the use of thin CdS without loss in V_{oc} . The intrinsic SnO_2 layer may reduce the effectiveness of high spots on the TCO and pinholes in the CdS as shunt paths. Work performed at SCI which supports this hypothesis includes comparisons of devices made with thin CdS on low and high haze TCO. Older LOF TEC8 glass has a haze up to 10% whereas newer TEC8 and TEC15 products have considerably less haze, as reported by LOF (9). Haze is a measure of the diffuse white light scattering according to ASTM D 1003. The haze is a direct result of surface roughness of the TCO and high haze corresponds to higher roughness. Devices made on the low haze TEC8 substrates have produced substantially higher open-circuit voltages than older substrates when using similar processing. An example of this is the SCI record 1 cm^2 cells which were recently made on 3mm thick low haze LOF TEC8 glass. The CdS thickness of this sample was approximately 400 Å (also with an i- SnO_2 layer) yet it still produced an open-circuit voltage near 840 mV, which is close to the SCI record with thick CdS. The I-V curve measured at NREL for this record device is shown in Figure 16. In addition to the high V_{oc} , the short-circuit current density of 22.3 mA/cm^2 is as high as has been made previously on soda lime glass at SCI. The J_{sc} is higher than normal because of the reduced thickness of the CdS and glass. The quantum efficiency measured at NREL for an adjacent cell is shown in Figure 17. Comparison with Figure 15 shows that the response has increased in both the red and blue regions of the curve. The red response accounts for a 0.8 mA/cm^2 increase and is due to the thinner glass whereas the increased blue response accounts for a 2.7 mA/cm^2 increase and is due to the thinner CdS. The unknown loss of 1.2 mA/cm^2 reported in Figure 15 has been eliminated in this device. Using glass thinner than 3mm for full size modules (7200 cm^2) is not feasible because of mechanical strength requirements of installed modules. Therefore, reducing absorption loss in the glass can only be accomplished by lowering the Fe content in the glass. While uncoated low iron glass is commercially available, none is available with TCO coatings

comparable to LOF TEC8 or TEC15 coatings. If a TCO coated water-white glass was available, one could expect an additional 1.8 mA/cm^2 of current.

SCI L9504J1#52 CdTe cell

Loss currents in mA/cm^2

Calibration by Thermopile

J_{sc}	17.6
CdS bandgap loss	5.2
Deep penetr. loss	0.6
Reflection loss	1.6
Absorption loss _{glass}	2.6
Absorption loss _{SnO₂}	1.8
Unknown loss	1.2
Max. photocurrent	30.6

Photovoltaics Lab, CSU

Figure 15. Separation of current loss mechanisms for a standard device with thick CdS. (From Gunther Stollwerck's MS thesis from Colorado State University.)

Solar Cells Inc. CdS/CdTe

Sample: N2580#43

Sep 5, 1996 9:17 AM

ASTM E 892-87 Global

Temperature = 25.0°C

Area = 1.011 cm²

Irradiance: 1000.0 Wm⁻²

X-25 IV System

$V_{oc} = 0.8340$ V

$I_{sc} = 22.54$ mA

$J_{sc} = 22.31$ mAcm⁻²

Fill Factor = 69.73 %

$V_{max} = 0.6659$ V

$I_{max} = 19.69$ mA

$P_{max} = 13.11$ mW

Efficiency = 13.0 %

Figure 16. I-V curve for record 1 cm² SCI device. The device has an i-SnO₂ buffer layer on the TCO and a 400 Å CdS thickness.

Solar Cells Inc. CdS/CdTe

Sample: 2580-41

Temperature = 25.0°C

Sep 11, 1996 12:33 PM

Device Area = 1.013 cm²

Light bias = 13.0 mA
Bias Voltage = 0.00 V

Figure 17. Quantum efficiency from SCI's record 1 cm² device deposited on 3mm soda lime glass. Note the large increase in blue response and the slightly higher red response due to thinner CdS and glass respectively.

SCI's highest efficiency devices were made of 1 mm thick soda lime glass with a TCO deposited by Asahi Glass. The I-V curve for this device is shown in Figure 18. The diode parameters are similar to those for the cell described above. The V_{oc} is slightly higher and the current a little lower but the higher fill factor gives the cell the advantage and the slightly higher efficiency. Analysis of the quantum efficiency curve for this cell, shown in Figure 19, shows that the added current comes from the reduced glass thickness (the curve is flat out into the red) and an antireflection coating. The CdS thickness for this sample was approximately 1500Å. This is approximately the minimum thickness, on high haze TCO, that SCI has been successful using without an intrinsic SnO_2 layer and without a significant loss in V_{oc} . If the same CdS thickness was used on this cell as the cell in Figure 16, the J_{sc} would be 23.9 mA/cm². If all other parameters stayed constant, the efficiency would be approximately 14.5%.

Solar Cells Inc. CdS/CdTe

Sample: #1-3

Apr 30, 1996 4:06 PM

ASTM E 892-87 Global

Temperature = 25.9°C

Area = 0.2686 cm²

Irradiance: 1000.0 Wm⁻²

$V_{oc} = 0.8393$ V

$I_{sc} = 5.888$ mA

$J_{sc} = 21.92$ mAcm⁻²

Fill Factor = 72.38 %

$V_{max} = 0.6795$ V

$I_{max} = 5.263$ mA

$P_{max} = 3.576$ mW

Efficiency = 13.3 %

10 minute soak @ P_{max} , 4:50 cool.

Figure 18. I-V curve for record small area SCl device. The device was deposited on 1mm soda lime glass with TCO deposited by Asahi Glass.

Solar Cells Inc. CdS/CdTe

Sample: #1-3
Apr 26, 1996 8:22 AM

Temperature = 25.0°C
Device Area = 0.2686 cm²

Light bias = 2.00 mA
Bias Voltage = 0.00 V

Figure 19. Quantum efficiency from SCI's record small area device deposited on 1 mm soda lime glass. Note the relatively flat red response due to the thin substrate.

STABILITY

Many CdTe/CdS fabrication techniques are known. Some of these techniques result in devices with good stability. When observed, instability is usually attributed to the contact to p⁻-CdTe (10-12). While recent reports on CdTe module performance (13-16) have been encouraging, the data is limited and a more comprehensive testing methodology is needed. A complete description of the methods and results of this work has been previously reported (17). This section provides an update of the results from the first 2.5 years of these tests.

Photovoltaic module manufacturers must assure customers about the long-term power-delivery capability of their product. In the absence of extensive field history, methods of accelerated testing are needed. In addition, process development requires techniques to rapidly compare module stability differences resulting from process changes. Correlation of the results of accelerated tests and behavior in the field is complex but necessary.

Light soaking

The mainstay of the testing protocol, due to the similarity to field conditions, is continuous light soaking with resistive load. Furthermore, the majority of devices are biased near the maximum power point as they are under field conditions. Devices made with the standard process used in pilot production tested under resistive load are quite stable to greater than 20,000 hours of continuous light soaking at 0.8 sun illumination and 60 °C ambient, as shown by representative data in Figure 20. Devices held at short circuit conditions are also generally quite stable; however, devices held at open-circuit are less stable relative to the other bias conditions. We do not fully understand the mechanism responsible for the decreased stability at open circuit, but the effect appears to be rather general and consistently occurs for many, but not all, fabrication recipes. The exception is for devices with a Te IFL, as mentioned earlier. Figure 21 shows an example comparison of identical devices with and without a Te IFL and held at open-circuit under continuous illumination. The improvement with the Te is obvious. When held near the maximum power point, Te IFL devices perform as well as the standard device and tend to have a slightly better stability in the first several hundred hours of continuous light soak.

Figure 20. Efficiency of minimodules made with the standard process and subjected to continuous light soak while being held near the maximum power.

Discussion

Stable CdTe-based photovoltaic modules have been made with our standard pilot production process. The stability of modules made using a particular process can only be ensured with long-term testing. Simple indoor continuous light soaking conducted for >5000 hours is the minimal testing recommended. Without such testing, erroneous conclusions about the superiority of a particular fabrication recipe can be made. The recommendation applies to individual cells as well as to modules. Elevating temperatures beyond normal operating conditions by 20 to 35 °C in light soaking may be effective in accelerating degradation but can only be used for recipe comparisons at this time.

In the first phase of protocol development we have found that long term device behavior depends on bias in light soaking stress tests. Prediction of outdoor field operation based on indoor continuous light soaking tests at constant temperature is complicated due to several factors. First, sufficient field data has not been accumulated. Second, the inherent variation of illumination and temperature in the field may be important. For example, we have observed partial performance recovery of some degraded devices after several days of interrupted indoor light exposure. Thus a simple illumination dose equivalence between continuous indoor light soaking and intermittent light exposure in the field may not be valid.

Figure 21. Comparison of device performance between standard wet process and dry Te IFL when held at open-circuit under continuous illumination.

The next phase of development will include some extension and revision of the initial approach. First, while we understand some of the operating physical mechanisms, more analysis of device operation and physical changes is needed. Second, more detailed conclusions will require a larger number of samples for improved statistics, and thus concentration to fewer stress conditions is likely. Third, since some evidence of dark relaxation has been observed, an intermittent light soaking test will be added.

Outdoor array data

While all of the above described stability data for indoor tests are very important in device design and development, it alone is insufficient to predict module performance in the field. Additional information of actual field performance is required for two reasons. First, one must verify that the same phenomena is occurring in the indoor stress tests and outdoor operating conditions. For example, one must test that normal daily and seasonal temperature, humidity and illumination cycling do not induce additional degradation mechanisms not simulated in indoor tests. Second, one must use outdoor performance as a reference to determine any acceleration factor of indoor stress conditions.

SCI has detailed performance data on twenty-four months of outdoor exposure of our 1.2 kW array at our Westwood facility and twenty months of exposure of our 1kW array at NREL. Data includes current voltage data as well as illumination intensity and temperature data to permit the normalization of both intensity and temperature variations from standard reporting conditions. The data normalized for intensity

from the SCI Westwood array is shown in Figure 22. The periodic nature of the curve is due to the seasonal variation of the ambient temperature. The rated output of the array is 1200 W at 25 °C which agrees well with the average between summer and winter output. The back-of-the-module temperature on days with low wind is typically 20 °C above the ambient which results in operating temperatures during winter months of 0 - 20 °C and summertime temperatures of 50 - 60 °C. A linear regression on temperature vs. maximum power (illumination normalized) yields a temperature coefficient of -0.32%/°C which is large enough to give a noticeable apparent seasonal performance dependence. This is consistent with the range of temperature coefficients measured for small area devices under carefully controlled laboratory conditions. Data taken over an eight month period was used to maximize the temperature range. The temperature coefficient calculated from data taken during any one month agree within 5%.

Figure 22. Power output of SCI Westwood 1.2 kW array normalized for intensity variations but not for temperature fluctuations.

Figure 23 shows the array data with the normalized power corrected for temperature away from 25 °C and this normalized output agrees with the initial array rating. With the temperature correction, the data shows good stability for its 2 years of testing.

Figure 24 shows the average monthly power output (normalized for intensity but not temperature) over a twenty month span for the 1-kW array located at NREL. Again, stability appears to be excellent.

In addition to the array data discussed above, NREL has been testing individual modules under outdoor conditions for over 3 years. Figure 25 shows the performance of these modules over this time span indicating

Figure 23. Power output of SCI Westwood 1.2 kW array normalized for intensity variations and corrected for temperature variations from 25 °C.

Figure 24. Power output (normalized for intensity variations) of the SCI 1-KW array installed at NREL in June 1995.

SUMMARY

The research at SCI is focused on process and performance improvements that will result in high volume and low cost photovoltaic manufacturing. Significant progress on processing improvement has been made in the semiconductor deposition, chloride treatment, dry back contact processing, and interconnection. The deposition work has focused on developing vapor transport to allow for superior control of the semiconductor growth as well as continuous material feed. Devices made with material deposited with the new deposition apparatus appear to be similar to those deposited by the proven pilot production apparatus. The chloride treatment time has been reduced from 30 minutes to 5 minutes and shows some good device behavior with treatments as low as one minute. The chloride treatment has been carried out using HCl and CdCl₂ vapors as the source of chlorine. The back contact process has been improved with the use of a deposited Te interfacial layer to replace the standard wet etch. Device performance is similar to the SCI standard wet processed devices except they are more stable under continuous light soak under open-circuit conditions. Progress has also been made on an alternative interconnection technique, which can potentially increase the efficiency while allowing lower cost, more transparent TCO glass. Additionally, the interconnection can be self-registering. Minimodules with efficiency higher than 9% have been demonstrated utilizing this interconnect process.

Progress has also been made in performance improvements. The efficiency of small area devices (0.27 cm²) has been raised to 13.3% by using both thinner glass and CdS. The efficiency of 1-cm² devices has been raised to 13% by using an i-SnO₂ layer coupled with a 400 Å thick CdS layer on commercially available TCO on soda-lime glass. The stability of standard process mini-modules has now been demonstrated for over 20,000 hours of continuous light soaking while held near the maximum power point. The two years of data on SCI's 1.2 kW array show good stability to corroborate the indoor test data.

FUTURE PLANS

Emphasis in the coming year will be centered in four major areas:

- 1) Deposition - The newly developed continuous feed VTD process will be further refined and implemented into our manufacturing line. This VTD process will also be tested as a means of achieving an in-line dry semiconductor recrystallization via vapor CdCl₂. Additionally, if time permits, VTD will be evaluated as a means of depositing candidate IFL layers such as Te or ZnTe.
- 2) Efficiency Improvements - Emphasis will be placed on improving module efficiency. This will be achieved through thinning the CdS layer and improved control over processing, particularly semiconductor deposition. Since the VTD process allows for much greater control deposition parameters as well as film uniformity, this should narrow the gap between our cell and module efficiencies. For example, SCI can routinely produce 1-cm² cells in the 12 - 13% range. This translates to module efficiency in the 11% range.
- 3) Stability Verification - SCI will continue to carefully monitor its fields, arrays, modules and cells for performance verification. In addition SCI will take a leadership role in establishing an Accelerated Life Testing (ATF) procedure in conjunction with the NREL sponsored CdTe teaming program.
- 4) Cell Interconnects: SCI will continue development of its proprietary Dot Matrix process for providing cell interconnects. This concept will be compared laser line patterning on a cost/benefit basis.

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13. ABSTRACT (Maximum 200 words) Research at Solar Cells, Inc. (SCI) is focused on developing processes that will lead to high-volume and low-cost manufacturing of solar cells and will increase the performance of SCI's present technology. The process research has focused on developing vapor-transport deposition of the semiconductors, eliminating wet-chemistry steps while minimizing the chloride treatment time, forming a low-loss back contact using only dry processing, and creating an improved interconnection technique. The performance improvement work has focused on increasing the photocurrent by a combination of more-transparent glass substrates and a thinner CdS window layer deposited on an i-SnO ₂ buffer layer. SCI's record 13.0%, 1-cm ² devices have been fabricated using these techniques. Stability monitoring continues and shows minimal degradation for more than 20,000 hours of continuous light-soak at 0.8-sun illumination.					
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