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**Development of a Monolithic, Multi-MEMS Microsystem
on a Chip Demonstrating i MEMS™ VLSI Technology**

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Development of a Monolithic, Multi-MEMS Microsystem
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R&D Status Report Number 10
January 1, 1995 to March 31, 1995

Overview

This quarter saw the first silicon from the *i*MEMS® test chip, with complete circuits and beam structures. The wafers looked fine cosmetically and the circuits functioned as designed, but the beams suffered an anomaly that we have never seen before. Diagnostic work is under way to sort out the root cause, and other wafers are coming out this quarter to see if it was a one-time anomaly. Work on the process-development front has slowed because of the construction of a dedicated fabrication line for the last-generation process. With the current robust market place for ADI's business, our existing fabrication line has been operating at 100% capacity.

On the device front, great progress has been made by both Berkeley and ADI in the area of gyroscopes. Measurements of close to a degree per second or better have been made for gyros of all three axes and of both single- (linear) and double- (rotary) axis devices. In addition, ADI has designed a gyro that can be packaged in air that very well might meet some of the low-precision needs.

Accelerometers of several new formats have been designed and several have been implemented in silicon. First samples of the ADXL181 designed especially for the fuzing, safe and arming application have been assembled and are in characterization by ADI and others. In addition, 2-axis, Z-axis and digital output designs have been demonstrated. A 3-axis micro-watt accelerometer has been designed and is in fabrication. A 2-axis design for tilt applications is also nearing silicon realization. This portfolio of linear accelerometers, and even angular versions of the same provide, an arsenal of capability for specialized needs as they arise in both commercial and military applications.

Task IV. MEMS Process Technology

i MEMS™ Process Development at Analog Devices

The first lot processed through the full *i*MEMS process flow has shipped from wafer fab. Scribe-line test-chip data indicated properly processed CMOS and passive devices and good interconnect yield. The sensor-beam structures appear

to be fully released. However optical fringe counts indicate that the beams have severe curvature of more than $2\text{ }\mu\text{m}$. We have not yet tested any beam structures integrated with CMOS circuitry. There may be a problem with proper accelerometer operation due to the severe beam curvature present on this lot.

Beam curvature is caused by a large vertical stress gradient in the beam poly. The source of this stress gradient is currently unknown. Wafers that were released on another lot, after all high-temperature processing (i.e., over 900°C), produced beams with extremely flat beam poly. The additional thermal processing of the 900°C gate oxidation and 900°C BPSG flow cycle were expected to have minimal impact on beam curvature. The beam poly is encapsulated with over $4000\text{ }\text{\AA}$ of oxide before gate oxide and subsequent processing. We need to evaluate lots at intermediate stages between the beam module (before gate oxide) and final beam release at the end of the process flow to determine where the extra vertical stress gradient is being produced. Of course it is also possible that the observed curvature is an aberration resulting from some unusual processing which can occur on the first lot of a new process.

Over the next quarter we will try to obtain more test data on the first lot. However, the majority of our effort will be to support the ramp-up of a new MEMS production line at Analog Devices where we can also do process development work at a more rapid pace.

iMEMS™:

Multi-MEMS Microsystem on a Chip

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During the past three months, the Berkeley integrated MEMS design team was extremely productive, despite delays in completion of the BiMEMS-3 (TRP) run. Three papers from this project are to be presented at the 1996 Hilton Head Workshop [4]-[6]. Dr. Paul McWhorter of Sandia National Laboratories offered 9 die sites in their embedded polysilicon + 2 μm CMOS technology. This process approximates the capabilities of the ADI iMEMS™ technology and is an excellent proving ground for testing more aggressive sensor and circuit designs. This report summarizes the adaptations of the projects to the new integrated surface micromachining technology.

1.0 Task I: Accelerometers

1.1 Integrated 3-Axis Accelerometer

The goal of this project is to build and test a monolithic 3-axis accelerometer with sensitivity along the x-, y-, and z-axes with a single-layer surface micromachining technology. There are two separate designs on the first run of the Sandia National Laboratories integrated technology [1] (hereafter called SNL-MEMS): (i) individual x-, y-, and z-axis accelerometers fabricated in a single well and (ii) a single-proof mass xyz accelerometer. Both chips rely on sigma-delta control electronics and build on results from earlier BiMEMS designs [2]-[4].

In the tri-sensor design, the common centroid structure shown in Fig. 1 was used for the x- and y-axis sensors. A parallel-plate structure was used for the z-axis sensor, which is visible in the center of well, together with a matched rigid plate that enables a differential sensing scheme. The need for multiple sensors mandates a size reduction of the individual elements which in turns leads to a higher resonant frequency and consequently, reduced sensitivity. The performance penalty is minimized through the use of the improved fully differential position sense interface designed for lateral accelerometers [2].

FIGURE 1. SNL-MEMS layout of the sensing elements for the first design, consisting of three separate single axis accelerometers.

The layout for the sense element of the second chip is shown in Fig. 2. This sensor senses both the x- and y-axis directions using differential comb-fingers, similar to the x- and y-axis sensors used in the previous chip. Z-axis accelerations are sensed by using the sensor's main body, as a parallel-plate capacitor. A rigid reference plate with a matched capacitance (not shown) is included to allow a differential measurement.

The past three months have been spent on the following tasks:

- Adapting the sense element and the electronic designs to the SNL-MEMS process.
- Simulating and modifying the circuitry, to improve the noise performance, including a completely redesigned amplifier to acquire a larger signal in the sigma-delta loop.

1.2 Resonant Accelerometers

The basic goal of this subtask has been to explore the potential of resonant sensors in an integrated surface-micromachining technology. The initial step was to focus on a resonant force sensor, which has been designed and fabricated in BiMEMS and tested. The lessons learned are now to be applied to a push-pull resonant accelerometer.

The work of the last quarter has focussed on the development of a resonant accelerometer in the SNL-MEMS technology. A quarter-die layout is shown in Figure 2. The devices on this fabrication run are predicted to reach sensitivities of 100 Hz/g, with the possibility of a sub-milli-g noise floor. Much effort has gone into the improvement of the oscillation loop for maximum stability, resulting in a lower noise floor for the sensor. To what extent these efforts improve the stability cannot be determined until the devices are tested.

FIGURE 2. Layout of the sensing element, for the single proof mass, three-axis accelerometer for the SNL-MEMS multi-project chip run.

1.3 Angular Accelerometer

The past few months have been spent learning how to design in the SNL-MEMS. The Sandia process has several advantageous features for MEMS sensors. The ultra-flat structural polysilicon can be used to make large proof-masses that have essentially no warpage out to dimensions of 1 mm. The 2 μm CMOS electronics also permits large amounts of on-chip electronics on a single die. Furthermore, connections between the structures and circuits are made with polysilicon interconnect, rather than diffused runners, providing considerably less parasitic capacitance.

Figure 3 shows one quarter of the angular accelerometer design for the SNL-MEMS run. The new structure is square in shape to best utilize the area in the micromechanical well. Low strain-gradient polysilicon enables a large sensor size – 650 μm on an edge, with 84 capacitive sensing plates for a nominal sense capacitance of 142 fF per side. Additionally, the flexural suspension can be placed on the inside of the structure, which is a more advan-

tageous arrangement than the outside suspensions previously needed to suppress out-of-plane warpage.

FIGURE 3. One quarter of the SNL-MEMS angular accelerometer design.

In the upcoming months, the main focus of the angular accelerometer project will be characterization of new devices. Testing of the reworked, open-loop sensors from the BiMEMS-2 run will begin immediately along with characterization of the sigma-delta angular accelerometers fabricated on the BiMEMS-3 run at ADI.

The larger diameter, open-loop angular accelerometer in the Q14 slot of the BiMEMS2 run contained a design flaw. Certain etch holes were spaced too far apart, and, as a result, the structure did not release. When a second batch of BiMEMS2 wafers was fabricated, one wafer was over-etched for 30 minutes in order to remove the extra oxide. That wafer has been diced, and the chips packaged. After probing the Q14 devices, it is apparent that the structures are now released. Up until this point, all angular accelerometers have used the XL50 force-balance circuits, which are a limiting factor in the sensor sensitivity. Testing of these open loop sensors will begin imminently, providing new data on the minimum detectable signal that can be achieved with surface micromachined angular accelerometers of this type.

Analog Devices has finished fabricating the third generation, closed-loop angular accelerometer design with a sigma-delta force-balance system. Packaged devices have just arrived, and testing and characterization will also begin shortly.

2.0 Task II: Gyroscopes

2.1 X- and Y-axis Vibratory Rate Gyro

The final stages of testing the dual input axis rate gyro fabricated by Analog Devices Inc. were undertaken over the past three months. The experimental work focused on electrostatic tuning of natural frequencies to improve sensitivity. Matching natural frequencies improved performance from 1 °/second *without* tuning to 10 °/minute *with* tuning, in a 25 Hz bandwidth. The rate gyro is nearly able to resolve the rotational rate of a the minute hand on a clock! As the open-loop design modeling and experimental verification for the dual input axis rate gyro draws to a close, attention has turned to publishing the research results [5] and using the research results to design a gyro with higher performance. Specifically, a gyro design submitted to SNL-MEMS is projected to have consistent performance of 6 °/minute. This gyro is part of a multi-sensor block including a z-axis gyro and an x, y, & z axis linear accelerometer, thereby implementing full three degree of freedom inertial measurement unit. The preliminary system level design work for closed-loop control has also been pursued. Closed-loop control and possibly automatic natural frequency tuning should greatly enhance offset and scale factor stability while also reducing the minimum detectable signal.

FIGURE 4. The mask layout for the next generation SNL-MEMS gyro design.

Figure 4 is a mask layout for the new gyro design., which uses a larger diameter, internal suspension, internal comb drive, and a structural polysilicon busses to boost sensitivity and decrease noise. The goal is to achieve consistent 6 °/minute minimum detectable signal in a 25 Hz bandwidth without excessive offset and scale factor drift.

2.2 Z-axis Vibratory Rate Gyro

The Z-axis rate gyroscope has been thoroughly tested over the past three months and will be reported in an upcoming paper [6]. Frequency tuning of the sense mode, with little effect on other modes of the structure, has been demonstrated. In addition, the scheme for cancellation of the quadrature error has worked according to design.

The SNL-MEMS z-axis chip incorporates enhancements on the basic design demonstrated in BiMEMS. The new sense element maintains the driven mode resonant frequency at 20 kHz, but increases the proof mass to 0.3 μ grams. The on-chip CMOS electronics operates synchronously with the oscillating sense element. Electrostatic feedback is implemented to actively cancel quadrature errors and to control the output deflection.

An angular accelerometer for in-plane signals is also incorporated into a chip on the SNL-MEMS run. The optimized suspension achieves a factor of four separation between the z-axis and torsional (sense mode) resonant frequencies, with the latter being about 5 kHz.

3.0 Task III: Microresonators

During the past quarter, this task involved process development in the UC Berkeley Micro-lab, as well as participation on the SNL-MEMS run. Figure 5 shows the basic narrow-gap, double-ended tuning fork (DETF) microresonator. The motional resistance varies with the fourth power of the gap in Fig. 5, which has motivated shrinking it below the lithographic limit.

Initial attempts to fabricate the microresonator have been completed, using the process outlined in the 1995 annual report. The goal was to investigate the methods of achieving narrow gaps and the suitability of CVD silicon-dioxide deposition and thermal oxidation for spacer definition. Cross sectional SEMs of test structures are shown in Fig. 6(a) and (b). To minimize the gap, we use a second polysilicon for the DETF tine definition. The structure will be further planarized using chem-mechanical polishing.

The second task was a microresonator design for fabrication in the SNL-MEMS multi-project chip run. The goal is to explore the issues of drive and sense schemes and the resonator topology for high-frequencies. DETFs covering the range 10, 20, 30 and 40 MHz. have been designed. The main operating circuit is the trans-impedance amplifier. Figure 3. shows a portion of the design layout.

FIGURE 5. The mask layout for narrow-gap double-ended tuning fork resonators.

4.0 IC and System Design

This task is merged into application-specific sense and control circuit design for the linear and angular accelerometers, the resonant accelerometer, and the vibratory rate gyroscopes.

The accelerometer design team (M. Lemkin, M. Ortiz, and N. Wongkomet) is implementing sigma-delta control strategies in CMOS for achieving minimum electronic noise. Recently, approaches to cancel errors due to charge injection have been developed that will be tested on the SNL-MEMS run.

Both the resonant accelerometer and the two rate gyroscopes currently use analog signal processing. In the future, re-thinking these integrated sensors to better exploit the digital CMOS technology will be needed.

FIGURE 6. (a) Cross section of the sidewall-spacer gap in a test structure.

FIGURE 6. (b) close-up of (a).

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