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Design and Characterization of Microscale Heater Structures for Test Die and Sensor Applications

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(Abstract)

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We describe a class of microscale heaters fabricated with CMOS processes on silicon wafers. These heaters were designed to produce localized high temperatures above 400°C for test and sensor applications. The temperature levels produced for various input powers and the thermal profiles surrounding the heater for packaged and wafer-level heater structures were studied to guide the placement of microelectronics integrated with the heater structures on the same die. To show the performance of the design, we present resistance sensor measurements, IR temperature profiles, and results from a 3D thermal model of the die. This effort demonstrates that it is possible to successfully operate both a microscale heater and microcircuits on the same die.

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Introduction

In contrast with traditional microelectronic thermal efforts designed to reduce chip operating temperatures, this work exploits the use of deliberately elevated temperatures. Microscale heaters integrated with circuitry on a silicon die are useful for test die, sensors, and other special applications. By reducing the size of the area heated, and by using reasonable judgement in distancing circuitry from the heater on the die, we can generate temperatures above 400°C with modest power levels while avoiding the overheating of microelectronics used to drive a test or sensor application. These integrated heater and microelectronic structures are useful for accelerated aging studies of electromigration, diffusion, and oxidation. The heaters may find additional use in sensors and for "chemlab on a chip" applications. We used high-resolution infrared imaging of heater structures on Sandia SHIELD[®] test die[1] to characterize the degree of temperature uniformity over 50- by 950-μm polysilicon/polysilicide heaters supported by a field oxide layer on a silicon wafer. The thermal performance of die containing these heaters in both packaged form and in wafer-level tests was studied. Temperatures over the heated section were diagnosed three ways: 1) with measurements of resistance on an aluminum alloy metallization trace deposited over the heater, 2) with high spatial resolution infrared measurements, and 3) with model calculations based on a detailed analysis of the geometry and properties of the device materials. The result of this effort is a determination of temperature ranges available for specific power inputs, and a description of the temperature distribution on and near the heater structure.

At issue are the temperature range and the uniformity of temperature achievable on a test structure in a wafer-level application. Temperatures ranging from perhaps 200°C to as high as 350 to 450°C are needed for electromigration studies and other wafer-level thermal tests. Localized heating on the test chip must not heat adjacent electronics on the wafer to the point where their testing function is impaired, typically near 120°C. It is also important that the temperature be nearly constant over the test region with its electromigration test strip and resistance temperature sensor. Finally, a resistance temperature sensor in the test structure must be capable of making reliable measurements over the intended temperature range. The 3D thermal model allows us to describe temperature distributions in a cross section through the heater and substrate. Effects on the temperature profiles due to varying the oxide layer thickness and heater power

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are studied. We use the model, which describes temperature gradients along the length of the heater structure, to design a heater power input that varies spatially along the length in order to flatten the temperature gradients. We also describe tests in which the test structures are not packaged at all, but are tested in full-wafer form on a conventional vacuum chuck. The excellent thermal spreading in the silicon wafers allows us to do useful tests at powers of 7.5 watts to achieve heater surface temperatures in the range of 300°C.

In this paper we begin by describing the wafer-level testing setup and the geometry of the test structure. We then summarize results from the IR thermal tests, primarily the wafer-level tests. We describe the 3D finite-difference thermal model and compare the IR measurements with the model calculations.

Geometry of the Test Structure

The basic die tested in this work is a cluster of test structures, each of which contains a heater, a metal trace used as a temperature sensor, a metal trace serving as the device under test, and application circuitry not used in the present work. An overview of a test structure is shown in Figure 1. The microscale heater is

Figure 1. Heater layout configuration for the test structure. The heater is 950 μm in length and 50 μm in width. The squares are wire-bond pads 100 μm on a side and spaced by 100 μm . The heater is centered between the bond pads. The temperature sensor and DUT are approximately 800 μm in length.

used to effect elevated temperature conditions on the test strip. The thermal performance of the test structure is determined by the details of the heater geometry as well as by the package into which the die

Figure 2. Focused ion beam photo through a cross section of the heater oxide and test strips of one device. The resistive heating is due to electrical conduction in the platinum silicide and, to a lesser extent, in the polysilicon layers. The underlying $0.7\text{-}\mu\text{m}$ silicon oxide layer has a significant thermal resistance to heat conduction into the silicon substrate.

is mounted. Figure 2 shows a cross section of the test structure taken through the heater. This photo enables us to measure the layer thicknesses important to heat transfer within the die. The temperature sensor and electromigration test strips, which are supported on a sequence of oxide layers, are overlaid by silicon nitride and p-glass passivation layers. Since the heat flux is very low in the layers above the heater, those overlays play a negligible role in determining the local temperatures. Potential self-heating of the temperature sensor and test strip are not addressed in this work.

For measurements on packaged die, the test structures are diced from the silicon wafer so that a structure such as that shown in Figure 1 is located near the middle of a die cut from the wafer. We carried out measurements with die cut to dimensions of 6 mm by 3 to 3.2 mm. This size is significant because it offers a large area for bonding the die to the copper-tungsten or Kovar packages, and a correspondingly low thermal resistance.

The temperature sensor strip determines the average temperature of the heater area by using a measurement of the sensor resistance and interpreting its value with a temperature calibration. If the temperature is uniform along the length of the sensor, this can be done by a straightforward calibration of the sensor in an oven. A calibration curve for several of the test parts was determined in this way and is shown in Figure 3. At temperatures above 325°C some change in the sensor was found. This change is related to alloy solid solution and annealing of the aluminum-copper alloy in the sensor.[2]

The temperature sensors are annealed by heating to a temperature of 300°C for about 40 minutes. The activation energy associated with this annealing process was measured to be approximately 0.68 eV. When heated above 325°C the copper goes into solution while the sensor still measures following the calibration of Figure 3, but on cooling potentially reverts to the unannealed state. If cooled rapidly, it remains in the unannealed state. Thus, cycles of increasing and decreasing temperature measurements that are unaffected by time require that the sensor be annealed, and that all measurements be carried out below 325°C .

Once annealed, the sensor appears to give repeatable results in the range up to about 400°C. A change in resistance of about 2 ohms, corresponding to nearly 20°C, occurs during the annealing process. Figure 3 shows the calibration for one of the test die over the range up to nearly 400°C. The squares on the calibration curve show measurements made independently on the IR system temperature stage. The

Figure 3. Resistance versus temperature calibration for test die (solid curve). Also shown with solid squares are data from a calibration taken independently with the temperature stage on the IR system.

calibration coefficient from the full calibration is 0.1338 ohms/°C below 325°C and 0.158 ohms/°C above 325°C. A low-temperature data set from an independent calibration on the IR system thermal stage gave the slope 0.1296 ohms/°C. Thus an estimate of temperatures near 325°C derived from only the low-temperature calibration would be in error by about 1.3°C, exclusive of any annealing effects.

Another concern in monitoring the die temperature with this resistance during heater-driven testing is the fact that the temperature is not constant along the length of the temperature sensor when the heater strip is used as the heat source. Thermal simulation calculations (discussed later in this paper) for the temperature profile along the length of the sensor are used to correct for the temperature variation.

Microscale Heater Temperature Measurements

Infrared images of the heated die or wafer area were acquired using a Barnes InfraScope system[3] to determine surface temperature profiles near operating heater structures. Tests were conducted on die cut from a wafer and mounted in either copper-tungsten or Kovar packages. Additional measurements were made with test structures in full-wafer form. This paper concentrates on the full-wafer tests.

The standard InfraScope system was modified to include a vacuum chuck to hold down and thermally attach the wafer to the thermal stage of the IR system. Precision positioning and rotation of the wafer in the IR system field of view were provided. A probe table was fabricated to allow a series of up to eight individual probe contacts to be positioned and lowered onto the appropriate 100- by 100-μm contact pads of the test structure on the wafer. Two probes supplied current to the heater assembly. Independent heater

voltage measurement contacts were made to these probe tips to accurately measure the voltage applied to the wafer and allow us to determine the heater power delivered in each test. The resistance temperature sensor on the wafer was monitored with four probes to give the sensor resistance independent of the probe contact resistance. The wafer was thermally attached to the temperature-controlled stage by drawing the wafer against the aluminum vacuum chuck. The wafer and chuck surfaces were cleaned with a solvent, but no special treatment of the surfaces was used and no interface material was placed between the surfaces. The stage controlled the wafer temperature during the emissivity calibration and the powered temperature measurement. Views of the system as modified for wafer-level testing are shown in Figure 4. An overview of the test system (left) shows the table surface added to hold the probe contact arms. The opposing view shows a wafer mounted on the vacuum chuck, with the probe contact arms positioned over the wafer surface.

Figure 4. InfraScope system, as modified for full-wafer measurements. System overview (left). Close-up view (right) of a 150-mm diameter wafer on the vacuum chuck, with probes for the electrical contacts.

In general, we found that the testing works well at wafer level with heaters operating at high temperature. Limited thermal conductivity between the wafer and vacuum chuck is more than overcome by the large contact area of the full wafer interface with the thermal stage. These tests demonstrate the feasibility of delivering a relatively high heater current through probe tip contacts to the wafer without significantly disturbing the temperature profile near the heaters.

Results of Wafer-Level Tests

Measurements of temperatures on the wafer near a heated test structure were made using the vacuum chuck to secure a full wafer for test. The temperature profiles near the heater are similar to those observed in the tests with packaged die.[4] The temperatures in the region a few hundred microns from the heater are determined largely by thermal resistance through the interface between the wafer and vacuum chuck. Although the interface resistance per unit area is much higher than that for the die attach of a packaged part, the large surface area of this interface leads to good thermal conduction between the wafer and temperature-controlled chuck.

Measurements of temperature distributions on the wafer were made at two different levels of magnification. The low-magnification (1X) test gave the temperature distribution over a larger region on the wafer that is sensitive to the thermal resistance between the silicon wafer and the aluminum vacuum chuck holding the test part. The higher-magnification (5X) test gave additional resolution in the temperature near the heater. Uncertainty in the wafer surface emissivity at high temperatures, however,

limits the accuracy of higher temperature values determined from the IR signals. In the hottest region near the heater we must rely on the resistance sensor to give a better measure of temperature. Since the minimum detectable temperature difference is a strong function of the surface temperature, the thermal stage holding the wafer was raised to 80°C for this test to give adequate resolution for wafer temperature measurements well away from the heater. Figure 5 shows the two temperature maps from these tests with 7.4 watts power input to the heater strip.

Some variation in the temperature background can be seen in these images. This variation is due to limitations of the IR measurement method. Thermal expansion in the 10.2-cm-wide thermal stage used for these tests causes a wafer displacement of a few micrometers as the stage temperature is changed during the emissivity calibration process. This means that the emissivity map is displaced relative to the actual wafer position recorded during the thermal-image acquisition. Regions of the surface where the emissivity changes rapidly with position (such as at the edge of bond pads) are most strongly affected. The resulting emissivity errors give the appearance of temperature variations with position. Regions in which the emissivity is relatively constant produce the most reliable measurements.

Figure 5. Temperature maps of wafer surface with 7.4 watts power input to heater. The top image was made with 1X magnification optics, and the bottom with 5X optics. The size scale for each image is shown in millimeters.

The surface region over the heater strip has an emissivity of about 0.33 when measured in the temperature range of 80 to 90°C. Accuracy of the temperature measurement improves for surfaces having values close to 1. In traditional IR work the surface is generally coated to increase emissivity. In this work, however, the die surface cannot be coated easily because of the small scale of the features. Instead, we used the low emissivity values measured for each pixel in the image to determine temperature. We assume this emissivity is temperature-independent, often a reasonable assumption. However, comparisons with information from the resistance sensor and the thermal simulation model suggest that the emissivity of the wafer surface over the heater falls with increasing temperature. The surface of this die is complex because silicon is partially transparent in the infrared. However, the silicon is overlaid by oxide, metal, and silicon nitride layers. In particular, the metal is more opaque in this range. The sensitivity of the measurement to emissivity also increases at higher temperatures due to the long wavelength (2 to 5 μm) of the infrared system being used. This fact severely limits temperature measurement accuracy above 200°C. The IR results are most accurate at lower temperatures, but still useful for determining relative temperature profiles at higher temperatures.

Thermal Simulation of Wafer-Level Tests

A model simulating the test structure heater on an extended layer of silicon was developed to complement the thermal testing. Rather than model the entire wafer, we elected to model only the area of interest -- a section 2 cm by 2 cm in size that represents the heated area of the wafer. Including the unheated regions of the wafer would have only added unnecessary, time-consuming calculations. The heater geometry from a test structure is positioned at the center of the modeled silicon wafer section. A thin silicon dioxide layer supports the heater on the silicon wafer. The wafer is assumed to be in contact with a constant temperature heat sink through a thermal resistance representing the interface between the wafer and the vacuum chuck on the test system. The thermal resistance per area is assumed to be a constant value over the interface area.

Figure 6. The 2- by 2-cm mesh that represents the heated area of the wafer (left). A layer with a uniform thermal resistance per area conducting to a constant heat sink temperature is at the back surface of the wafer section. A magnified view of the center area (right) shows the 25-by 50-micron elements in the heater region. Both the green and magenta regions represent silicon material. The oxide and heater regions can be seen in the center of the magenta region.

The magnified view shows the 50- μm by 950- μm heater area in red, attached to the silicon wafer through a layer of elements representing the silicon dioxide. The silicon mesh under the heated region is a series of 25- by 25- by 50- μm rectangular elements. The mesh is graded to larger size at a distance from the heater where small temperature gradients exist. Distributed over the surface of the heater nodes are surface heat

inputs set to match a given total power to the electrical heater. The solution of this model and display of the calculated results is done using a 3D thermal analysis solver.[5] This solver is based on a finite-difference solution method. The speed of this technique is sufficiently fast that there is no need to assume symmetry to the model.

The thermal properties input to the model are taken from several sources. The thermal conductivity for silicon is from standard handbook references.[6] Following are the values used in the simulation:

Table 1. Silicon Thermal Conductivity

Temperature °C	Thermal Conductivity (W/cm-°C)
-253	12.552
-195	6.276
-110	2.929
0	1.381
100	0.962
300	0.556
500	0.397
727	0.3138
900	0.293

The wide range of silicon temperatures occurring in this problem and the strong temperature dependence of the conductivity require that the temperature dependence of the silicon thermal conductivity be included in the simulation. The tabular conductivity values from Table 1 are interpolated for the temperature at each point in the mesh during the calculations. The temperature dependence significantly affects both the shape of the high-temperature spatial profiles and the temperature levels predicted for a given power input.

A value of thermal conductivity for the silicon dioxide layer of 0.0147 W/cm-°C was used in the simulation and is based on the work of Kleiner.[7] A thermal resistance for the interface between the silicon wafer and vacuum chuck is derived from the test data. The thermal resistance is extracted by comparing the surface temperature profiles measured by the IR system to the corresponding calculated temperatures. This resistance value is adjusted until a satisfactory match is found between temperature profiles for the surface well away from the heater. The power input to the heater is measured during testing, and the same value is used as input for the simulation of the test. Figure 7 shows the calculated temperature profiles on a small area of the wafer surface, and also on a cross section through the heater and the silicon under the heater strip. Some roughness in the thermal contours is evident in the coarse mesh region. These are due to approximations in interpolating the mesh temperatures during post processing, particularly where mesh-size transitions occur.

Figure 7. Temperature profiles for the top of the wafer (upper plot) and for a cross section through the length of the heater strip and normal to the surface (lower plot). The cross section shows the temperature distribution through the silicon wafer below the heater strip. The heater length in these plots is $950\text{ }\mu\text{m}$, and the power input is 7.4 watts.

We simplify the model by omitting the detail of the test structure located above the heater (see Figure 2). The presence of this detail does not affect the temperature distribution; the heat flux in that region is essentially zero compared with the flux below the heater. Self-heating effects due to current flowing in the electromigration strip and temperature sensor strip are not considered. Nor do we include the effects of thermal radiation and convection. They produce heat fluxes above the heater that are more than six orders of magnitude smaller than the conductive fluxes below the heater, and thus are negligible in determining the wafer temperatures near the heater.

Figure 8 provides a comparison of temperature traces from the thermal simulation and from the IR measurements. The figure shows temperatures on the wafer surface for points on a line that bisects the heater strip along its length. Thermal conditions are a 7.4-watt heat input and a sustained stage temperature of 80°C . A value for the thermal resistance per unit area of the interface between the silicon and aluminum vacuum chuck of $2\text{ W/cm}^2\text{-}^{\circ}\text{C}$ was used for the thermal simulation shown in Figure 8. This value was selected by matching the IR temperature profile near the heater to that of the calculation; the model resistance is varied to match the temperature profile. The constant temperature boundary under the wafer section is set to the thermal stage temperature used during the IR measurements.

In contrast to the thermal resistance of the vacuum chuck interface, the tests of packaged part showed higher conductance values.[4] Typical Au-Si eutectic die attach resistances were roughly $44\text{ W/cm}^2\text{-}^{\circ}\text{C}$, while package attach resistances to the thermal chuck (made with a Dow Corning #340 thermal compound

layer) were found to be $1.4 \text{ W/cm}^2\text{-}^\circ\text{C}$ in the model over an effective conducting area of one square centimeter.

Temperature profiles from the IR images can be extracted numerically from the image files to give a basis for comparison of the data. Figure 8 shows the surface temperature profile extracted from the 1X and 5X images for a row of pixels across the field of view at a position that matches the heater strip center line. The 5X trace position was overlaid on the 1X trace. Thus, low-resolution data is shown for the full die width and higher-resolution data for the heater strip region in the figure. Some variation in the temperature profile at the ends of the heater is due to shadowing in the field of view by the electrical probes.

Figure 8. Comparison of surface temperatures along a line bisecting the heater strip. The dotted curve shows the raw IR data for temperature-independent emissivity. The solid curve shows the same IR data corrected assuming a lower emissivity at high temperature.

For the highest temperatures (near the center of the heater) the simulation results match more reasonably to temperatures from the resistance sensor than to the IR data. The calibration data from Figure 3, taken together with the sensor resistance during these tests, predicts an average temperature along the sensor of 312°C . This temperature comes from measured resistances of 45.9 ohms at 80°C with zero heater power and 77.1 ohms with the heater under power. The calibration coefficient of $0.1338 \text{ ohms/}^\circ\text{C}$ was used. Remaining differences between this sensor temperature and the peak model temperatures are well within a range explainable by uncertainty in the thermal resistance of the oxide layer supporting the heater strip in the model.

In determining temperature with the IR system, we measured emissivity over the interval from 80 to 90°C in this test. The IR system assumes this emissivity value applies at the higher temperatures as well. The long-wavelength (2 to $5 \mu\text{m}$) response band of the detector in the InfraScope results in a strong dependence of the temperature on the emissivity assumed at higher temperatures. To show the sensitivity, a "corrected" curve (solid curve) is plotted also in this figure. The corrected IR data assumes a linear variation of emissivity from the measured value of 0.33 at 90°C to a selected value of 0.17 at 350°C . The high-

temperature value was selected to better match the simulation and resistance sensor temperatures. Due to equipment limitations emissivity could not be measured above 120 °C, but the values assumed at higher temperature produce results that match to the high-temperature sensor and simulation data. This correction illustrates the sensitivity of temperatures to the emissivity, but remains to be confirmed with high-temperature emissivity data. Until such confirmation, the high-temperature thermal profiles should be used only for relative comparisons.

Once a thermal simulation model is developed for a test structure design, the model can be applied to useful variations of the test structure. Limited space in this paper precludes our including all of the variations calculated. Instead, we point out selected areas in which such calculations may be useful. For example, it is straightforward to calculate a sequence of temperature profiles for a range of heater power levels. Simulations can be used to determine the effect on thermal profiles of varying the wafer chuck temperature. In Figure 9 we show a detailed temperature map of the heater surface for a particular heater design.

Figure 9. Temperature map for the top of a 950- by 50- μ m heater strip of a test structure on a wafer. The heat input of 7.4 watts is distributed evenly over the strip surface.

The temperature varies strongly along the heater due to the simple uniform power at all points along its length. Note the variation in temperature across the width of the heater as well as along its length. It is desirable to have the temperature as uniform as possible in the test strip region and along the length of the temperature sensor. Such uniform conditions simplify using oven-type resistance calibration data to interpret temperatures from the resistance sensor. Hence, another application of the thermal simulation is to design a power input profile along the heater length to flatten the temperature profiles. We have done this with several heater geometries. The power profile can be built into a heater by sculpting or slightly changing the heater width to adjust the resistance profile locally along its length. The sculpted heater profiles from the simulation analysis should greatly improve temperature uniformity of the heater centerline for future designs of heated test structures.

Finally, the simulations can be used to explore the sensitivity of the heater temperature to various features of the design. We have found, for example, that the thickness of the oxide supporting the heater, with its relatively low thermal conductivity, affects the power input needed to reach a given temperature. Simulations predicting the performance for various new heater design can be performed. Indeed, such simulations can be used to develop a full range of design rules for heated structures.

Discussion

The measurements and simulations show the feasibility of wafer-level testing with test structures that use on-chip heater designs. The design tools based on the IR measurements and thermal calculations presented here offer a means for improved development of heated test structures for future test applications. The thermal simulation tools are effective in describing the temperature variation near heated structures on a silicon wafer. Infrared measurements available to us at this time are primarily helpful in evaluating thermal resistances in test configurations and in measuring relative thermal profiles.

One can use the simulation to design a heat input profile along the length of the heater that will flatten the temperature profile, thus reducing temperature gradient problems. The variation of power along the heater can be implemented with a sculpted width profile for the heater design.

Following is a summary of the main findings in this work:

1. **Useful temperature range of the structure in wafer-level testing:** We tested the design above 300°C and expect the heater to perform with little degradation at temperatures above 400°C.
2. **Power required to heat the structure:** We find a temperature rise of 30.3°C per watt of heater power input in this design.
3. **Temperature variation along the test strip** was similar to the variation found in the packaged test parts. For a temperature rise of 225°C, temperature variation along the full length of the heater is ~100°C; over the center temperature sensor section (800 micron long), the variation is ~30°C.
4. If **control circuitry** is located on the heater centerline, with 200-micron spacing from the end of the heater, the circuitry experiences a 35°C rise for a heater peak temperature rise of 225°C above the heat sink temperature in this design.
5. **Significant accuracy limits** exist for aluminum alloy resistance-temperature sensors above 325°C, where the readings may vary with time due to annealing effects. An improved sensor design may increase the accuracy of these measurements.
6. There is a **modest sensitivity** of the heater temperature on the resistance between thermal chuck and wafer thermal resistance. If the thermal resistance is cut in half, the peak heater temperature is reduced by 4.4%, and the temperature at the end of the heater is reduced by 6%.

This study produced design changes to accomplish the following:

- Lower the temperatures of on-chip electronics to improve the integrity of high-frequency signals for electromigration testing.
- Dramatically reduce unwanted temperature gradients along the EM test structures.
- Assist in developing a more accurate on-chip thermometer for the EM test strip.
- Produce the first set of design rules for the thermal layout of test structures comprising microscale heaters integrated with microelectronics on the same die.

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References

- [1] D. G. Pierce, E. S. Snyder, S. E. Swanson, and L. W. Irwin, "Wafer-Level Pulsed-DC Electromigration Response at Very High Frequencies," Proc. IEEE 1994 International Reliability Physics Symposium, p. 198, April 1994.
- [2] D. R. Frear, J. E. Sanchez, A. D. Romig, Jr., and J. W. Morris, Jr., "The Evolution of Microstructure in Al-2 Pct Cu Thin Films: Precipitation, Dissolution, and Reprecipitation," Metallurgical Transactions A, p. 2449, September 1990.
- [3] InfraScope, EDO Barnes Engineering Division, 88 Long Hill Cross Roads, P.O. Box 867, Shelton CN 06484-0867.
- [4] D. A. Benson, Letter Report 1333/2-19-97 to D. J. Bowman, "Thermal Characterization of a Packaged Electromigration Test Die," Sandia National Laboratories, Feb. 19, 1997.
- [5] PC3D, Harvard Thermal, P.O. Box 508, Harvard, MA 01451.
- [6] Y. S. Touloukian, *Thermophysical Properties of Matter*, Vol. 2, IFI/Plenum, New York, 1967.
- [7] M. B. Kleiner, "Thermal Conductivity Measurements of Thin Silicon Dioxide Films in Integrated Circuits," IEEE Transactions on Electron Devices, Vol. 43, 9, p.1602, September 1996.

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