DOE/EE/15656--T1

Interim Report
Aug-October, 1997

NIST Energy Related Inventions
Electronic Starter Device for Fluorescent Lamps

MASTER

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ERIP # 656

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Applicant: Beacon Light Products, Inc. Ron Porter

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Statement of work efforts completed to date:

From the Scope of Work document which accompanied the original proposal, three silicon devices were anticipated for development, simulation, and quality assurance fabrication. The status of these are in the same format as the Scope of Work...Attachment -A-:

Task 1 Design and Simulation:

03/03 Triac simulation

Arizona State University was contracted out to provide numerical simulations of differing design approaches for the power semiconductors. The work was performed by Dr. Schroeder and a graduate student, Mr. David Kohnke. These efforts were assisted by Dr. Lowell Clark, of IEEE Consulting. From these simulations based on the device physics, we learned that by varying the diameter and spacing of emitter shorting structures, that the desirable power device turn off characteristics could be achieved. This is crucial in order to generate adequate voltage to ignite the lamp. Also studied was the gate turn on sensitivities to processing and design parameters. It is important to minimize the device turn-on power, in order that the device consume minimal power. This greatly simplifies the circuit complexities, and will allow us to significantly reduce component count. Through subsequent, although project unrelated, receipt of materials from three different semiconductor firms, it was determined that small specialty houses do not possess the quality control necessary to hold the design tolerances. These firms were Teccor, Hutson, and Phoenix Semiconductor. From previous, though unrelated projects, we know firms such as Motorola and SGS-Thompson are capable of maintaining high quality levels. Please see the section on 03/04 Triac development.

02/03 Triac development:

The development of unique thyristors as anticipated in the Original Scope of Work outline has changed for this portion of the project. Two parts, the 02 and the 03, are now combined into a single structure. A commercially available power semiconductor device has been identified and qualified as suitable for this application. The part is manufactured by SGS Thompson (France), and is designated the TN22. Significant effort has been involved in the characterization and qualification by Mr. Rudy Hausdorf, a Beacon test engineer, and Mr. Richard Nelson. As a result of the availability of this device, significant design and ASIC architectural changes had to be implemented to properly interface with this device. This activity was led by Mr. Tyler Lowrey, a Beacon development engineer. Although this resulted in increased design activity per the ASIC schedule above, it is felt that the overall design will more completely meet it's intended goals as a result. We consider this phase complete, with the exception of working with SGS engineers and management to reduce the cost of this component by providing it in die form, vs. as a packaged component. Mr. Lowrey is working on this issue.

ASIC Simulation and Design

Central to the operation of the starter device, the Application Specific Integrated Device(ASIC) had to be cost reduced and optimized for this application. Prior ASIC technologies which were in production at Beacon Light was a 2.0 micron mixed signal technology produced at American Micro Systems (AMI),

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whose principal fabrication location is Pocatello, Idaho. As is the case with mainstream semiconductor suppliers, in order to remain competitive, these firms must upgrade to the latest technologies to produce smaller, cheaper chips. Conversion to these advanced technologies is essential in order to meet the program cost goals.

The AMI .8 micron process has stabilized into a production capable process, and we have selected it as the platform for our ASIC development. Unfortunately, existing designs (such as our 2.0 micron) cannot be ported without major re-engineering. Our two employees, Mr. Gerry Miller and Mr. Randy Zimmerman, have become engaged in the process of preparing the Beacon design tools to interface to the formats required of AMI .8 micron process. These tasks are broken out as follows:

Activity	Who	Engineer	% Complete	Status
Receive and study Design Rules	RZ		100	
Prepare Technology File	RZ		95	Waiting for check off of test... Sent to AMI
Verify Technology files meet Design Rule Checks	RZ		50	Test File sent... waiting for reply
Analog Schematic Entry	GM		85	Spice Analysis
Digital Schematic Entry	RZ		25	Functional description done
Analog Layout	GM		10	Bond placement done starting on band-gap
Digital Layout	RZ		0	
Simulation	RZ + GM		35	70% analog done...5% digital done
DRC			0	
Tapeout			0	
Test Vector Preparation			0	

Task 2 Prototype Tooling:

Many of the ASIC activities in the above ASIC Design and Simulation chart are necessary to accomplish Task 2... to enable our production fab to produce first article devices which work correctly the first time. Therefore, Task 2 will commence when all of the ASIC Design and Simulation tasks are complete. this activity will only require one to three days of an engineer's time. This is expected to occur late 4th quarter 1997, early 1st quarter 1998.

Task 3. Test Engineering:

The design and development of wafer testing hardware and software is approximately 80% complete. This was accomplished by engineers Hausdorf and Noble. The hardware is operational, and only software needs to be customized for each unique part number. The automation of this testing greatly improved the quality and consistency of critical measurements.

Task 4 Product Tooling

Not Yet Started. this will be late 4th quarter 1997, early 1st quarter 1998.

Task 5 Package Tooling / Manufacturing Design and Assembly:

No activities in this area, however, upon completion of the ASIC, a substrate layout will be implemented. The substrate is akin to a printed wiring board, except it will be constructed on ceramic, vs. Epoxy/glass, as is more typical of these types of products. This is a no risk activity, as it is routinely performed at Beacon. The design goal is to fit all components on a 7.5 mm x 7.5 mm ceramic substrate, which will meet the original cost goal of \$ 0.05. If volumes exceed 1 million pieces per year, then alternate lower cost packages such as stamped metal lead frames, will be explored. However, the tooling charges for these exceed \$100,000.

Task 6 Quality Assurance Runs and Final Report

We anticipate that these work activities will remain as planned.

Projected per unit costs:

Component	Projected Cost (low)	Projected Cost (high)	
ASIC	\$0.10	\$0.12	
TN22	\$0.30	\$0.42	
Capacitor	\$0.04	\$0.08	
Resistors	\$0.01	\$0.01	
Substrate	\$0.05	\$0.07	
Labor	\$0.05	\$0.08	
Product Cost	\$.55	\$.76	
Profit	\$.22	\$.30	
Selling Cost	\$.77	\$1.06	

Summary:

It is felt the program will meet its stated goals of producing a low cost, high performance fluorescent lamp starter which will lower the acquisition and operating cost of fluorescent technology... thus saving significant amounts of energy. The likelihood of success is even greater, now that the TN22 component has been qualified. The challenges of creating a custom ASIC, while still significant, are within the skill and expertise level of the assigned engineers.

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