Material Development of Polymer/Metal Paste for**Flip-Chip Attach Interconnection Technology**

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Conductive Paste Production

In the last leg of the project the major thrust has been on the assembly process using the conductive adhesive, viz., the optimization of the process conditions and the bonding equipment. The paste at this point is deemed optimum in terms of the three basic properties: adhesion, screenability and conductivity. The reliability and wafer level screening is proven reproducibly over several experiment constituting assembly of more than one part.

Using the optimum paste we have provided an uninterrupted supply of reproducible (optimum) paste. By tweaking the compounding conditions a first-level scale-up was successfully achieved. The initial 30g batch to Endicott is increased to as high as 300g batches with similar properties. The large batch material is shown to behave similar to the small batch materials. Also, it has been essential to do large wafer level studies: Endicott has scaled up their screening from 5" wafer to 8" wafer.

Indentation Measurements

The squeezability of a bump is very important in determining the reliability of the structure. This compliance in the thickness direction plays a crucial role in several ways:

1. The bump after drying should be hard enough such that it does not crack under the bonding load. This would lead to infiltration of the encapsulant during the under-filling process. Also the crack can later act as a defect center.

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2. However, some compliance is required such that there is intimate contact between the pad and incident bump during bonding.
3. In the bonding process the material is cooled under load after the bonding is completed. Thus, the hardness of the bump after the subjection to bonding temperature is also important.

We made several blanket samples of paste C and D and subjected them to various loads using a pyramidal indenter. Fig. 1 shows the imprint after the loading on a typical sample. The sample is paste C after drying at 70 C. Even at low loads of 0.1 kg the indentation shape is barreled. The large extrusion of the material indicates that the material is soft and can plastic deform easily. However, after the annealing, the polymer metal composite "sinters" and forms a more compact structure. As a result the hardness improves significantly. Table 1 shows the hardness after the drying process and after the 220 C annealing process. The increase in hardness is about 2 to 5 folds. Since Paste C and D are better than Paste A it is important to note that high hardness after both drying and after annealing is important for a better structure. Of course if this is too high, above 0.2 GPa the adhesion will begin to deteriorate due to poor conformability with the bonding surface.

(This work is in collaboration with Robert Cook, IBM Yorktown)

Commercialization

After Ferro stepped away from licensing negotiations, we have been pursuing other avenue to commercialize the paste material technology. Presently, discussions are underway with Ablestik. A technical presentation was made to them where the properties of the material and the DARPA program have been described.

Paste	Hardness
A, 70C dry	0.076 GPa
A, 220C anneal	0.32 GPa
C, 70C dry	0.19 GPa
C, 220C anneal	0.35 GPa
D, 70C dry	0.084 GPa
D, 220C anneal	0.4 GPa

0.5 kg

0.3 kg

0.2 kg
0.1 kg

0.1 kg

0.3 kg
~~0.1 kg~~

SCALE : 0.5" = 100 μ m

FIG. 1 : PASTE-C dry at 70°C
Indentation load is indicated.

BONDING PROCESS DEVELOPMENT

Chip Bonding

Objective: The objective of chip bonding is to test the effect of various bonding parameters such as bump height and encapsulant on the t-zero joint quality.

Accomplishments: Last quarter we established (flip-chip) bonding process window for electrically conductive adhesive (ECA). An optimum process point was also identified. The assembly process performance is reproducible (over several runs) and repeatable (by several operators), and has resulted strong and electrically good interconnects. Cohesive fractures of the ECA interconnects with fracture strengths of 1400 psi to 2000 psi have been achieved.

During this quarter we have established optimum process parameters for encapsulation. In the past, we identified encapsulation as the most critical process in ECA assembly, with >10% increase in contact resistance and several electrical "opens" after encapsulation. Several encapsulant materials were studied for their flow, dynamic viscosity, gelation at different flow and cure conditions. Matsushita encapsulant with higher dispense viscosity at 80°C, over most encapsulants resulted in a void free encapsulation in 2 minutes or less for the 9.4 mm test chips. A rapid cure at 150°C for 1 hr resulted in <5% increase in contact resistance of assembled chips. The following table compares the dispense (at 80°C) and the lowest viscosity of three commercial encapsulants through the flow and cure process. Matsushita encapsulant, with a factor of 5 to 10 larger viscosity over other encapsulants and faster gelation, resulted in the smallest CR change. The higher the viscosity through flow and faster the gelation of the encapsulant, the less likely is the encapsulant to seep in and perturb the ECA/pad interface, with a resulting increase in contact resistance.

Encapsulant	Dispense/Cure Process	Dispense viscosity cps	Min. Viscosity cps	Gelation Time/Temp
Mat. CV5183S	Disp.@80°C; Cure @130°C	8.5	6.8	5 min (90-100°C)
Mat. CV5183S	Disp.@80°C; Cure @150°C	7.9	6.4	4 min (90-100°C)
Dexter FP4511	Disp.@80°C; Cure @130°C	3.3	1.5	5 min (100-110°C)
Dexter FP4511	Disp.@80°C; Cure @150°C	3.5	1.0	4 min (120°C)
Dexter FP4526	Disp.@80°C; Cure @130°C	1.5	0.5	6 min (100-110°C)
Dexter FP4526	Disp.@80°C; Cure @150°C	1.7	0.5	4 min (120°C)

During the last quarter, Universal has made several software modifications to the bonding tool. No change in bonding process or control was observed as a result of these modifications. Strong and electrically good ECA interconnects were obtained, using blanket chips.

To establish the ECA shelf life (of screened photobumps) several chips screened early this year were bonded, fractured, or encapsulated, and also exposed to reliability testing. High fracture strength (1400 psi to 2000 psi), cohesive fracture, and 1000+ ATC cycles without a failure, indicate >6 month shelf life for the ECA photobumps. These chips will be tested in the future, to establish the shelf life for ECA, if any.

A rework process has been established for the ECA. Non encapsulated chips were pulled off from the chip site, mechanically, and new chips were re-bonded to achieve "good" bonding. The card side was wiped clean with IPA before the new chip bonding. The small adhesive residue left behind on the card side did not interfere with the re-bond process. The new chips bonded at the reworked sites resulted in average contact resistances for all 16 nets per chip. One reworked card (two chips), was exposed to deep thermal cycle (-55 to 125°C) and exhibited no fails in first 1000 cycles. This preliminary result is very encouraging and needs to be reproduced and repeated to develop a statistical data set.

All above results, encouraging and reproducible, were obtained with ECA bumps on blanket Au chips. The test results using chips with a stitch pattern have been consistently disappointing. The stitch chips have a polyimide passivation coating, and electroless Ni and immersion Au pads. Although the screening and photobumping processes are identical for stitch and blanket wafers, the passivation etch during the photoresist strip can lead to formation of polyamic acid which can adsorb on the ECA bumps and result in a weak interface between the bump and the Au pad (on card) during bonding. Chemical analysis of the ECA bumps on blanket and stitch chips are planned and the results will be reported in the annual report. If acid adsorption is evidenced on the ECA bumps, inorganic passivation can be used for the stitched wafers in the future. Alternative hypothesis and analyses will also be explored to address the poor bonding results of the stitch chips.

Reliability

Objective: The objective of the reliability testing is to investigate the overall joint stability of the PMC material as a function of time and in particular, to monitor the stability over time as a function of the t-zero joint resistance.

Accomplishments: In early August, 24 stitch chips (12 cards) were assembled using the optimized bonding and encapsulation process for reliability testing. Three cards each went into the 0°C to 100°C thermal cycle, and 85°C / 85% relative humidity storage. Six cards were submitted to deep thermal Cycle; -55°C to 125°C. These chips were encapsulated immediately after the bonding, by cooling the card to 80°C after bonding for encapsulation. Despite optimum bonding process and control, these chips (cards) exhibited a 12.5% fails as assembled (t-zero). During thermal cycling, additional 1 and 6% fails occurred in 0-100°C, and -55 to 125°C tests, respectively. The t-zero and early fails in the stitched chips are explained by our polyamic acid adsorption and contamination on the ECA bumps hypothesis. A sizable t-zero and early fails for stitched chips have now been observed for the third time.

On a brighter side, 10 blanket chip (5 cards) assembled at the same time as the above stitch chips, exhibited no fails upto 1000 deep thermal cycles of -55 to 125°C. Deep thermal cycle is the most severe stress test, and these ECA interconnects have demonstrated a solder equivalent performance in this test for the last three times. The blanket chips tested in the deep thermal cycle, included 6 month stored (old) chips, refrigerated chips, and two chips that were assembled to a reworked card.

PASTE DEPOSITION PROCESS DEVELOPMENT (Screening)

SUMMARY

A new dispense head was developed to reduce and/or eliminate void formation. The dispense head (See Figure 1) has vacuum chambers (1) adjacent to the linear blade orifice (2) that the ECA is dispensed from. One side of vacuum chamber is formed by the normal ECA dispense blades (3). The other side of the vacuum chamber is formed by outer vacuum blades (4).

The use of vacuum should remove "trapped" air formed by the action of pushing a highly viscous material into a blind hole as shown in Figure 2. The first pass blade motion (5) across the blind holes (6) causes void formation (7) in step 4 because the void has been trapped by the motion of the high viscosity ECA material and the geometry of the hole. The aspect ratio of hole diameter to resist thickness is very important relative to void formation as a function of material viscosity.

Figure 3 shows a range of worst to best cross sections at 0 and 90 degree sections. All part numbers were run with optimum screening parameters, which were .12 "/second head speed, 30-35 psi dispense pressure and 38# downward head force. All features were .008" diameter x .004" high. Wafer 32 and 33B were run with 8-10" Hg vacuum. Wafer 33A and 33C were run without vacuum. By observation, there is no difference between parts run at optimum parameters with OR without vacuum. Apparently vacuum is not enough to influence the high viscosity material to move towards the containment surfaces after the head is moved beyond that area. However, wafer 32 and 33B (both ran with vacuum) had 10 times more good chips than 33A and 33C (ran without vacuum) so the vacuum grossly enhanced the survivability of the bumps.

In conclusion, although these small voids at the base of the deposit have not been shown to adversely affect contact resistance performance, work continues to reduce their occurrence. A lower viscosity ECA is very important to the dispense process, but a lowered viscosity will also give poor contact resistance and poor strength. Therefore, the viscosity must remain as it is to yield good bump resistance and strength.

The next experiment will contain standard screening parameters with one exception. Immediately after the first passes have been processed, the wafer will be placed in a high pressure air chamber. The high pressure will move the ECA material towards the containment surfaces (the resist) and will shrink the air void that has been formed. All this will happen when the material is soft. The wafer will be baked in that pressure at 70°C for 1/2 hour to stiffen the bump in its compressed state. The second series of dispense head passes will fill the bump to the correct height, as it normally does.

FIGURE 1
END SECTION VIEW OF DISPENSE HEAD

FIGURE 2

TIME LAPSE OF ECA DISPENSED IN HOLES (1-7)

0° 90°
 west east west east

#32
(VACUUM)

33A
(NO VAC)

33B
(VACUUM)

33C
(NO VAC)

FIGURE 3

Date: 11/05/97

To: Bill Bernier

From: Michael D. Snyder

Subject: Third Quarter 1997 Report on DARPA Project UIC J/N M919980
ID No. DE-FC-04094AL98817 Covering Universal Instruments Activities
for the Timeframe 6/30/97 Through 9/30/97

Overview

Universal performed work in several areas during the Third Quarter of 1997:

- Modification and continued empirical characterization of the automated and benchtop testbeds
- Use of the Universal testbeds to carry out bonding tests in support of efforts to optimize bonding parameters for the ECA bumped Flip Chips to laminate printed wiring boards (PWB)
- Use of the Universal testbeds to produce ECA bonded samples in support of IBM joint reliability testing
- Continued discussions relating to selection of appropriate test vehicles for incorporation of the IBM ECA polymer material into the work planned by the Universal Flip Chip / Chip Scale Packaging (CSP) Consortium
- Initiated discussion with an outside vendor regarding an alternative heating source for the bonding tool for potential future incorporation into a production implementation.
- Changed the motion control PC card forming the major part of the positioning system control to a more advanced model. This allows the implementation of improved graphic user interfaces to the Automated Testbed.
- Changed the integrated vision image processing engine from an ASI Model 3000 to an ASI Model 3500, which allows use of advanced feature finding algorithms for fine pitch Flip Chip components.
- Implemented a LABVIEW[®] graphical user interface to the Automated Testbed to allow an improved ability for the control of alternative bonding process control sequences.
- Designed and fabricated holding fixtures to allow the bonding of the IBM 4M SRAM Flip Chip, a chip having features 0.005 inch diameter on a 0.010 inch pitch.

These activities, as in the past focused on accumulating a knowledge base to enable rapid development of future production tool capability.

This work represents the culmination of the efforts to develop a potentially viable process for the application of Flip Chips using an electrically conductive adhesive material as the interconnect medium. Though work will proceed on this project to provide the final encompassing report, the effort after publishing the report will not be chargeable under the cost sharing structure of the project.

Universals intent is to continue to help develop the commercial tools and process to allow this ECA medium to be a viable attachment technology for Flip Chips. As mentioned in earlier reports, the Time- Temperature-Pressure bonding cycle still has room for significant improvement, particularly in the desire to reduce the time required at present for the bonding portion of the process (See Figure 1.). We intend to continue our efforts to inject this material into the Universal "Chip Scale Packaging and Large Fine Pitch Direct Chip Attach Consortium", which officially began with a kick off meeting on September 23, 1997.

General Project Activities:

As noted above, a major portion of the expended effort throughout this final period centered on the use of the Automated Testbed to support process testing studies with IBM personnel. The other activities are treated separately below.

Process testing and experimentation support:

- A series of designed experiments (DOE) and surface response tests (SRT) were conducted to continue to identify the set of processing parameters which created the best combination of joint strengths (as measured by pull strength results) and reliability results. The substantial efforts in this area (at Universal) centered on design, fabrication and assembly of suitable test fixtures, operation of the Automated Testbed, and carrying out the physical testing. The effort included measurements of electrical joint resistance in the pre and post underfill condition, as well as joint pull strength evaluation conducted on the Universal Instron® tensile tester.

Automated Testbed Modifications:

- The existing motion control card, a Precision Micro Control Model DCXPC100 was changed to a Model AT200 card. The new card supports drivers for the positioning system X-Y tables which are addressable by the LabView® Software package. The detailed information on the new card is shown in attachment 1.
- The existing ASI Model 3000 Vision engine was changed to an ASI Model 3500 system. This more advanced system allows use of Universal developed vision find algorithms to aid in the location aspects of fine pitch Flip Chip placement on target.
- Installation of LabView Software as an enhanced graphical user interface to the Testbed was completed in the third quarter. This software allows easier implementation of unique processing sequences in the placement and bonding portion of ECA Flip Chip bonding. Details on the Labview® Software is shown as shown as attachment 2.
- A fixture was designed and fabricated to support the IBM 4M SRAM Chip on the Automated Testbed. The fixture is shown in Figure 2. The 4M SRAM Chip will allow us to explore the bonding properties in the fine pitch, small ECA feature domain, the feature size being 0.005 inch Diameter on 0.010 inch pitch.

Future Work

- Incorporation of the IBM ECA material into the Universal Instruments Chip Scale Packaging and Large Fine Pitch Direct Chip Attach Consortium. (See attachment 3. for list of Principles)
- Investigation of alternative heating source for the "production" instantiation bonding tool to increase industrial robustness.
- Refinement of the process cost estimates through the use of the Computer Aided Cost Estimation Tool (CACE) previously developed under this program.

Concern from "Machine" Perspective:

ECA process time requirement larger than solder based alternative

Task

Task	ECA	Solder	
		(UFP)	(4SP)
Fiducial Find	0.6sec	0.6sec	0.6sec
Pick/Inspect/Place	6.0sec	6.0sec	1.3sec
Flux	N/A	2.0sec	0.3sec
Bond	Ramp	N/A	N/A
	Dwell	N/A	N/A
	Cool	N/A	N/A
TOTAL	72.6sec	8.6sec	3.2sec

Figure 1. Processing Time Comparison ECA Bonding vs. Solder

Figure 2. Support Assembly

Specifications

DCX 200 Series Motherboards

DCX-AT200 Motherboard

DCX-AT200

Processor	Intel i960 RISC
Processor Clock	16 MHZ
Code Memory	128k X 16 bit
Data Memory	(Standard) 32k X 16 bit Dual Ported (Optional) 128k X 16 bit Dual Ported 32k X 16 bit Static Ram. @ 55 nsec
Undedicated Digital I/O	16 Channels, TTL
Undedicated Analog inputs	4-8 bit, 0 to 5 volt
Processor Fault Detection	Watchdog Reset Relay
Status LED's	Power, Reset, Watchdog Motor Error (6)
Standard User Interface	ISA\PC\AT bus dual ported memory, Switch selectable, 4k byte boundaries
Optional User Interface	RS-232 (Networkable) IEEE-488 bus
Supply Requirements	+ 5vdc @ 2.0 amps + 12vdc @ .1 amps - 12vdc @ .1 amps
Form Factor	(4.3" X 13.6")

Analog and Digital I/O connector J3

1	+5vdc	14	Digital I/O #6
2	Analog Input #1	15	Digital I/O #5
3	Digital I/O #16	16	Digital I/O #4
4	Analog Input #3	17	Digital I/O #3
5	Digital I/O #15	18	Digital I/O #2
6	Digital I/O #14	19	Digital I/O #1
7	Digital I/O #13	20	Analog Input #4
8	Digital I/O #12	21	+12vdc
9	Digital I/O #11	22	Analog Input #2
10	Digital I/O #10	23	Analog Input Ref
11	Digital I/O #9	24	Ground
12	Digital I/O #8	25	-12 vdc
13	Digital I/O #7	26	Ground

DCX-VM200 Motherboard

DCX-VM200

Processor	Motorola 68020
Processor Clock	16 MHZ
Code Memory	128k X 16 bit
Data Memory	(Standard) 32k X 16 bit Dual Ported (Optional) 128k X 16 bit Dual Ported
Processor Fault Detection	Watchdog Reset Relay
Status LED's	Power, Reset, Watchdog Motor Error (6)
Standard User Interface	VME-bus dual ported memory, Switch selectable, 4k byte boundaries,
Optional User Interface	RS-232 (Networkable) IEEE-488 bus
Supply Requirements	+ 5vdc @ 2.0 amps +12vdc @ .1 amps - 12vdc @ .1 amps
Form Factor	(9.187" X6.299")

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