Microtechnology

**Raymond P. Mariella, Jr.,
Thrust Area Leader**

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Raymond P. Mariella, Jr., Thrust Area Leader

The Microtechnology thrust area conducts activities for the Lawrence Livermore National Laboratory (LLNL) missions of global security, global ecology, and bioscience. Our activities are associated with devices, instruments, or systems which require microfabricated components, including electronics, photonics, microstructures, and microactuators. Our staff of more than 50 people have advanced degrees and expertise in electronics, engineering, mechanical engineering, chemistry, physics, biology, and chemical engineering.

Our longer-term direction is to invent and develop the technology to move into the areas of optoelectronic integrated circuits and into integrated microinstruments. In everything we do, we work through close collaborations with the various LLNL programs, selecting those areas for our attention that offer the greatest leverage. For example, our largest collaboration is with the photonics effort within the Physics Department, and in conjunction with this, our researchers received a patent and an R&D 100 award for a cross-talk-free semiconductor optical amplifier (SOA). This solved the industry's outstanding problem regarding SOA's.

All of the microtechnology work revolves around our Micro Technology Center. Over the last year, with a total budget of over \$10M, including approximately \$0.8 M of technology-base projects, we have successfully performed collaborations with industry, and we have had an instrumentation project for the polymerase chain reaction for DNA amplification, funded by DARPA, achieve international success with a demonstration of real-time detection of product.

Our first-of-its-kind project with Silicon Video Corporation (our microfabricated components were in the critical path of success) has achieved national recognition in its successful development of the technology to fabricate field-emitter-based flat-panel displays. Our principal investigator on that project received the Federal Laboratory Consortium Award.

As a critical part of the invention of seed technologies, we continue to perform LDRD and technology-enhancement projects. Our work in FY-96 included the fabrication of specially-doped silicon films, both wet and dry etching and bonding of substrates, including silicon-on-insulator and large substrates, and biological and medical instrumentation and devices.

In the area of microstructures and microactuators, our personnel have fabricated: (1) silicon-based microaccelerometers for kilo-g and for micro-g accelerations; (2) circular-cross-section capillary channels in silicon wafers (produced via mirror-image lithography and wafer/wafer bonding) which have cleanly separated a mixture of industrial gases; (3) sub-mm adjustable-position bimorphic actuators that function in air or in water; (4) thin-film shape-memory-alloy actuators that have brought our researchers considerable attention for fabricating the world's first self-powered microgripper on a guide wire; (5) thin fresnel lenses; (6) clear ultra-low-stress silicon nitride films, 100 nm thick with 1-cm² area; and many other microstructures.

In interdisciplinary work, we also have had patent claims allowed on our new physical configuration to collect perpendicular light scatter in flow cytometry, which increases S/N by more than an order of magnitude and increases the intrinsic accuracy of the measurement by a factor of 3. We also have demonstrated the world's first real-time detection of polymerase-chain-reaction (PCR) product in a portable instrument. In October of 1996, we took our flow cytometer and PCR instruments to the Joint Field Trials in Dugway, UT, for the open competition.

We have received external support for miniature micromachined valves; integrated photonics; flat-panel display fabrication; portable PCR instrumentation; low-temperature optical modulation; and electrophoresis.

The background of the entire page is a grayscale aerial photograph of a city grid, likely New York City, showing streets, parks, and building footprints. A thick black horizontal line runs across the top of the page. A white, torn-paper-like shape cuts across the middle-right of the page, creating a layered effect. The word "Microtechnology" is printed in a bold, black, serif font on the white background. The large number "3" is also on this white background, positioned to the right of the title. The bottom right corner shows the spiral binding of a notebook, with several black rings visible.

Microtechnology

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3. Microtechnology

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Advanced Plasma Etch Processes for High-Aspect-Ratio, Sub-Micron-Feature-Size Applications

Jeffrey D. Morse
*Engineering Research Division
 Electronics Engineering*

The objective of this effort was to develop and establish plasma etch processes in the newly acquired Lam Transform Coupled Plasma (TCP) Etch Reactor. Our research supports micro-electro-mechanical systems (MEMs), sensors, and programmatic activities at Lawrence Livermore National Laboratory (LLNL) that require high-aspect-ratio, sub-micron, or critical geometry structures to be fabricated in thin film or bulk materials.

Introduction

Plasma etching with advanced tools such as the Lam TCP 9400 reactor is a high-density plasma system that allows for independent control over the plasma efficiency (top electrode power) and the directionality of the ions (bottom electrode bias power).

The result is that extremely small feature sizes ($<1000 \text{ \AA}$) and highly anisotropic structures ($>5:1$) can be fabricated, with extremely high etch rates achievable through operation of the plasma at relatively low pressure regimes (1 to 10 mTorr) in comparison to other etch tools. Technologies that exploit such structures range from MEMs devices, flat panel displays, sensors, and high-efficiency gratings for specialized optics.

For MEMs applications, the feature sizes are larger (1 to 5 μm), yet the requirements of aspect ratio ($>10:1$), anisotropy, and selectivity of etching one material with respect to another (Si vs SiO_2 , for example) are critical. It is desirable to have etch processes for these applications which require only a single photoresist mask or, at a minimum, a single layer of oxide or nitride as a mask, with etch selectivity of silicon better than 10:1 to form the appropriate structures for defined applications.

Progress

Several experimental matrices using the Lam TCP reactor have been investigated to better understand the effects of variations in the

operating parameters (power, pressure, gas mixture) on etch performance. These matrices determined the effects of varying the operating parameters on the etch rates of different dielectric materials, including thermal and plasma-enhanced chemical vapor deposited (PECVD) SiO_2 , silicon nitride, and polycarbonate.

The JMP Statistical Analysis Program is used to analyze the experimental data. The resulting prediction profiles for these materials are illustrated in **Fig. 1** for variations in TCP (top) and bias (bottom) power, pressure, and percentage of CF_4 in the gas mixture. These profiles become the basis for process designs, and subsequent statistical process control, which uses specific performance parameters that are input to the model.

As an example, these results could be used to design a process in which one of the materials is a mask for the other, or one in which one or more of these materials has to be etched in a single etch step, with minimal undercutting of the films. Depending on the specific response of the etch step, a desirability function can be implemented in the statistical model, thus providing the optimal process conditions for the desired response.

Another experimental matrix directly investigated the etch rate and selectivity of etching one material over another, in this case the Si/ SiO_2 system. This particular material system has importance since SiO_2 can be thermally grown from Si. One approach is to develop a chlorine-based chemistry, which chemically forms SiCl_4 on the Si surface as the volatile etch product. Thus the etching of Si is chemically assisted

with Cl_2 plasma gases, and the volatile etch product readily dissociates from the surface when impacted by low energy incident ions or neutrals.

For SiO_2 , no volatile etch product is formed at the surface, therefore etching only occurs when ions of sufficient kinetic energy impact the surface. Proper control of the substrate bias by the bottom electrode power, hence ion energy within the plasma, allows the oxide etching to be minimized, thereby increasing the selectivity of the etch rates. The trade-off with selectivity is anisotropy.

For more chemically-assisted etch processes, the tendency is to increase the lateral etch rates as well. Chlorine-based chemistries have thus far resulted in Si etch rates as high as 3000 Å/min, with excellent selectivity over SiO_2 , greater than 50:1. Due to the

corrosive nature of chlorine chemistry, however, experimental matrices were limited in scope, and the effort focused on the use of fluorine chemistry.

Fluorine-based gas chemistries have similar issues, except that volatile etch species are formed on SiO_2 as well, although those forming on SiO_2 require more energy to dissociate from the surface. Therefore, with careful process selection and control, selectivity of etching Si over SiO_2 can be optimized.

Another consideration in the use of fluorine-based gas chemistries is the optimization of polymer forming radicals in the plasma, such as CF_2 , which readily deposits onto surfaces being etched, thereby reducing the etch rate. Thus, to increase etch rates, gases providing higher ratios of free F_2 , such as C_3F_8 are typically used.

Figure 1. Prediction profiles for variations in pressure, TCP (top) and bias (bottom) power, and percentage of CF_4 in the gas mixture.

Other approaches use SF_6 chemistry. Passivating layers during etching can be taken advantage of as well, to inhibit lateral etching, in this manner achieving excellent anisotropy, such as with the addition of O_2 or H_2 to the chemistries.

Considering a SF_6 -based chemistry, the resulting effects of varying the bottom electrode power are shown in **Fig. 2**. The other operating parameters are detailed in the figure as well. While the etch rates decrease for both materials as the power is decreased, the percentage decrease of the Si etch rate is less, thus the overall selectivity increases. For this example, the selectivity of etching Si over SiO_2 is >10 selectivities. Further improvements in increasing this selectivity are anticipated by broadening out the range of parameters to be studied.

Figure 2. Dependence of etch rate and selectivity for Si/ SiO_2 system for bottom electrode power for operating parameters indicated above.

Figure 3 illustrates the dependence of silicon etch rate on percentage of O_2 in the gas mixture for two sets of operating conditions. While the results are quite diverse, it is believed that the one operating condition creates significant polymer-forming radicals in the plasma, which limit the etch rate of Si. With the addition of O_2 to the gas mixture, the polymer-forming radicals are scavenged by the O_2 , and the Si etch rate is enhanced significantly.

Figure 4 illustrates the etch profile as a function of process pressure. In effect, several parameters can be varied to optimize the processes for specific integration approaches to achieve the desired selectivity, etch rate, and anisotropy. **Figure 4** further illustrates that deep trench etching of Si is possible. In this case, 20- μm -deep Si trenches have been formed at a nominal etch rate of 1.8 $\mu\text{m}/\text{min}$.

Figure 3. Dependence of Si etch rate on percentage of O_2 in gas mixture.

Figure 4. Etch profile as a function of process pressure: (a) 10 mTorr; (b) 20 mTorr; and (c) 60 mTorr.

PECVD-oxide etching was studied using the CHF_3/CF_4 chemistry with the objective of achieving deep sub-micron ($<0.2 \mu\text{m}$), anisotropic, high-aspect-ratio trenches. The mask used was a thin layer of Cr with $\sim 1000 \text{ \AA}$ diameter vias patterned in it using an advanced lithography tool at LLNL. For the design of experiment (DOE) the following input variables were considered in the model;

- 10% $< \text{CF}_4$ (sccm)/($\text{CHF}_3 + \text{CF}_4$) (sccm) $< 40\%$
(total flow is 200 sccm)
- 200 $< \text{TCP power (W)} < 500$
- 30 $< \text{bias power (W)} < 120$
- 10 $< \text{pressure (mTorr)} < 60$

Once again, JMP statistical process control software was used for this DOE, and a Fractional Factorial resolution IV design was constructed. This type of design can estimate the main effects for each input variable, and three of the six interactions. The confounding scheme for the design is presented below;

Fractional Factorial Structure Factor Confounding Rules

$$\text{CF}_4 \% * \text{Press}(\text{mTorr}) = \text{TCP}(\text{W}) * \text{Bias}(\text{W})$$

$$\text{CF}_4 \% * \text{TCP}(\text{W}) = \text{Press}(\text{mTorr}) * \text{Bias}(\text{W})$$

$$\text{CF}_4 \% * \text{Bias}(\text{W}) = \text{Press}(\text{mTorr}) * \text{TCP}(\text{W})$$

The responses measured were the oxide etch rate and the degree of sidewall slope, that is, the tangent of the angle with respect to normal. Thus, a value of zero represents a perfectly straight sidewall.

Oxide Etch Rate Analysis

Etch rate increased with both TCP and bias power, and decreased with increasing pressure. $\text{CF}_4\%$ was not an important parameter for determining etch rate. The highest observable oxide etch rate was $5000 \text{ \AA}/\text{min}$. Using the F-test capability in the software to select significant model parameters, a very good model fit of the etch rate was obtained with just three parameters: TCP power, TCP*Press, and TCP*Bias cross-terms. The model for the etch rate, then, is;

Figure 5. Interaction profile for PECVD oxide etch rate for parameters using LAM TCP reactor. Profiles were determined using JMP statistical analysis software.

$$ER(\text{\AA}/\text{min}) = 315$$

$$+0.0439 * TCP(W) * Bias(W) - 0.113$$

$$* Press(\text{mTorr}) * TCP(W) + 5.249 * TCP(W)$$

For the entire range of parameters explored, the etching is dominated by physical, ion-assisted processes leading to anisotropic etching profiles. There are two distinct operation regimes as a function of pressure. At higher pressures, the etch rates are significantly lower. In this regime, the effect of TCP power on etch rates is minimal, but there is some increase with increased bias power. These effects are most likely caused by the decreased substrate-impact ion energy at 60 mTorr pressure as a result of decreased ion mean-free-path.

At lower pressures, increasing both TCP power and bias power will increase the etch rate. At all TCP power levels, increasing the bias power and decreasing the pressure will increase the etch rates. The interaction profiles are illustrated in **Fig. 5** for the oxide etch rates.

Trench Profile Analysis

The measurements of the trench profile from scanning electron micrographs (SEM) was somewhat complicated due to polymer build-up on the sidewalls. The most anisotropic, vertical profiles were obtained at lower pressure, higher bias power, and higher CF_4 concentrations. For the range of input variables studied, two terms were most significant in predicting the slope: pressure, and interaction of pressure with CF_4 %.

At lower pressures, CF_4 concentration has virtually no effect on trench profiles. At high pressures, where ion bombardment is not as effective, increased CF_4 concentration reduces the sidewall polymer formation, thus improving the sidewall profile. TCP power had no significant effect on the final trench slope.

Figure 6 illustrates the interaction profiles for the sidewall slope. **Figure 7** is a SEM that illustrates one of the trenches etched with the Lam TCP reactor. In this example, a pattern was formed in a resist film on top of a thin Cr layer.

Figure 6. Interaction profile for oxide trench sidewall slope determined using JMP statistical analysis software.

Figure 7. High-aspect-ratio ($>5:1$), deep sub-micron via ($<0.1\ \mu\text{m}$) etched with LAM TCP. Top layer is Cr metal, and the via is etched through $5000\text{-}\text{\AA}$ SiO_2 .

Using this pattern as a template, a via having a diameter of $1000\text{ \AA}$ is etched in the Cr layer. Subsequently, a CHF_3/CF_4 chemistry is used to etch a via through the underlying SiO_2 layer which is $5000\text{ \AA}$ thick, to an etch stop. From the figure it can be seen that the features are preserved, and the sidewalls are very straight. This represents state-of-the-art performance in terms of feature size and aspect ratio. Further, it is estimated that without the use of the etch stop, $>2\text{-}\mu\text{m}$ vias could readily be etched, thus achieving aspect ratios of better than $20:1$.

Conclusion

We have made significant progress towards optimizing plasma etch processes for a variety of applications. The present effort has demonstrated 1) moderately high aspect ratios ($>5:1$); 2) high etch rates ($1.8\ \mu\text{m}/\text{min}$ for Si); 3) moderate selectivity ($>10:1$ for the Si/ SiO_2 system); and 4) etching of a variety of materials, including Si, SiO_2 , Si_3N_4 , Cr, Mo, polycarbonate, photoresist, quartz, HfO_2 , and other rare earth oxides.

These etch capabilities are routinely finding new applications within the programs where other approaches fail to achieve the desired results.

Integration of PCR Amplification and Capillary Electrophoresis in a DNA Analysis Device

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and William J. Bennett
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Microfabricated silicon polymerase chain reaction (PCR) reactors and glass capillary electrophoresis (CE) chips have been successfully coupled to form an integrated DNA analysis system. To demonstrate the functionality of this system, a 15-min PCR amplification of a β -globin target cloned in M13 was immediately followed by high-speed CE chip separation in under 120 s, providing a rapid PCR-CE analysis in under 20 min. A rapid assay for genomic *Salmonella* DNA was performed in under 45 min, demonstrating that challenging amplifications of diagnostically interesting targets can also be performed. This work establishes the feasibility of performing high-speed DNA analyses in microfabricated integrated fluidic systems.

Introduction

Our objective in this project is to integrate at least two micromachined MEMS devices into a working system for DNA analysis. The past few years have seen the development of single, stand-alone micromachined devices. These need to be coupled to other MEMS-based devices to show that they have added value over existing "macro" technologies. Valves and reaction chambers, for example, do not stand alone but are part of integrated systems that also need or could benefit from miniaturization.

In the current project, we have focused on developing a fluidic interface to control reagent flow between a micromachined reaction chamber for the PCR and microchannel CE devices for product analysis. The valving/interface system will be applicable to means of controlling flow between two MEMS devices other than reaction chambers and CE channels.

We have taken a three-tiered approach to integration: 1) to simply combine a silicon-based reaction chamber^{1,2} with a micromachined glass CE channel, in collaboration with the University of California at Berkeley, (UCB), to perform combined micro-PCR-CE experiments; 2) to develop and test a unique microvalve as a possible PCR-CE interface valve; and 3) to explore the development of unique silicon processing to make an inherent/passive valving mechanism.

Progress

Successes were achieved in all three areas, including the acceptance of the results of the integrated micro-PCR-CE system for publication.³

In particular, the direct interfacing of the PCR chamber to the CE channels worked quite well, and a large amount of real analytical data was obtained.

Figure 1. PCR reaction chamber designed to interface to electrophoresis chip.

Figure 2. Real-time micro-PCR with microelectrophoretic detection of a PCR product (268 bp, β -globin genetic marker). The product can be seen on the right, the build-up of non-specific PCR product on the left. (The traces were shifted slightly to the left for ease of viewing.)

The microelectrophoresis system had already been developed at UCB^{4,5}. **Figure 1** is a schematic of the integrated PCR-CE microdevice.³

The separation channels are 100 μm wide, 8 μm deep, and 46 mm long, with a 40-mm distance between the injection channel and the end. The injection channels were 50 μm wide, 8 μm deep, and 12 mm long, with a distance of 2 mm from the reservoir to the separation channel.

The etched glass plate was thermally bonded to the top glass substrate, which had access holes drilled to align with the etched reservoirs. These holes were 1.5 mm in diameter. The silicon PCR chambers with extruded plastic liners were glued in place over the access holes, allowing a direct connection between the reaction chamber liners and CE injection channels. Detection of the electrophoretically-separated PCR products was performed by laser-induced, confocal microscope detection.

Integrated PCR amplification and CE on a β -globin genetic marker (268 bp) was performed in less than 20 min (30 PCR cycles, 83-s electrophoretic separation and detection). This would normally take about 2 h on a commercial PCR instrument with gel electrophoretic detection.

As important as the speed in the integrated approach is its characteristic “hands-off” assay, in that there was no direct sample handling between the PCR amplification and detection.

This is the first time that these two techniques have been combined on a miniature scale, attaining advantages in both speed and integration. We were also able to detect *Salmonella* bacteria with reagents provided by the U.S. Department of Agriculture in the integrated system, and were able to perform real-time product analysis during PCR.

The real-time assay was performed by thermal cycling for a set number of cycles, and performing a 5-s injection step followed by electrophoretic-separation product detection. Results of such an experiment are shown in **Fig. 2**. In that case, the product was detected at 9, 12, 15, and 18 cycles, showing the exponential increase in product concentration. Subsequent cycle analyses showed the leveling-off of product production past 21 cycles, commensurate with predicted reagent limiting factors known to PCR.

It can be seen from the figure that there is an increase in smaller, non-specific product past the twelfth cycle. This is another important feature of an integrated, real-time system: the ability to perform studies on the efficiency of the PCR process itself. In the above case, for example, there was no advantage (in fact, there was a disadvantage) to performing more than 12 PCR cycles. This means that the entire analysis could have been performed in under 10 min.

Future Work

We have been able to demonstrate that improved performance can be attained by integration of two-micromachined devices in a bio-analytical system. The next steps are to continue to improve the integrated system, and add further functionality, such as miniaturized detection components. It will also be important to explore manufacturability and reusability of the systems, to perform real-world analyses on samples of interest, and to package the system into a portable instrument.

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Microactuators for Optical Interferometry

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We are developing a phase-shifting diffraction interferometer as a metrology tool for extreme ultraviolet lithography.

Introduction

Extreme ultraviolet lithography (EUVL) combined with reflective optics is the primary method to achieve critical dimensions in IC processing below $0.25\ \mu\text{m}$, the current state-of-the-art line width. By 2007 AD, when $0.1\text{-}\mu\text{m}$ lithography shifts into high gear, the multi-billion dollar IC industry will require vendors to manufacture lithography tools for EUVL. This requires non-conventional EUV metrology that can measure precisely to below 1 nm. There is

currently a multi-million dollar CRADA in EUVL between Lawrence Livermore National Laboratory (LLNL) and the IC industry.

At LLNL we are developing a phase shifting diffraction interferometer (PSDI)¹ as a metrology tool for EUV optics (**Fig. 1**). This interferometry system is so attractive that vendors want it immediately for conventional optics. Eventually, the success of the EUVL project will be judged not only by its ability to characterize high-precision optics, but also by the ease with which the technology can be transferred to the manufacturers.

Figure 1. Phase-shifting diffraction interferometer system.

Progress

Given the scale of most specialized vendors, companies will not be able to hire a Ph.D.-level expert to maintain such a system. An ideal system would be a black box that they can buy to measure their manufactured optics without much maintenance. It would be extremely difficult for the existing system to be user-friendly with its 30-lb., 3-PZT actuator component, which is mounted vertically.

Our project is to replace this PZT phase-shifter with a miniaturized micromirror. We believe this is a major building block to a black box, and has potential of attracting funding from the industry as well as from the government. The realization of the project proposed here will greatly benefit the optical metrology efforts at LLNL and create new opportunities for industrial collaboration.

Microelectromechanical systems (MEMS) enable the integration of actuation, sensing, control and signal processing onto a single silicon chip. Microactuators that have been developed in the last two years at LLNL's Microtechnology Center include polyimide thermal bimorphs, smart polymers, shape memory alloys, and hydraulic and magnetic actuators. At LLNL we also have experience in designing, fabricating, and testing electrostatic microactuators. Our microvibromotors^{2,3} are being applied to optical modules at the University of California, Berkeley, in collaboration with HP.

The resolution achieved by linear microvibromotors is 0.25 μm . Angular microvibromotors have rotational speeds up to 60,000 rpm. These microactuators are fabricated by adapting IC technology and can be batch-fabricated to reduce manufacturing costs. At LLNL, MEMS and optics are two major core competencies. MEMS components for optical measurements and calibrations have generated successes in many x-ray and laser experiments. Our early successes in Fresnel zone plates, x-ray windows, and gratings, have focused on passive microstructure components, where no moving elements were involved, and most were *ad hoc* projects with no long term plans to advance this promising new field.

By combining existing LLNL optics and micro-fabrication expertise with our recent development of microactuator technologies, a potential major impact area for LLNL can be seeded.

Future Work

Besides the EUVL project in LLNL's Lasers Program, many other programs can benefit from the success of MEMS optics work. Examples are:

- (1) Fourier Transfer for infrared (FTIR) detection for spectroscopy/chemical and biochemical analysis. A precision position-controlled micromirror enables the filtering of wavelengths by the Fabry-Perot interfering principle. Tunable cavity lasers can be developed using the same concept.
- (2) An optical phase array. A 2-D array of these micromirror phase shifting interferometers can set up a platform to steer and focus optical beams.
- (3) Others: MEMS combined with photonics is a very hot research and development field. Microscanners, microshutters, microdynamic focusing mirrors, micromirrors for *in situ* coupling of optical fibers, flat panel displays, and movable diffraction gratings, are all components that have had initial success. Many more applications are being developed. The next generation of photonics will most likely depend on the maturing of this technology.

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Thin Silicon Windows

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We have explored the use of carbon as an etch-stop material for fabricating thin silicon windows. We have produced one of the largest thin silicon windows ever made, 0.4 μm thick, with an outside frame dimension of 24 mm $\times$ 24 mm.

Introduction

Thin silicon windows find many applications in scientific experiments at Lawrence Livermore National Laboratory (LLNL). They are used as supports for x-ray interferometers, in radiation detectors, as debris shields, as supports for Moiré grids, as exit windows for electron sources, in x-ray microscopes, and in other apparatus where one requires a thin transmissive window for the radiation of interest.

The preferred method to fabricate such windows is to diffuse approximately 1% boron (atoms) into the surface of a silicon wafer and then chemically etch away the undiffused silicon from the other surface. This is the so called "p-stop" etch method, which takes advantage of the reduced etch rate of silicon when it is doped with a heavy concentration of boron. Germanium is usually added to compensate for the tensile stress caused by the boron. This material is referred to as SiGeB. In our research we have explored the use of carbon as an etch-stop material for window fabrication, since it has a much higher etch selectivity. This new material is referred to as SiGeC.

Progress

The silicon wafers used in this research were (100) orientation, with a thickness of 530 μm and a diameter of 100 mm. A carbon/germanium-doped silicon film was grown by epitaxy on the surface of

these wafers by Lawrence Semiconductor Research Laboratories (LSRL) in Tempe, Arizona. LSRL is interested in this material for a number of applications, including its use as an etch stop in the fabrication of silicon-on-insulator (SOI) material for high-speed, high-voltage microcircuits. They plan to study this material at the University of California at Davis.

The thickness of the epitaxial layer in our wafers (which eventually determines the window thickness) ranged from 0.1 μm to 1 μm . The carbon concentration was varied from 1 to 7% (atoms). Various amounts of germanium (18 to 40%) were added to the carbon-doped layers to compensate for the stress caused by the carbon.

Once the wafers were received at LLNL, they were coated with a 1000-Å thick film of silicon nitride by low pressure chemical vapor deposition (LPCVD). This process is carried out at 800 °C and does not cause appreciable diffusion of the carbon out of the epitaxial layer. The silicon nitride is used as an etch mask to etch the thin window. Photolithography is used to pattern the wafer on the surface opposite the epitaxial layer, and then the nitride is etched in a Freon-14-plus-oxygen plasma.

Several silicon etches and temperatures were tried, mostly consisting of various concentrations of potassium hydroxide (KOH) which was saturated with isopropyl alcohol (IPA). **Figure 1** is a photograph of a large-area (12-mm $\times$ 12-mm) silicon window fabricated using this method. The window thickness is 0.4 μm and the outside dimension of the

thick silicon frame is $24\text{ mm} \times 24\text{ mm}$. This is a very large window for this thickness. Such large sizes are often required in experiments, such as in x-ray interferometers for laser plasma diagnostics.

Some of the wafers we received were used to determine the etch rate of this new material. For this purpose, we used a chrome-gold etch mask. Silicon nitride could not be used for these experiments since the plasma process used to etch the nitride also slightly etched the underlying silicon. The etch selectivity for this carbon-doped material was found to be much higher than the etch selectivity of the boron-doped material. For instance, when using 44 % (wt) KOH saturated with IPA, at 60°C ,

Figure 1. Large-area ($12\text{-mm} \times 12\text{-mm}$) silicon window, $0.4\text{ }\mu\text{m}$ thick. This window was fabricated using the SiGeC etch-stop material.

the etch rate of the SiGeC material is approximately 1000 times slower than undoped silicon. On the other hand, the etch rate of the SiGeB material is only 100 times slower. This increased selectivity with the SiGeC material makes window fabrication much easier, since the material will tolerate a much longer over-etch.

The ultimate burst strength of the SiGeC windows was compared to the ultimate burst strength of the SiGeB windows for the same window sizes. For these experiments we used windows that were $0.5\text{ }\mu\text{m}$ thick and had a surface area of $12\text{ mm} \times 12\text{ mm}$. The SiGeC windows failed at 1 psig; the SiGeB windows failed at 3 psig.

Future Work

Our SiGeC material appears to be a superior thin window material, primarily because of the increased etch selectivity. Some remaining work needs to be done on the optimum carbon and germanium concentration for this application. Also, we need to establish the thinnest window that can be fabricated for a given area.

In the above experiments, we found that $0.4\text{ }\mu\text{m}$ was about the thinnest window that would survive the fabrication process for the large area of $12\text{ mm} \times 12\text{ mm}$.

Finally, there needs to be a theory developed which explains the etch-stop behavior of this new material.

Eutectic Bonding and Fusion Bonding

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The first goal of this project, the eutectic bonding with gold/tin alloy (Au/Sn), has been shown to produce strong bonds in Si, and these bonds are shown to be excellent for cryogenic applications. Initial experiments in bonding GaAs to Si were not successful, but this can be attributed to contamination of the braze interface. The key idea of this effort should still work since no fatal flaws in the plan have been seen. More effort is needed.

The second goal of this project, the fusion bonding of glass, has been demonstrated with excellent results. Glass substrates up to 58 cm in length have been 100% void-free bonded in Lawrence Livermore National Laboratory's Microtechnology Center (MTC) with some newly developed apparatus and procedures, resulting in an invention disclosure.

Introduction

The two goals of this project encompass large area bonding of substrates. The initial project focus was to develop a Au/Sn eutectic bond between GaAs and Si substrates, in the range of 2 cm², that will withstand cryogenic temperatures (77 K). This first goal would make possible much larger IR imaging array chips for advanced surveillance. The scope of the project was then enlarged to include a completely different, larger area substrate bonding need, the fusion bonding of borosilicate types of glass with areas as large as 400 cm². This second goal makes feasible completely new microstructures that are now possible only with the recent completion of large area lithography technology within the MTC, that was used to first pattern the substrates.

Progress

Eutectic Bonding

The bond between substrates with different temperature expansion coefficients can be subjected to a great deal of stress for sufficient sizes and temperature changes. Our goal is to bond thick GaAs to wafer thin Si. Since GaAs shrinks more than Si, when this combination is cooled, the Si will be subjected to compressive

strain. If the GaAs is thick enough, it will remain approximately flat. The composite can then be used as a carrier to mount focal plane arrays, with similar temperature coefficients to GaAs, onto the Si with currently developed indium bump-bond technology. To use this scheme, a hard, strong eutectic metal bond is needed between the substrates that will withstand the stresses generated by cooling down to cryogenic temperatures such as 77 K. A Au/Sn eutectic alloy has been successfully used in small areas of Si and III-V devices, and is a promising candidate.

Initial testing of evaporated films with separate deposition in layers from separate Au and Sn sources showed that the predicted melting points were not obtained and the surface morphology was questionable. Next, a composite Au/Sn alloy sputtering-source target was obtained, and this source produced films that seemed usable for further testing.

We deposited eutectic Au/Sn sputtered films on Si and GaAs wafers and performed bonding experiments. First tests done on coated Si wafer parts showed that the wetting was good and that the alloy could be heated to past its melting point, without evidence of non-wetting or globule formation. Strips of alloy about a millimeter wide on Si were subjected to adhesive tape pull tests and also to temperature stress tests with no evidence of peeling or bond failure. The most extreme test was

to plunge the bare eutectic strip/substrate into liquid nitrogen. For this temperature shock test, the alloy peeled back from shrinkage to form an arch-like shape, shown in **Fig. 1** upside down. The once-bonded side is up, showing that the alloy peeled back from the Si, but was 100% covered with Si that was pulled out of the host wafer. It shows up as the grooved material at the top of the arch. The alloy is the thin bright white line, visible only at the base of the arch on the side edge. There was no evidence anywhere of alloy separation at the Si interface.

The next bonding tests were done with a Si/eutectic-eutectic/Si wafer pair. A 2-cm² wafer pair of this type was cycled several times to 77 K with about 1 min cycle times, and no evidence of delamination was observed. Before and after cycling tests, samples were subjected to the so-called “razor blade” test. A scalpel was used to try to wedge apart the two wafers. The edges of the wafers are quite rounded, so it is possible to apply a great deal of separation force to the wafers. Ultimately, the Si was observed to fracture at the beginning of the alloy, but no separation of the alloy bond was observed, as illustrated in **Fig. 2**. The rounded edge of the top wafer piece runs diagonally across the lower wafer piece. On the left

Figure 1. Si on a ribbon arch of eutectic alloy. The Si is the grooved material. The alloy is the thin white line on the bottom of the arch and visible on the side of it.

end of the top wafer piece, is the shattered Si region where the end of the scalpel was eventually pushed out sideways with a great deal of force. It went through the Si, but without delaminating the alloy bond region.

Initial tests with eutectic on GaAs thin wafers were promising, in that the alloy seemed to thoroughly wet, and possibly alloy into the GaAs. Again, no peeling or globule formation was observed. Subsequent tests of thin wafer bonding GaAs to Si were not successful. The brazing jig appeared to have been contaminated chemically, and an oxide-like film visually appeared on both wafers. This seemed to prevent the two eutectic alloy coated surfaces from wetting each other thoroughly. More parts remain to be tested and this should be done because of the extremely promising positive results obtained with Si.

Glass Fusion Bonding

The goal of this work was to establish apparatus and procedures to thoroughly bond large (7.5 cm x 58 cm) borosilicate glass plates that are densely patterned with microchannel capillary arrays for DNA sequencing. The capillaries are 20 to 150 μ m in cross-section and 48 cm long.

Figure 2. Two wafers of Si eutectically bonded. After several cycles to 77 K, the pieces were subjected to the razor blade wedge test. The metal wedge shattered the upper wafer piece on the left end, but no eutectic bond failure is seen.

Recently developed large area lithography technology in the MTC was used to pattern and etch the glass substrates. A special and unusual bonding jig and procedure was developed to align and hold the two large glass substrates together in a manner compatible with the high temperature furnace (500 to 700 °C). The apparatus and procedure, which are integral to the success, are described in invention disclosure IL-10039 (S. Swierkowski, 9/29/96). Alignment can be less than 20 μm on these huge plates. (20 μm out of 48 cm is 40 ppm.)

The bonding experiments have shown 100% full fusion bonding with no voids. The original glass interface is undetectable, even under cleaving experiments and SEM observation. The interface region appears as continuous homogeneous glass. The distortion of μm -sized channels appears to be less than a few percent. The channels have been pressure-tested and dye-tested with no delamination or bonding voids evident. Initial tests of DNA electrophoresis sequencing experiments in the prototype capillary plates have produced very good results.

A cleaved section of a bonded plate pair is shown in **Fig. 3**. The SEM view is oblique. The large upside-down U-shaped channel (appears dark) in the top plate, for sample injection, is matched to the shallow trough-shaped channel in the bottom plate and the cross-section is a cleaved interface. There is no evidence anywhere of interface delamination. In fact, there is no observed evidence of an interface except for the pre-etched channels. Another cleaved cross-section from the same bonded plates, but in a region where only the small channel exists, is shown in **Fig. 4**. This nearly end-on view shows the channel shape to be ideal for separation experiments. It has no sharp acute-angled concave corners and is quite smooth. Again, there was no evidence of delamination along the original interface along all of the 101 etched channels.

Figure 3. An SEM oblique view of fusion-bonded glass with large grooves bonded against small capillaries. The view is of a cleaved section of the composite and shows no evidence of delamination.

Figure 4. The end-on view of a cleaved section of the same fusion-bonded glass of Fig. 3, but in a different region, where only the small capillary is present. Its dimensions are 19 μm by 153 μm , or about the size of a human hair. The original glass interface was along the plane of the top of the capillary, but there is no trace of it with the full fusion of the glasses.

Acknowledgment

Major complementary funding for this developmental core competency was also provided by the LLNL BBRP program. These results make possible large-scale, high-throughput human genome sequencing.

Solid-source MBE-Grown GaAs/AlGaAs Ridge-waveguide Semiconductor Optical Amplifiers

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We have established the growth of phosphide-based semiconductors at Lawrence Livermore National Laboratory (LLNL) by solid-source molecular beam epitaxy (MBE), and developed a robust etch-stop technology for applications to ridge-waveguide optoelectronic devices. We have met the technical objectives of this project and have applied it in several areas. In this report we present first the general operating parameters for growing phosphide thin films with a solid-source valved cracker that is now installed and operating successfully. Second, we demonstrate high-quality InGaP thin films that are lattice-matched to the GaAs substrate with less than 0.1% error. Third, we demonstrate wet etch-stop chemistries for selectively etching AlGaAs with respect to InGaP, with a selectivity of over 200 times. Fourth, we demonstrate 0.8 μm -wavelength ridge-waveguide semiconductor laser diodes (SLDs) and semiconductor optical amplifiers (SOAs) that use this technology to simplify processing and improve uniformity. The amplifiers are the first in the world to use an InGaP etch-stop technology to simplify processing. They have a chip gain of 32 dB, which is comparable to the best SOA results in the literature.

Introduction

LLNL has a track record in producing high quality arsenide-based III-V photonic devices such as the cross-talk-free SOA.¹ However, much of the world's data traffic now flows over fiber-optic systems that are built around phosphide-based III-V devices. In this "information age" phosphide-based devices are thus of great interest and our previous inability to grow these materials was identified as one of the weak links in LLNL's overall strategy for III-V photonics research for the next century. With this in mind, one of the major goals of this project was to establish the growth of phosphide-based III-V devices. While we are not the first in the world to grow phosphides by MBE, we are among the first to use a new type of safe phosphorus source known as a solid-source valved cracker. Our project makes a contribution in this area.

In addition to establishing growth of phosphide materials, this project sought to apply the new capability to a real device.¹ The device project that was

targeted was to improve our existing 0.8 μm -wavelength ridge-waveguide GaAs/AlGaAs SOA process by introducing an InGaP etch-stop layer, as seen in **Fig. 1**. The etch-stop layer simplifies the SOA fabrication process, and increases yield, uniformity, and reproducibility of these devices.²

Figure 1. Schematic of ridge-waveguide SOA device with InGaP etch stop.

Progress

In the first phase of this project, a phosphorus source was added to our MBE system to give us the ability to grow phosphide thin films by all solid-source MBE. A new type of “safe” phosphorus source called a valved cracker was used to eliminate the need to work with phosphene gas (which is extremely toxic) or solid white phosphorus (pyrophoric, and also extremely toxic). These valved crackers are loaded with red phosphorus, which is safe to handle. Once the source is loaded and under vacuum, a small amount of red phosphorus is

Figure 2. Double crystal x-ray diffraction results from a calibration sample consisting of three 0.4- μm InGaP layers grown on GaAs with different In and Ga source temperatures.

converted to white phosphorus, which is then used for the growth. Following installation of the phosphorus source and initial characterization, recipes were determined for the growth of InP-on-InP wafers and InGaP-on-GaAs wafers.

A major issue for the growth of InGaP is matching the lattice constant of the InGaP to that of the GaAs substrate. This requires very careful control of the In-to-Ga ratio in the material. This can be controlled by adjusting the In and Ga source temperatures. **Figure 2** shows double crystal x-ray diffraction results from a MBE wafer grown to calibrate lattice mismatch. For this wafer, three 0.4- μm $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ layers were grown on the same substrate with different In and Ga source temperatures. The temperatures for the first layer were $T_{\text{In}} = 885^\circ\text{C}$ and $T_{\text{Ga}} = 875^\circ\text{C}$; the In temperature was raised 5°C for the second layer, and the Ga temperature was lowered 5°C for the third layer.

The x-ray data shows a large peak from the substrate, and three smaller peaks from the InGaP layers, one of which overlaps with the substrate peak. From this wafer, it is determined that the lattice matching condition is for $T_{\text{In}} = 890^\circ\text{C}$ and $T_{\text{Ga}} = 870^\circ\text{C}$, and that the lattice constant shifts $-100 \text{ arc s}/^\circ\text{C}$ with In cell temperature and $+105 \text{ arc s}/^\circ\text{C}$ with Ga cell temperature. Note that 100 arc s corresponds to 0.04% lattice mismatch. For high quality material, the lattice mismatch must be kept below 0.1%, and mismatches below this are consistently achieved with our MBE system.

Once we established the ability to grow InGaP lattice-matched to GaAs substrates, the next step was to develop a wet etch chemistry for selectively etching AlGaAs with respect to InGaP. For this

Figure 3. Selective etch results for removing AlGaAs down to a 7-nm-thick InGaP etch-stop layer with 1:8:100 $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ at room temperature. (a) Etch depth vs. time. The 7-nm-thick layer holds off the etchant for 3 min; (b) etch rate vs. time, showing etch selectivity greater than 200 times for AlGaAs over InGaP.

purpose, a test wafer was grown that incorporated an InGaP etch-stop layer in the middle of $2\text{ }\mu\text{m}$ $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$. The thickness of the InGaP layer was chosen as 7 nm, or about 25 atomic layers. The selective etch used was $1:8:100\text{ H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, which etches AlGaAs at a rate of $0.5\text{ }\mu\text{m}/\text{min}$ at room temperature. To determine the selectivity of this etch, the test wafer was masked with stripes of photoresist, diced into $2 \times 5\text{ mm}$ pieces, and etched for different times in the solution. The photoresist was then stripped from these wafers, and the etch depth was determined using a profilometer.

The results for the etch depth as a function of etch time are shown in **Fig. 3a**. From this figure, it is seen that the 7-nm-thick InGaP etch stop held off the etchant for about 3 min. Thus, stopping the etch any time between 2 and 5 min would yield an etch depth of exactly $1.0\text{ }\mu\text{m}$ and a smooth surface. In practicality, it was found that over-etching by too long affected the width of the ridge-waveguides, and over-etching of about 15 s provided better device results than over-etching by several minutes.

Figure 3b shows the etch rate as a function of time for the test wafer. An etch selectivity of over 200 times for removing AlGaAs with respect to InGaP was achieved.

Following development of the InGaP growth and selective etch recipes, this technology was used to fabricate ridge-waveguide semiconductor lasers and optical amplifiers. The same MBE wafer design is

used for both lasers and amplifiers, and they differ only in the angle of the ridge waveguide with respect to the cleaved facets of the device. For lasers the ridges are perpendicular to the cleaved facets, which then act as the laser mirrors, and for amplifiers the ridges were tilted by 7° from the perpendicular to reduce the fraction of reflected optical power to below 10^4 .

The MBE-grown wafers consisted of a n-type GaAs substrate, a $1.0\text{ }\mu\text{m}$ n-type GaAs buffer layer, a $1.0\text{ }\mu\text{m}$ n-type $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$ lower cladding, a $0.4\text{ }\mu\text{m}$ graded-index single quantum well active region, a $1.0\text{ }\mu\text{m}$ p-type $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$ upper cladding, and a $0.1\text{ }\mu\text{m}$ p+ GaAs contact layer (**Fig. 1**). A 7-nm-thick $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ etch-stop layer was inserted in the upper AlGaAs cladding $0.2\text{ }\mu\text{m}$ above the active region. The structures were grown at 835°C thermocouple reading with an arsenic over-pressure of 4.5×10^{-5} Torr, except for the InGaP layer which was grown at 480°C with a phosphorus over-pressure of 3×10^{-5} Torr. The arsenic and phosphorus sources were both EPI valved crackers, and both cracking sections were operated at 920°C .

Although our primary interest is in ridge-waveguide SOAs, it is easier to characterize the quality of the MBE wafer by fabricating broad area laser diodes, and the quality of the device processing by fabricating ridge-waveguide laser diodes. The quality of a wafer is determined by the threshold current density for broad area lasers fabricated from the

Figure 4. Pulsed ($1\text{ }\mu\text{s}/1\text{ kHz}$) light vs current for 500- μm and 1000- μm -long ridge-waveguide 830-nm laser diodes fabricated using the etch-stop technology. Threshold current is 11 mA for the 500- μm -long-device, and 17 mA for the 1000- μm -long device.

Figure 5. Pulsed ($1\text{ }\mu\text{s}/1\text{ kHz}$) chip gain at 100 mA drive current as a function of device number in a 12-element SOA array.

material. The wafers grown for this project showed minimum broad area threshold current density of 159 A/cm^2 for 1-mm long devices, which is an extremely competitive number for unstrained GaAs quantum well lasers such as this. Results from ridge-waveguide laser diodes are shown in **Fig. 4**. The threshold current was 11 mA for a 500- μm long laser, and 17 mA for a 1000- μm long laser. The internal quantum efficiency was measured to be about 95%.

These numbers are comparable to the best results to date for unstrained lasers from our MBE system. This is important because it proves that the addition of phosphorus to the MBE growth chamber has not had an adverse effect on the quality of our AlGaAs/GaAs laser material.

The results of 830-nm ridge-waveguide SOAs are shown in **Fig. 5**. The SOA gain is shown as a function of device number for a 12-element SOA array. The gain was measured as $31.6 \pm 0.35 \text{ dB}$ for these devices (optical gain of about 1500 times). The uniformity of gain across the array is partially attributed to the uniformity of etch depth obtained through use of the InGaP etch-stop layer. These devices are the first SOAs fabricated using an

etch-stop technology, and the gain is believed to be comparable to the best results in the literature for SOAs in general.

Future Work

Although this was a one-year project, the phosphorus growth technology developed here will be used in many future applications. It is already being used for the SOAs discussed above, for substrate removal etch-stops, and for 1.55 μm SOAs. Our future plans are to use this technology for active/passive integrated optics and for vertical-cavity laser diodes.

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arge Area Lithography

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A general purpose large-area lithographic apparatus and process have been established, enabling the Lawrence Livermore National Laboratory's Microtechnology Center (MTC) to make unique programmatic parts. Etching and bonding have been completed for the first programmatic components from this technology: electrophoresis capillary array plates for use in the BBRP human genome program. This technology should also be suited to several substrate types commonly developed in the MTC that are not amenable to spin coating, even if they are not large. This would include substrates that are uneven or stepped, non-flat or curved, or thick and heavy. It is also ideal for double sided coating.

Introduction

The goals of this project were to design, fabricate, and test apparatus and processing procedures that will enable the MTC to make high resolution (5 to $10\text{ }\mu\text{m}$) features on very large ($18 \times 61\text{ cm}$; $7 \times 24\text{ in.}$) substrates. The apparatus includes: 1) a photoresist dip coating machine for large substrates; 2) a UV flood exposure system for scanning substrate illumination with UV for contact printing the fine mask features; and 3) bake-out apparatus, developing trays and filters for recycling the large volume (6 L) of photoresist.

The procedures include 1) qualifying a special vendor, 2) obtaining high-resolution photo masks of flat panel display size ($20 \times 24\text{ in.}$), and 3) producing high-resolution, full-length capillaries in high-density arrays etched in glass substrates, initially $3 \times 18\text{ in.}$ in size, as needed by BBRP program.

Progress

Photoresist Dip Coating

Our first major effort in large area lithography was to design and build an apparatus for coating large substrates with specialized photoresist. The literature and vendors were reviewed and dip coating was selected as the method over other possibilities that include roller coating, spray coating, dry film transfer, meniscus coating, and spin coating. A

large apparatus, about 2 m tall and about 1 m wide, was designed and built to hold the substrate and to lower and raise it slowly in a tank of photoresist.

It is essential that the speed is slow and uniform, and that vibration be at an absolute minimum.

The apparatus shown in the background of **Fig. 1** has produced uniformly coated plates as large as $7.5 \times 60\text{ cm}$. The pull rate is about 2.5 cm/min and the photoresist is about $6\text{ }\mu\text{m}$ thick. These values are right on the manufacturers design values. The thickness varies less than a micron; the lateral

Figure 1. Large-area ($45 \times 55\text{-cm}$) master photomask, held in the foreground. In the background is the 2-m -tall photoresist dip coating puller apparatus.

spread in optical interference fringes is over several centimeters. The apparatus has easily interchanged photoresist tanks, so different width and depth tanks can be used to match substrate size and thereby minimize photoresist usage.

Photomasks

Producing photomasks for very large substrates is a highly specialized business, mainly focused on the flat panel display industry. By relaxing the normal line width specifications a little and concentrating the other mask specifications on minimizing the number of shorts or opens on a multi-design grating mask, it was possible to obtain a very high quality 45×55 cm mask with dense arrays of gratings, including tapered structures, with line widths varying from 20 to 100 μm , comparable spacings, and lengths of 48 cm.

There were no shorts or opens on this plate, which is remarkably high quality. This master photomask plate is shown in the foreground of **Fig. 1**. The five-design plate costs under \$5K, comparable to the cost per design for other high resolution masks used for 7.5 cm wafers. This plate was scribed and cleaved into the five separate plate designs within the MTC, with a specialized technique to prevent scratching or contaminating the separate masks with scribe fragments. Adhesive tape and clean room vacuum were used.

Figure 2. Typical printed features, subsequently etched in Cr/Au, shown from a portion of a 7.5×58 -cm glass substrate. The line widths are 107 μm on a 300 μm pitch, and the lines are 48 cm long. The resist is positive and etched regions are shown as dark lines.

Mask Alignment

Grating sub-masks 7.5×55 cm long were used with manual alignment onto dip coated borosilicate float glass substrates in the contact printing mode. The manual alignment is done with a low power magnifier. Hand adjustment and alignment within 20 μm is easily obtained. The contact is maintained by simple spring steel binder clips around the perimeter. By clamping from one end to the other, it is easy to get very close contact, as evidenced by optical interference fringes and also by the final quality of the printed lines.

Contact Printing

A second major apparatus was constructed to expose the mask/substrate clamped pair. No convenient deep UV sources were available for this large substrate size. An existing MTC deep UV flood source has a field of exposure of about 10 cm. An apparatus was constructed to slowly drag the mask/substrate pair under a slot of light from the existing unit. Adequate exposure is obtained, even for this very thick resist, in about 10 min. This is conveniently done by swinging the current light source head out over the end of its table and mounting the exposure puller apparatus temporarily onto pre-set pins on the end of the table. This exposure apparatus is about 1.5 m long and would stick out into the workspace too much when it is not being used.

Lithographic Results

Initial tests on quarter-sized (to save costs) substrates showed excellent photoresist coatings. Exposure and development were optimized on these smaller substrates with the aid of a special 7.5 cm very high resolution test mask. The development test mask is a top quality e-beam-generated set of gratings and exposure test patterns with line widths from 10 to 80 μm . Even with the 6- μm -thick resist that is specialized for dip coating, it was possible to print the 10- μm test lines with a narrow range of exposure and development. For line widths of 20 μm and larger, it is very easy to print high quality patterns.

A more serious test for the project was to print the full length designs. This was done by printing onto a Cr/Au-coated 7.5×58 -cm substrate with an actual BBRP program capillary array design. This

design had 101 channels of 100 μm line width with an initial pitch of 580 μm and a tapered middle section, followed by an output section pitch of 300 μm . From the entire process, a few defects were visible on the printed pattern that were caused by particulates, most likely in the dip coating part of the process. Only about three printed lines out of 101 were flawed in width by process defects, but none of the lines were shorted or open.

The printing quality onto the gold film is excellent over the whole plate, as shown in **Fig. 2**.

Acknowledgment

Major complementary funding for this developmental core competency was also provided by the LLNL BBRP program. These results make possible large-scale, high-throughput human genome sequencing.

Phase-Shift Lithography

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We have used phase-shift photomasks to enhance the lithographic capability of steppers.

Introduction

Programs at Lawrence Livermore National Laboratory (LLNL) often find the need for sub-micron lithography. As an example, the Advanced Microtechnology Program (AMP) is working on giant magnetoresistance devices for advance-read heads for the magnetic disk industry. For this application, 0.25- to 0.5- μm lithography is required. In addition, sub-micron pinholes are required for point diffraction interferometers, and sub-micron resolution targets are needed for x-ray tomography experiments. Unfortunately, the state-of-the-art steppers used by industry to do this are very expensive: a 0.7- μm stepper costs \$1.5 M; a 0.35- μm stepper costs \$5 M. Also, there are not many companies willing to do sub-micron lithography as a service. Consequently, there is motivation to develop techniques to enhance the lithographic capability of available equipment. This can be done with phase-shift photomasks, as we demonstrated in this research project.

Progress

A number of phase-shift techniques have been explored by the IC industry. The one we used is referred to as edge phase-shift masks, and is illustrated in **Fig. 1**. With this technique, there is no opaque chromium on the photomask, as is normal. Instead, a phase-shifter region is etched into the surface of the photomask so that the electric field

vector in the illuminating UV is shifted by 180°. To do this, the etch depth, d , has to be equal to:

$$d = 0.5\lambda/(\eta - 1)$$

where λ is the wavelength of the exposing radiation (i line = 0.365 μm) and η is the index of refraction (1.46 for quartz). Using these values, an etch depth of 0.3832 μm is needed for a quartz phase-shift mask. The intensity to expose the photoresist at the wafer is proportional to the square of the electric field intensity. Since the magnitude of the electric

Figure 1. Illustration of edge phase-shift lithography process.

Figure 2. (a) Photoresist line, $0.2\ \mu\text{m}$ wide and $1\ \mu\text{m}$ thick, printed with an edge phase-shifted mask; (b) photoresist posts, $0.3\ \mu\text{m}$ diameter, $1.0\ \mu\text{m}$ thick, printed with a phase-shifted mask.

field vector is forced to pass through zero, the resulting intensity profile is narrower than would be obtained with a conventional chrome photomask. The photomasks we used were fabricated by Du Pont Photomasks for Ultratech's stepper. These photomasks contained a wide range of feature sizes and were fairly expensive, \$7.7 K each.

Our experiments were performed at Ultratech, in San Jose using their SATURN 1X stepper, model 2550i, which uses $0.365\text{-}\mu\text{m}$ radiation, and has a numerical aperture of 0.365 and a minimum resolution of $0.7\ \mu\text{m}$. Our goal was to lower the minimum resolution of this machine by using edge phase-shift masks. We used 150-mm silicon wafers for the experiments. They were coated with resist, exposed and developed at Ultratech. The wafers were then brought back to LLNL where they were sectioned and inspected using our SEM. Many experiments were performed in an effort to optimize the process. The most important variables turned out to be the exposure intensity and the focus. Some modeling, with the PROLITH 2D program was used to guide the experiments.

Figure 2 shows some results of our work. In **Fig. 2a** we see an SEM of a $0.20\text{-}\mu\text{m}$ line of resist which is full thickness, $1\ \mu\text{m}$. This line was printed from a mask feature consisting of a phase-shifted region adjacent to a non-phase-shifted region. In **Fig. 2b** we see an SEM of a column, with a diameter of $0.3\ \mu\text{m}$ and a thickness of $1\ \mu\text{m}$. In both cases, the resolution of the stepper is clearly improved. The column in **Fig. 2b** was printed using a 0.75 by $0.75\text{-}\mu\text{m}$ phase-shifted area on the photomask. Some experiments were performed doing a double exposure of a phased-shifted edge. The second exposure was rotated at 90° to the first. These experiments resulted in columns which were full thickness and had a diameter of $0.2\ \mu\text{m}$.

Future Work

The above results clearly show the advantage of using phase-shift lithography to improve the performance of a projection printer. The features printed consist mostly of straight lines and circular columns. Some experimenters require more complicated features with corners and/or elliptical shapes. These shapes are more difficult to accomplish using the phase-shift approach.

The features printed so far were on bare silicon surfaces. We need to explore this technology on other surfaces, such as those coated with metal and/or containing topography.

Thermally Robust Optical Semiconductor Devices Using AlGaInAs Grown by Molecular Beam Epitaxy

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We have proposed and demonstrated a thermally robust semiconductor optical amplifier (SOA) at 1.5 μm wavelength. The novel contributions are the use of thermally robust gain medium at 1.5 μm wavelength and the use of a highly thermally conductive dielectric for the fabrication of the SOA. The devices possessed high gain, over 30 dB, and thermally robust behavior in pulsed operation from 60 to 80 $^{\circ}\text{C}$.

Introduction

We have addressed the problem of the thermal sensitivity of optoelectronic devices at 1.5 μm wavelength. The reasons for the thermal sensitivity are that the usual semiconductor material used for the active gain region, InGaAsP, suffers from poor electron confinement and Auger recombination, a strongly temperature-dependent non-radiative recombination mechanism. The poor electron confinement is due to small conduction band off-sets of the active region with respect to the surrounding cladding.

Our solution is twofold. First, we use a thermally robust gain material, AlGaInAs/InGaAs, that has shown excellent thermal characteristics for laser diodes at 1.5 μm wavelength. Second, we use a highly thermally conductive dielectric material near the active region that both serves as a waveguide and conducts heat away from the active region where most of the heat is generated. This demonstration of making a high-gain thermally robust SOA using AlGaInAs/InGaAs is a first, to our knowledge.

Indeed, making a SOA thermally robust is more difficult than the demonstration of thermally robust laser diode since the carrier density level is typically a factor of three higher than in a good laser diode design. Thus, Auger recombination is almost a factor of 30 higher, since it depends on the cube of the carrier density. Ultimately, we hope to operate these SOAs without thermoelectric coolers.

Thermoelectric coolers operate with currents on the order of a few amps and often are the reliability bottleneck in an optoelectronic module.

Briefly, we will describe a SOA. The basic function of any optical amplifier is to make the light intensity brighter. In the case of a high performance SOA, the light is made brighter by about one thousand times, or 30 dB. This number is reduced by input and output fiber coupling losses which can be around 6 dB total. **Figure 1** shows a schematic of a ridge waveguide SOA. The light is confined in two dimensions by an optical waveguide. The p-type and n-type semiconductor regions have a lower index than the intrinsic region, thus forming an optical waveguide in the vertical direction. In the horizontal direction, a waveguide is formed by the etching of the ridge. Outside the ridge, the effective index for

Figure 1. Basic diagram of a semiconductor optical amplifier.

the optical mode is lower than in the center since the index for the dielectric is made lower than the p-type semiconductor. The ridge height is critically adjusted to keep the waveguide single mode in the horizontal direction. The ridge width is typically about 5 μm .

The light beam propagates down the ridge waveguide, approximately 1000 μm in length. Gain is provided by stimulated emission that occurs in the intrinsic or active region. By injecting current through the device, holes are injected into the intrinsic region from the p-type region and electrons, at a higher energy, are injected in from the n-type region. The electrons and holes recombine and give off the energy in the form of light. If a light beam is present, then the release of energy will be "stimulated" and the net effect is a coherent addition of energy to the original light beam. Thus, as the beam propagates down the ridge waveguide it gets brighter and brighter. Ultimately, saturation of the gain due to the signal and spontaneous emission sets an upper limit on the amount of gain that can be obtained.

Optical amplifiers are used to make up for losses in the transmission of an optical signal. The losses can arise from serial transmission of a light beam in an optical fiber. The amplifier is used in a fiber optic link as a booster, regenerator, or preamplifier between the transmitter and receiver. Also, as optical networks become more prevalent, losses can occur from the distribution of the signal to many users or by splitting losses in a switched network. Optical amplifiers can be used to make up for splitting losses as well. For semiconductor optical amplifiers, the advantages over other types of optical amplifiers are in cost, size, and the fact that they can be switched at a rate more than six orders of magnitude faster than the doped fiber amplifiers. The main problem preventing their widespread use has been the problem of cross-talk between different wavelength channels and gain recovery in the time domain. These problems arise from the dynamic gain variations that occur in the SOA. Recently, we have demonstrated a solution to this problem that we believe will enable the widespread deployment of SOAs.¹

Progress

Figure 2 shows the band diagram for the active regions and surrounding p- and n-type material. The carriers (electrons and holes) are confined to the active region by the increase in the band gap energies between the active region and the surrounding

n- and p-type regions. As the temperature is increased, the resulting electron energy distribution causes the higher energy electrons to surmount the band gap of the n- or p-type regions and leak out of the active region. The effective mass of the electrons is much lighter than that of the holes, and the loss of carriers due to thermionic emission out of the active regions tends to be dominated by the electrons. The quantum wells provide improved carrier confinement and make the stimulated emission of photons more efficient.

In the case of the AlGaInAs/InGaAs, the difference in energies in the conduction band between the bottom of the quantum well and the conduction band in the n- or p-type regions is around 500 meV. This energy difference compares quite favorably to the energy differences in the conventional material used at 1.5 μm wavelength. For InGaAsP active regions and InP n- and p-type regions, the energy difference is around 300 meV.

Also, in the case of the AlGaInAs/InGaAs material system, strained InGaAs quantum wells are used. In an energy versus momentum diagram, this strain causes the light and heavy hole bands to split in energy. The result is that conservation of energy and momentum required for Auger recombination to occur is significantly reduced. Auger recombination is a non-radiative recombination mechanism between the electrons in the conduction band and holes in the valence band, and thus suppresses efficient stimulated emission.

The molecular beam epitaxy (MBE) machine was used to grow the thermally robust material. To grow high quality AlGaInAs films on InP substrates, high quality epitaxial InP needs to be grown. To accomplish this, a solid source phosphide cracker was prepared and installed into the MBE. The film stacks that were grown consisted of a n-type InP buffer, a n-type AlGaInAs region, a graded AlGaInAs region to a lower energy band gap, an intrinsic

Figure 2. Energy band diagram for the AlGaInAs/InGaAs multi-quantum well heterostructural material.

region consisting of AlGaInAs barriers and InGaAs quantum wells, a graded AlGaInAs region to a higher energy band gap, a p-type AlGaInAs region, a p-type InP buffer region, and a p-type InGaAs cap layer. All the layers were lattice-matched to the lattice constant of InP, except for the InGaAs, where an approximate 0.7% tensile strain was introduced.

An x-ray diffractometer was set up and the lattice match conditions were measured. Several wafers were grown and the MBE growth conditions were adjusted to achieve the necessary lattice match conditions. Broad area lasers were processed from the resulting laser material and the laser thresholds were measured. A laser threshold current density of 400 A/cm^2 was achieved. For MBE grown AlGaInAs/InGaAs, this performance number is the best by a significant margin as compared to currently published work.

The laser wafer material was then processed into ridge waveguides using a self-aligned process developed at Lawrence Livermore National Laboratory (LLNL). The ridges were tilted at 7° with respect to the (011) crystal plane. The etch process was developed so that smooth and controlled etches are achieved on InP. A self-aligned and highly thermally conductive dielectric was deposited using a magnetron sputtering machine. The device is self-aligned since the electrical contact opening in the dielectric and the top of the ridge waveguide are intrinsically aligned in the process. This dielectric provides a lower index of refraction so that a waveguide is achieved in the lateral direction. Also, it provides for a highly thermally conductive material that has a significantly higher thermal conductivity than that of regrown InP. The devices are cleaved along the crystal planes. The tilt in the ridge with respect to the crystal facet is used to suppress the coupling of the back reflection into the guided mode. The back reflections into the guided mode should be reduced to about 10^{-4} ; otherwise undue spectral gain ripple or lasing can occur. The process is routinely performed and good yields are achieved. **Figure 3** shows a SEM of the completed SOA device.

A plot of the amplified spontaneous emission (ASE) versus wavelength from the device is shown in **Fig. 4**. The output was taken with a multi-mode fiber coupled to the output of the SOA. The signal was measured using an optical spectrum analyzer with a 10 nm resolution bandwidth. The center wavelength is at 1535 nm and the full width at half-maximum (FWHM) is approximately 60 nm, representing about 8 THz of optical bandwidth. The operating current for the device was 300 mA.

To facilitate rapid measurements of the gain of the device, we used a power meter to measure the ASE power output of the device. The formula for ASE power coupled into the guided mode of the SOA is given by $P_{\text{ASE}} = 2 h\nu \Delta\nu (G - 1) \chi$, where G is the gain of the SOA, $h\nu$ is the photon energy at $1.5 \mu\text{m}$ wavelength, $\Delta\nu$ represents the optical bandwidth of the ASE spectra, and χ represents the amount of inversion in the gain medium and ranges from 1 to 3 dB.

Figure 3. SEM photo of the completed thermally robust SOA using AlGaInAs on InP substrates.

Figure 4. Amplified spontaneous emission spectrum for the $1.5 \mu\text{m}$ SOA device.

Figure 5. Gain versus current at various temperatures for the 1.5 μm SOA for (a) pulsed and (b) CW operation.

Thus, by measuring the ASE power output, we can obtain a rapid measurement of the gain present. **Figures 5a** and **5b** show the pulsed and CW gain of the SOA device as a function of applied current at various heat sink temperatures. The current pulses were 1 μs in duration at a 1 kHz repetition rate. At room temperature, the SOA device showed a maximum gain of over 35 dB pulsed and 28 dB CW. At 60 °C, the device showed 32 dB gain pulsed, and 17 dB CW. At 80 °C the pulsed gain is still over 20 dB. The pulsed data with temperature being varied indicate the performance of the active region alone. The drop in gain due to CW operation indicates how well the heat is being extracted from the gain region.

Unfortunately, the current consumption is quite high. We are taking steps to reduce the current by redesigning the optical mode so that a narrower ridge width and adequate ridge height to reduce current leakage is achieved while still maintaining the effectiveness of the anti-reflection tilted facets. We are confident that we can achieve a low current consumption device and have the CW gain versus current data approach the pulsed data to within several dB. It should be pointed out that

in spite of the high current consumption, the devices, as they stand, can operate to 60 °C and still have an adequate gain.

Future Work

Next year we look forward to improving the device results and then achieving polarization-independent performance, which will allow us to start field testing the thermally robust high performance SOA devices at 1.5 μm wavelength in real world optical data links.

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Porous Silicon Formation and Characterization

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We have formed various porous silicon films using electrochemical and chemical etching techniques and have measured basic properties of the films, as well as adsorption/desorption and gas transport characteristics. We have also developed fabrication procedures for porous silicon membrane structures on silicon and pyrex.

Introduction

Porous silicon has attracted significant interest recently, primarily due to its light emission characteristic. However, the material can have many other applications for microelectromechanical system (MEMS) devices, including use as gas sensing or fluidic elements, which have been explored in this study.

Progress

Equipment

The pore diameter of porous silicon is critical to the resultant film properties. In this study we have considered pore size diameter varying from about 10 nm, 100 nm and up to the 1 μ m range.

The smallest pore material was formed using an existing conventional electrochemical etch apparatus with single-cell anodization.¹ Current is applied to a platinum wire immersed in a HF solution in a teflon beaker which flows to a (100) silicon substrate mounted with an O-ring seal opposite the wire. The largest pore material was formed using wet etching of (110) silicon in a heated KOH solution.

Intermediate pore material is possible using either technique. For electrochemical formation, a modification of the etch apparatus was made to provide backside illumination without heating.² This was accomplished using a small tungsten lamp with an infrared filter and cutting away the substrate backside contact plate except at the wafer edges. Packing of the bottom of the teflon beaker was necessary to prevent light penetration

into the etch solution. A simple silicon cover was placed on top of the beaker to prevent background light input.

Film Formation

Most of the films made were electrochemically formed without backside illumination using a HF etch solution on p+-type substrates. This procedure is expected to give approximately circular cross-section pores at about 10 nm diameter. The heavily doped substrates were chosen as a compromise between high porosity and the mechanical integrity of the films.³ The formation rate was about 1.8 μ m/min, with no apparent area or voltage dependence. Reproducibility of the etch rate was verified by consistent etch weight loss within 5%, with repeatable etch solution desorption, also measured by weight. Film thicknesses from about 50 to 150 μ m over a 4.35-cm-diameter area were made. The thicker films were used for adsorption measurements on a weight balance.

The films formed using chemical etch were made with a KOH etch solution on p-type substrates. The pore pattern was an alternating array of 5- μ m rectangular slots aligned parallel to the (110) wafer flat. Film thicknesses up to 60 μ m were made.

Only initial attempts were made to form circular pores of intermediate to large size using the electrochemical etch with backside illumination. Wafers with n-type dopant and appropriate resistivity were acquired to form 0.2 to 2.0 μ m diameter pores. These experiments are on-going. Resist patterning for formation of circular holes and rectangular slots of intermediate size are not trivial and are under review.

Film Basic Properties

The porosity of the small diameter pore material was measured at 32%, using weight measurements before and after formation and removal. The etch rate was extremely fast in KOH wet etchant at room temperature, at a value of 25 $\mu\text{m}/\text{min}$, about 1250 times faster than that of crystalline silicon. However, the etch rate was reduced using $\text{CF}_4\text{-O}_2$ dry etch to a value of 3.6 $\mu\text{m}/\text{min}$, only 18 times faster than that of crystalline silicon. The difference is presumably due to the more limited chemical etch component of the dry etch, with corresponding reduced attack on a smaller value of surface area. Film cleaning in standard RCA-1 solution gave some oxidation, but no measurable weight change. The surface of the porous silicon was hard and did not scratch during typical process steps.

The porosity of the large diameter material was about 70% by SEM observation. Etch rate in wet KOH or dry $\text{CF}_4\text{-O}_2$ is virtually identical to that of crystalline silicon. Film cleaning in RCA-1 solution had no effect.

Film Adsorption/Desorption

The adsorption/desorption characteristic is important for gas sensing applications. Adsorption measurements were made at room temperature by exposure of thick porous silicon films, made with small pore diameter, to the vapor pressure of a particular liquid under sealed conditions, followed by weight increase measurements on a balance. Desorption was generally measured at room temperature also, by weight loss. Typical liquids used were water and ethanol.

Figure 1. Adsorption/desorption characteristic for small-pore size porous silicon film of 150 μm thickness and 4.35 cm diameter.

Initial data indicates that the calculated amount of adsorption is about 10 to 40% of film saturation. The adsorbed capacity of the porous silicon film for water was about 32 mg/cm^3 for saturation, whereas that for ethanol was at least 150 mg/cm^3 , since saturation was not believed to be obtained in the latter case. The adsorption time could be as low as 30 to 60 min, also typical for desorption.

A measured adsorption/desorption characteristic is shown in Fig. 1. The actual measured adsorption flux for water was about 0.3 $\text{mg}/\text{cm}^2\text{-h}$, whereas that for ethanol was higher, at 0.9 $\text{mg}/\text{cm}^2\text{-h}$. The desorption flux for water was about 1.1 $\text{mg}/\text{cm}^2\text{-h}$, whereas that for ethanol was again higher, at 1.7 $\text{mg}/\text{cm}^2\text{-h}$. The difference between the water and ethanol rates can be most likely explained by their corresponding difference in molecular weights. Note that the desorption for water was observed to increase significantly upon heating at 100 $^{\circ}\text{C}$ to give 10.1 $\text{mg}/\text{cm}^2\text{-h}$ flux.

We hope to decrease the adsorption/desorption times to about 1 to 2 min for exposure at atmosphere, as opposed to liquid vapor pressure at room temperature, which may be more practical for a useful application. Initial reproducibility tests indicate that desorption is repeatable for ethanol, except for a base weight shift observed after multiple vapor exposures. This shift may be due to residues from the ethanol vapor and not from a change in the adsorption characteristic of the material.

Film Gas Transport

The time for gas transport through a porous silicon membrane is important for flow-through sensing applications to keep the sensing time realistic. Lower pressure transport across a membrane made with small pore material was first measured using liquid ethanol as a test vapor source. The membrane was exposed to vapor on one side of the membrane, and an additional porous silicon layer on silicon substrate on the other side of the membrane was used to monitor vapor transport by adsorption. The monitor wafer was removed after exposure and its weight increase measured on a balance. The transport time was determined by this method to be about 1 to 2 min for a 50- μm -thick membrane, with linear increase of adsorbed amount in the monitor for further exposure time.

Higher pressure transport measurements closer to atmosphere were then addressed. A test set-up was devised and assembled to permit pressurization of one side of a porous silicon membrane with nitrogen through a shut-off valve. The valve is then closed and

the pressure drop monitored with a pressure gauge. The minimum gas transport rate possible is about 10^{-4} cm³/min/psi, as limited by the leak rate of the set-up. The flow rate through a 2-mm-square membrane made with small pore material was measured to be linear with pressure and equal to about 10^{-2} cm³/min at 10 psi.

Film Fluid Transport

The time and amount of fluid transport are important for fluid flow applications. A test set-up was devised to permit filling of a flow line with liquid on one side of a membrane. The fluid is then pressurized and the amount of fluid transport is monitored by optical microscope observation on the other side of the membrane. Heating of the membrane to see its effect is done by exposure to a hot air gun or by use of an integral heater element adjacent to the porous silicon membrane. Measurements on actual membranes are planned.

Flow Rate Calculations

The gas or fluid flow rate through a porous silicon membrane can be simply estimated using the equation for flow velocity in the pores, appropriate for an incompressible fluid.⁴ The flow rate is then equal to the product of pore velocity, pore area and the number of pores. Assuming a pore diameter of 10 nm, a pore surface-to-volume ratio of 2.3×10^6 /cm, and a membrane geometry of 2 mm² with 45% conversion and 50 μ m thickness, the pore area is 7.8×10^{13} cm², and the number of pores is 1.3×10^{10} .

For air gas, the viscosity is 1.85×10^{-5} N-s/m², which gives a velocity of 2.3×10^{-2} cm/s for a pressure of 10 psi, or an air flow rate of 1.4×10^{-2} cc/min. Note that the calculated flow rate is quite close to that measured at 10^{-2} cc/min.

This result helps to justify the use of the equation of velocity for an incompressible fluid for a compressible gas.

For water fluid, the viscosity is higher, at 0.9×10^{-3} N-s/m², which gives a velocity of 4.7×10^{-4} cm/s at 10 psi or a water flow rate of 2.9×10^{-4} cc/min. For applications where about 1 nL volume is required, the pressure activation time is then 0.2 s, which is quite reasonable.

Microstructures: Membranes on Silicon and Pyrex

Flow-through gas sensing or fluid flow requires that the sense gas or fluid be drawn through a porous silicon element. A likely implementation of this element is a membrane on either silicon or pyrex substrates. The membrane would ideally be made from small diameter pore material, and be relatively thick to enhance adsorption sensitivity for gas sensing applications, for example.

A special fabrication procedure was developed to make the membranes on silicon, as shown in Fig. 2a. Membranes with small pore material were demonstrated, with a 5 mm $\times$ 5 mm area as well as a 2 mm $\times$ 2 mm area, both with 50 μ m thickness. The achievable conversion from crystalline to porous silicon ranged from 25 to 75%. No areas of optical transmission were visible under microscope view. Membranes with large pore material were also demonstrated.

Some bow of the membrane with small pores was observed after formation. The center deflection of the membrane ranged from about 60 μ m for the 5 mm area geometry to as little as 4 μ m for the 2 mm area. The bow is presumed due to compressive stress in the membrane, caused by native oxide growth as the oxide thickness is comparable to the dimension of the silicon fibers for the small diameter pore material.⁵ No bow was observed for membranes with large pores.

Figure 2. Porous silicon membrane structures fabricated on various substrates: (a) silicon and (b) pyrex. Electrode backside contact to silicon required for electrochemical etching is made directly in (a) and through holes in the pyrex in (b).

A special fabrication procedure was also devised to make membranes on pyrex, as shown in **Fig. 2b**. Tests of all fabrication steps indicate that membrane formation of large-diameter pore material using a KOH etch solution over a 5-mm diameter area at 50 μm thickness is realistic. More experiments to form the small-pore size material on pyrex substrates using electrochemical etching are needed.

Summary

Usable formation procedures for both small- and large-pore size porous silicon have been demonstrated. Significant adsorption has been measured on small-diameter pore material. Vapor transport at low pressure and gas transport at high pressure have been achieved as well. Test apparatus has been devised for high pressure gas and fluid transport. Fabrication procedures for porous silicon membranes on both silicon and pyrex substrates have been developed.

Future Work

More experiments are needed to complete characterization of basic properties for small-size porous membranes with small- as well as large-diameter pores. Further measurements on specific film properties, such as atmospheric pressure gas

and fluid transport, are planned. Longer term efforts to produce intermediate pore size material, which is more difficult to make, are on-going.

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