COMPOUND SEMICONDUCTOR FIELD-EFFECT TRANSISTORS WITH IMPROVED DC AND HIGH FREQUENCY PERFORMANCE

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COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTORS
WITH IMPROVED DC AND HIGH FREQUENCY PERFORMANCE

GOVERNMENT RIGHTS

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BACKGROUND OF THE INVENTION

FIELD OF INVENTION

This invention pertains to improving performance of compound semiconductor devices, generally, and more particularly to enhancing both DC and AC performance of field-effect transistor devices. In the preferred embodiment, carbon (C-ion) implants in gallium arsenide (GaAs)-based transistors are utilized both to sharpen the profile of a Si n-type channel and to minimize parasitic capacitances associated with implanted buried p-regions. Use of the invention allows for improved DC and AC (high frequency) functioning of metal semiconductor field effect transistors (MESFETs), junction field effect transistors (JFETs) and other similar devices.

DESCRIPTION OF THE RELATED ART

There has been an inherent trade-off between optimizing the DC and AC (high-frequency) performance of GaAs MESFETs or JFETs that incorporate a p-type implant below the n-type channel region. This trade-off relates to the need for a high implant dose
to realize good carrier confinement, and thus good DC performance (by minimizing short channel effects), and a low dose implant to minimize the gate-to-source capacitance ($C_{gs}$) from the resulting p/n junction at the bottom of the channel. Any increase in $C_{gs}$ will degrade the high-frequency performance by reducing both the unity gain cutoff frequency ($f_t$) and the maximum oscillation frequency ($f_{max}$). This problem becomes more severe as the gate length of the transistor is reduced since carrier confinement is more difficult to realize, thus requiring an increased dose for the buried p-implant that in turn will degrade the high-frequency performance.

The inherent conflict in optimizing both DC and high-frequency performance is illustrated in a study by K. Onodera, et al., (IEEE Trans. Electron Device, Vol. 38, No. 3, pp. 429 - 436, 1991). The authors there reported that in the case of two Be-implant doses used to form a buried p-region in GaAs MESFETs, the gate-to-source capacitance ($C_{gs}$) increased at the higher Be dose ($4 \times 10^{12}$ cm$^2$ compared to $2 \times 10^{12}$ cm$^2$ at 50 keV) thus degrading the unity current gain cutoff frequency ($f_t$) and the maximum oscillation frequency ($f_{max}$). The DC MESFET performance was enhanced by the high Be dose implant as demonstrated by a decrease in output conductance ($g_{ds}$), but high-frequency performance, for reasons stated above, diminished. Prior to the invention disclosed herein, one way of dealing with this situation has been to construct devices wherein the buried p-implant is completely depleted of free carriers to minimize the junction capacitance while achieving good electron confinement in the channel. For conventional p-type implants (Be or Mg),
however, neither the DC nor the high-frequency performance is optimized under this condition.

Figure 1 is presented in order to provide a foundation for later discussion regarding the application and utility of the invention. The figure illustrates in a simplified flow diagram the prior art with respect to the primary steps in the process sequence for an all implanted, self-aligned GaAs n-channel metal semiconductor field effect transistor (nMESFET). The overall method for fabricating a GaAs MESFET is well known (see, for example, J.P. de Souza and D.K. Sadana, IEEE Trans. Electron Dev., Vol. 39, pp. 166-175, 1992 or M.J. Howes and D.V. Morgan, eds., Gallium Arsenide: Materials, Devices, and Circuits, pp. 361-427). It should be understood, though, that an implanted MESFET is only one device in which the present invention has utility. The principles of C-ion implantation described in this patent will also apply to other semiconductor devices such as junction field effect transistors (JFETs), heterostructure field effect transistors (HFETs), and high electron mobility transistors (HEMTs). In addition, non-self-aligned transistor structures that incorporate an implanted channel region will also benefit from this invention.

Figure 1(a) depicts GaAs substrate material (5) onto which a photoresist (20) is patterned to define a region into which ions are to be implanted. First, according to the prior art, a buried p-region (10) is created by implanting \(^9\)Be or \(^{24}\)Mg ions using ion implantation methods well-known to those skilled in the art of semiconductor device manufacturing. An n-channel (15) is then implanted above the buried p-region, typically
using $^{28}\text{Si}$ ions. Referring now to Figure 1 (b), a gate metal contact (18) made from material such as tungsten, tungsten silicide, tungsten nitride or titanium nitride is deposited in contact with the n-channel previously deposited. (The figure depicts the situation in which the photoresist (20) is removed. The decision as to whether to remove or to repattern the photoresist will depend on the final configuration of layers desired with respect to any particular application. As with implantation, use of photoresist masking is well established and known to those practicing the art.) Figure 3(c) depicts a second implantation step performed using $^{29}\text{Si}$ ions to form the n$^+$ source (30) and drain (35) regions of the transistor. Following this step, and after the photoresist removal, the implants are all annealed (typically between 800 and 850°C for 10 to 60 seconds) to electrically activate the implanted species. Finally, as represented in Figure 3(d), ohmic source and drain contact metallization (40) is patterned, deposited and alloyed.

The role of the buried p-implant is to improve the confinement of electrons in the MESFET channel. Confinement is realized by sharpening the profile of the silicon channel implant and providing a n/p junction barrier to electron flow out of the bottom of the channel. The sharpening of the Si-channel implant is seen in simulated ion and carrier profiles such as are depicted in Figure 3 (which is discussed more in detail, below, in the Detailed Discussion). This sharpening typically is accomplished by implanting acceptor atoms such as Be or Mg in the region just below the Si-channel. A drawback associated with this practice, however, concerns the fact that many of those atoms come to rest beyond the tail
of the Si-channel and become active acceptors increasing $C_{gs}$ and robbing the device of its high-frequency efficiency. This problem, however, is overcome by the method of the present invention, wherein C-ions are implanted in the place of Be, Mg or other similar acceptor atoms.

Although the use of C to modify Si-implant profiles has been reported (B. P. Davies, P. Davies, D. M. Brookbands, D. J. Warner, and R. H. Wallis, "Anomalous Behavior of Carbon Implants in Si-Doped GaAs," *Int. Sum. GaAs and Related Compounds*, pp., 275-280, 1990; R. M. Gwilliam, R. J. Wilson, T. D. Hunt, and B. J. Sealy, The Use of Multi-Species Implantation for Carrier Profile Control in GaAs MESFETs Fabricated Using Silicon Ion Implantation," *Nucl. Instr. and Methods in Phys. Res.*, B74, pp. 94 - 97, 1993), the unique feature relating to enhanced high-frequency performance is new with this invention. These references point to the efficiency of carbon as a compensator when implanted in silicon-doped GaAs material, specifically with respect to compensating the tail of the Si-implanted channel to produce sharper channel profiles. It is also known that carbon has a low activation efficiency. An important feature of the present invention concerns the distinctive characteristic of C wherein it exhibits low activation as an implanted acceptor by virtue of the fact that it occupies an As-site within the GaAs substrate matrix. Furthermore, the prior art does not incorporate this principle in semiconductor device structures to enhance performance.
BRIEF SUMMARY OF THE INVENTION

The present invention utilizes carbon ion implantation to effect improvement in DC performance of GaAs-based and other compound semiconductor-based devices comparable to that seen by the formation of a buried p-region using the prior state-of-the-art method of implanting Group II p-type species (Be, Mg, Zn, or Cd). Improvements in AC (high-frequency) performance, compared to the prior art, are also achieved by virtue of the unique activation and compensation properties of carbon making it capable of minimizing parasitic capacitances associated with an implanted buried p-region. The invention makes use of unique properties of C-ions in that they have a low activation efficiency as acceptors when implanted alone in the region below the Si-channel. This low activation stems in part from the fact that, following implantation, C acceptors occupy As-sites rather than Ga-sites. As-vacancies have a higher energy of formation as compared to Ga-vacancies thus contributing to C having a lower activation efficiency than, for example, Be or Mg that occupy Ga-vacancies to become acceptors. At the same time, C-ions that overlap with the Si-channel profile will effectively compensate Si donors, particularly in the tail of the channel profile, and will sharpen the channel donor profile. This combination limits the gate-to-source capacitance associated with the n-channel/buried-p junction, minimizing any reduction in high-frequency operation, while still reducing the DC output conductance. The invention further contemplates implantation using species other than C, and compound
semiconductor substrates other than GaAs, so long as the other implant species and substrates conform to the principles detailed here wherein the implant species acts to compensate the n-channel tail, but does not significantly increase acceptor concentration in the buried p-region.

Accordingly, it is an object of the present invention to provide a method for manufacturing compound semiconductor transistor devices comprising the steps of providing a compound semiconductor substrate and co-implanting into said compound semiconductor substrate a first species comprising an electron donor and a second species comprising a weakly activated hole acceptor to form a n-channel having a profile which is modified by said second species functioning as an acceptor.

It is another object of the invention to provide a method of manufacturing compound semiconductor transistor devices where the compound semiconductor substrate comprises two or more different elements occupying distinct positions in a crystal matrix prior to implantation, and, following implantation, a first species occupies positions previously occupied predominantly by one element, and a second species occupies positions previously occupied predominantly by a different element.

It is another object of the invention to provide compound semiconductor transistor device comprising a compound semiconductor substrate and a first species comprising an electron donor and a second species comprising a weakly activated hole acceptor co-
implanted into said compound semiconductor substrate to form a n-channel having a profile which is modified by said second species functioning as an acceptor.

It is yet another object of the invention to provide a compound semiconductor device wherein the compound semiconductor substrate comprised two or more different elements occupying distinct positions in a crystal matrix prior to implantation, and, following implantation, a first implant species occupies positions previously occupied predominantly by one element, and a second implant species occupies positions previously occupied predominantly by a different element.

It is another object of the present invention to provide a method of field-effect transistor semiconductor device manufacture wherein a dopant is selected for implantation alone or in combination with other dopants which is capable of both actively compensating donor atoms in the n-channel region and exhibiting low activation efficiency in the p-region.

It is another object of the invention to provide a method for producing doped compound semiconductors for use in field effect transistor applications wherein carbon ions are implanted in order to sharpen the n-channel profile (thus enhancing carrier confinement) while not increasing C<sub>ns</sub> sufficiently to cause a significant diminishment of high frequency performance.

It is another object of the invention to utilize the unique activation characteristics of C-ions in GaAs enabling them to serve as active compensators when co-implanted with Si
in an n-region, but still exhibit low activation efficiency outside the presence of a significant amount of Si in a p-region.

It is another object to provide field effect transistor devices embodying the use of implanted carbon as a dopant rendering those devices capable of exhibiting good DC as well as good high-frequency performance.

It is another object to provide semiconductor devices wherein C is implanted at a dose within the range of $1.0 \times 10^{12} \text{ cm}^{-2}$ to $5.0 \times 10^{13} \text{ cm}^{-2}$.

It is another object to provide semiconductor devices wherein output conductance and sub-threshold current are reduced as compared with a transistor not comprising the second species.

It is another object to provide carbon-implanted devices wherein unit current gain cut-off frequency ($f_t$) is increased with respect to transistors implanted with comparable doses of Group II p-type species instead of carbon.

It is another object to provide carbon-implanted devices wherein maximum oscillation frequency ($f_{max}$) is increased with respect to transistors implanted with comparable doses of Group II p-type species instead of carbon.

Upon further study of the specification and appended claims, further objects and advantages of the invention will become apparent to those skilled in the art.

These objects have been attained by providing, in the preferred embodiment, a method of manufacturing compound semiconductor field effect transistor devices in which
C-ion implantation is utilized to effectively sharpen the n-channel profile while providing a means to reduce the p-type concentration below the n-channel thereby minimizing parasitic capacitances. These objects have further been attained by providing the semiconductor devices which embody this C-ion implant technology.

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**BRIEF DESCRIPTION OF THE DRAWINGS**

Figures 1 (a) through (d) illustrate prior art with respect to MESFET processing and together comprise a flow diagram showing steps used in manufacturing and all-implanted, self-aligned GaAs n-channel metal semiconductor field effect transistor (n-MESFET). These figures are provided to assist in understanding the utility of the present invention.

Figure 2 is a diagram illustrating the use of a combined implant to form the n-channel of a MESFET according to the principles of this invention.

Figure 3 is a graph showing simulated (TRIM92) ion and carrier profiles for a GaAs MESFET with either a C or Mg backside implant.

Figure 4 (a) - (d) is a series of graphs showing the relationship of \( I_{ds} \) versus \( V_{ds} \) for all-implanted GaAs nJFETs to demonstrate the DC performance of devices using the principles of the invention compared with that of devices using the prior state-of-the-art technology.

Figure 5 is a graph showing high-frequency performance metrics for all-implanted GaAs n-JFETs constructed using different Mg and C buried p-implants.
Carbon ($^{12}\text{C}$ or $^{13}\text{C}$) is unique among p-type dopants in GaAs in that it occupies an As-site to become an electrically active acceptor. All other p-type-only impurities (excluding the amphoteric dopants Ge, Si and Sn) in GaAs (Be, Mg, Zn and Cd) occupy a Ga-site to become active acceptors. Unlike other p-type species that typically have close to 100% activation in GaAs, implanted C in GaAs has a low activation efficiency of typically 50% or less (S. J. Pearton and C. R. Abernathy, Appl. Phys. Lett. 55, pp. 678 - 680, 1989). This is for two reasons: First, since C is a relatively low mass ion it generates fewer vacancies during implantation compared to heavier ions. Second, As-vacancies have a higher energy of formation than Ga-vacancies (R. W. Jansen and O. F. Sankey, Phys. Rev. B, Vol. 39, pp. 3192 - 3206, 1989) and, therefore, fewer As-vacancies will be available for the C-ion to occupy, resulting in a reduction in C’s activation efficiency as an acceptor.

The activation efficiency of implanted C can be increased by co-implanting a heavier ion to increase the lattice damage and thus the As-vacancy concentration. An example of co-implantation is implanting C along with Ga-ions thereby increasing the As-vacancy concentration both by the implantation bombardment itself and by altering the local stoichiometry of the crystal. Similarly, when C is co-implanted with Si, the Si implant will create additional As-vacancies thus allowing the C-ion to occupy an As-site and act as an acceptor atom. In the Si/C case, since the Si-ion will occupy a Ga-site to become a donor atom (Si$_{Ga}$) and the C will occupy an As-site to become an acceptor atom (C$_{As}$), the region
of Si/C co-implantation will be partially or completely compensated (electron concentration
\[ n = N(Si) - N(C) \] for \( N(Si) > N(C) \). In the region where Si-ions have not been
implanted, as in the MESFET below the Si-channel implant, the C-ions will not have
additional As-vacancies to occupy and the activation efficiency will be diminished. This
combination of activation properties makes C ideal for compensating the tail of a Si-channel
implant while at the same time minimizing the concentration of activated acceptors below
the channel. The minimization of the p-type region is critical to minimizing \( C_W \) and
improving the high-frequency performance of the transistor.

Figure 2 is similar to Figure 1(a) in that it depicts the step of depositing the n-
channel during semiconductor processing. Figure 2 goes beyond the prior art, though, to
illustrate the use of a combined implant according to the best mode of this invention. \(^{29}\)Si
and \(^{12}\)C are co-implanted in order to create a Si-ion (donor) -doped n-channel (15') modified
by the C-ions and a lightly-doped p-region (10') containing C-ions beneath the n-channel.
The C-ion implantation according to this technique achieves the objects of the invention
because of the favorable attributes of carbon with regard to its low activation efficiency as
an acceptor when implanted alone and its improved activation efficiency when a co-
implantation is performed. It should be understood, however, that the invention
encompasses the implantation of any dopant which exhibits implant activation properties
similar to those described for C. It is contemplated that ions or ion combinations which
include atoms other than \(^{12}\)C or \(^{13}\)C, alone, will serve this purpose and will fall within the
scope or the claimed invention. Likewise, the scope of the invention is not intended to be limited to use in GaAs semiconductor devices, but rather to include other forms of compound semiconductors for which the principles disclosed here are applicable.

Figure 3 depicts in a graphical format data showing sharpening of the Si-channel implant profile using different types of p-implants. The data shown are TRIM92 simulated ion and carrier profiles for a GaAs MESFET comparing C (95 keV, 3 \times 10^{12} \text{ cm}^{-2}) and Mg (150 keV, 3 \times 10^{12} \text{ cm}^{-2}) backside implants using standard ion implantation techniques known to those skilled in the art. (See J.F Siegler, J. P. Biersack, U. Littmark The Stopping and Range of Ions in Solids, Vol. 1, p. 202, Pergamon Press, New York, 1985, for a discussion of TRIM92 simulations.) Curve A is the simulation of the Si-ion implant profile for a 70 keV, 2 \times 10^{13} \text{ cm}^{-2} \text{Si-channel implant}. Curve B represents the difference of the Si-implant profile and the C-implant (95 keV, 3 \times 10^{12} \text{ cm}^{-2}) profile \( N(\text{Si}_\text{Ga}) - N(\text{C}_\text{As} \text{ 100\% activation}) \) and will correspond to the final electron profile (n) for the channel neglecting dopant diffusion, implant channeling, and depletion effects. Implant channeling, in particular, will make the initial Si-channel profile broader, therefore benefiting even more from the profile tailoring effect of the buried p-implant. By realizing enhanced carrier confinement in the channel, transistor modulation is improved by reducing the off-state leakage (reduced sub-threshold currents) and on-state conductance (reduced output conductance, \( G_{ds} \)). Sharpening of the implanted Si channel profile is accomplished by introducing activated acceptor atoms in the same region as the Si-channel tail thereby...
compensating some or all the Si-donors in that region. Prior to this invention, this channel
sharpening was accomplished by implanting Be or Mg ions with a projected range equal to
two to three times the projected range of the Si-channel implant. While such Be or Mg
implants are effective in modifying the Si-channel profile, some portion of the implanted Be
or Mg ions came to rest beyond the tail of the Si-channel (see Curve D in Figure 2 for p =
\(N(M_{Ga} \text{ 100\% activation}) - (N(Si_{As}) \text{ for } N(M_{Ga}) > N(Si_{As})\) with a Mg implant of 150 keV, 3 \(x 10^{12} \text{ cm}^{-2}\) and do not contribute to compensating the Si-donors, but rather, become active
acceptors with close to 100\% activation efficiency. The acceptor atoms beyond the Si-
channel tail form a buried p-region and increase the gate-to-source capacitance (\(C_{gs}\)) by
creating a n/p junction at the bottom of the channel. Increasing \(C_{gs}\) will degrade the
transistor high-frequency performance, as described later, and is the reason the present
invention improves on the state-of-the-art wherein Be or Mg implantation is done. By using
C implantation to modify the Si-channel profile, as described in detail below, the increase in
\(C_{gs}\) is reduced and the high-frequency performance is enhanced over a similarly Be or Mg
implanted device. The reduction in \(C_{gs}\) with a C-implanted device is a result of the lower
activation efficiency of C in the region below the Si-implanted channel as simulated in
Figure 2, curve C (\(p = N(C_{As} \text{ 50\% activation}) - N(Si_{As}) \text{ for } N(C_{As}) > N(Si_{As})\)) where a 50\%
activation efficiency for C is assumed.

The relationships between \(f_{t}\) and \(f_{max}\) and MESFET parasitics are
\[ f_t = \frac{g_{mi}}{2\pi(C_{gs} + C_{gd})} \]  

and

\[ f_{\text{max}} = \frac{f_t}{2[G_{ds}(R_s + R_g) + 2\pi f_t C_{gs} R_g]^{1/2}} \]

where \( g_{mi} \) is the intrinsic transconductance, \( C_{gs} \) is the gate-to-source capacitance, \( C_{gd} \) is the drain-to-gate capacitance, \( G_{ds} \) is the output conductance, \( R_s \) is the gate resistance, and \( R_g \) is the source resistance. It can be shown from Equations 1 and 2 that any increase in \( C_{gs} \) will degrade both \( f_t \) and \( f_{\text{max}} \). In addition, to realize a high \( f_{\text{max}} \), the output conductance (\( G_{ds} \)) must also be minimized while maintaining a high \( f_t \). This further demonstrates the significance of this invention and its ability to relax the design trade-off between DC performance (minimizing \( G_{ds} \)) and AC performance (maximizing \( f_t \) and \( f_{\text{max}} \)) for a buried p-implant dose.

The utility of the invention has been demonstrated in the DC and high-frequency performance of a self-aligned, all ion implanted, GaAs nJFET by comparing a Mg-implanted buried p-layer to a C-implanted buried p-layer. Two implant doses were studied for the buried p-region: \( 1.5 \times 10^{12} \) cm\(^{-2} \) and \( 3 \times 10^{12} \) cm\(^{-2} \). Mg implants were done at 210 keV and the C-implants were done at 95 keV. The Si-channel implant dose was varied for each device to give a threshold voltage of approximately 0.25 V. The need for different channel implants for the different backside implants is a result of the different activation and
depletion properties of the two implant species. Table 1 summarizes the DC performance of the four 0.5 μm nJFETs. To account for slight differences in the threshold voltage of the devices, the transconductance ($g_m$) and the saturation current ($I_{sat}$) are reported at a set voltage above threshold ($V_{gs} - V_{th} = 0.8V$). The DC results in Table 1 are comparable for nJFETs with the same buried p-implant dose independent of the species, Mg or C.

Figure 4 (a) - (d) shows $I_{ds}$ versus $V_{ds}$ (DC JFET performance) for the four backside conditions summarized in Table 1. (Figure 4(a) depicts data for Mg at $1.5 \times 10^{12}$, Figure 4(b) depicts data for C at $1.5 \times 10^{12}$, Figure 4(c) depicts data for Mg at $3.0 \times 10^{12}$, and Figure 4(d) depicts data for C at $3.0 \times 10^{12}$.) The transconductances and saturation currents are comparable for JFETs with the same backside implant dose independent of the implant species. The high dose backside implant JFETs have low output conductance (6 to 9 mS/mm) and sub-threshold slopes (80 to 90 mV/decade) indicative of good channel confinement for these nominally 0.5μm gate length devices.

### Table 1

<table>
<thead>
<tr>
<th>Buried p-implant (Mg @ 210 keV, C @ 95 keV)</th>
<th>Channel implant dose ($\times 10^{13}$ cm$^{-2}$)</th>
<th>$V_{th}$ (V)</th>
<th>$I_{sat}$ (mA/mm)</th>
<th>$g_m$ (mS/mm)</th>
<th>$g_{ds}$ (mS/mm)</th>
<th>sub-threshold slope (mV/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mg: $1.5 \times 10^{12}$</td>
<td>1.2</td>
<td>0.18</td>
<td>94</td>
<td>242</td>
<td>26</td>
<td>200</td>
</tr>
<tr>
<td>C: $1.5 \times 10^{12}$</td>
<td>1.2</td>
<td>0.30</td>
<td>99</td>
<td>248</td>
<td>15.5</td>
<td>110</td>
</tr>
<tr>
<td>Mg: $3.0 \times 10^{12}$</td>
<td>1.6</td>
<td>0.23</td>
<td>100</td>
<td>201</td>
<td>6.2</td>
<td>80</td>
</tr>
<tr>
<td>C: $3.0 \times 10^{12}$</td>
<td>1.3</td>
<td>0.20</td>
<td>98</td>
<td>209</td>
<td>9.0</td>
<td>90</td>
</tr>
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</table>
Figure 5 shows the high-frequency performance metrics (\(f_t\) and \(f_{\text{max}}\)) for the four nJFETs of Table 1. The C-implanted JFETs demonstrate enhanced high-frequency performance over the Mg-implanted devices in all cases. The C-implanted JFET with the high dose (\(3 \times 10^{12} \text{ cm}^2\)) demonstrates a 28% increase in \(f_t\) (to 28.3 GHz @ \(V_{GS} = 1\) V) and a 46% increase in \(f_{\text{max}}\) (to 43.2 GHz @ \(V_{GS} + 0.8\) V) over the comparable high dose Mg-backside JFET. In comparison to the lower dose backside implanted JFETs, the higher dose C-implanted JFETs showed less degradation in \(f_t\) (-6.3% @ \(V_{GS} = 1.0\) V) with an enhancement in \(f_{\text{max}}\) (+11.6% @ \(V_{GS} = 9.8\) V) while the Mg-implanted devices degraded sharply for the higher dose implant (-23.5% in \(f_t\) @ \(V_{GS} = 1.0\) V and -16.8% in \(f_{\text{max}}\) @ \(V_{GS} = 0.8\) V). The improvement on \(f_{\text{max}}\) for the C-backside sample is a result of the reduced output conductance (\(G_{ds}\)) without an appreciable increase in the gate-to-source capacitance as described below.

### Table 2

<table>
<thead>
<tr>
<th>Buried p-implant (Mg @ 210 keV, C @ 95 keV)</th>
<th>(C_{pd}) (fF/mm)</th>
<th>(C_{ds}) (fF/mm)</th>
<th>(C_{gs}) (fF/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mg: (1.5 \times 10^{12})</td>
<td>247</td>
<td>386</td>
<td>750</td>
</tr>
<tr>
<td>C: (1.5 \times 10^{12})</td>
<td>262</td>
<td>375</td>
<td>786</td>
</tr>
<tr>
<td>Mg: (3.0 \times 10^{12})</td>
<td>236</td>
<td>450</td>
<td>984</td>
</tr>
<tr>
<td>C: (3.0 \times 10^{12})</td>
<td>226</td>
<td>345</td>
<td>829</td>
</tr>
</tbody>
</table>

The reason for the enhanced performance of the C-implanted devices is evident from the extracted JFET capacitances summarized in Table 2. For the high dose JFETs,
the C-backside JFET has 4.2% lower gate-to-drain capacitance ($C_{gd} = 226 \text{ fF/mm}$), 23.3% lower drain-to-source capacitance ($C_{ds} = 345 \text{ fF/mm}$) and 15.8% lower gate-to-source capacitance ($C_{gs} = 829 \text{ fF/mm}$) compared to the high dose Mg-backside JFET ($C_{gd} = 236 \text{ fF/mm}$, $C_{ds} = 450 \text{ fF/mm}$, and $C_{gs} = 984 \text{ fF/mm}$) at a gate bias of 1V. We ascribe this reduced capacitance and increased high-frequency performance to the fewer activated C acceptors, compared to Mg, below the channel in the C-backside JFET. The lower acceptor concentration creates less channel depletion with more depletion of the p-side of the n-channel/buried-p junction for a net larger depletion region and a corresponding reduction in junction capacitance ($C_{j}$). The reduced channel charge depletion is also evident in the lower channel dose required in the C-backside compared to the Mg-backside JFET for the same threshold voltage (see Table 1).

These results comparing Mg-implanted to C-implanted JFETs clearly demonstrate the advantage of the invention over the previous state-of-the-art. In particular, a 28% increase was demonstrated in $f_t$ and a 43% increase was demonstrated in $f_{max}$ for the C-implanted device over the Mg-implanted device with equal or better DC performance ($G_{ds}$ and sub-threshold slope). It is important to also note that the invention is compatible with existing GaAs MESFET production techniques. Therefore, insertion of the new method will have limited impact on the other aspects of the process while giving significant performance improvements, particularly for sub-micron and deep sub-micron gate length devices.
Having thus described the invention, it will be obvious to those of ordinary skill in the art that various modifications can be made within the spirit and scope of the present invention. It is intended to encompass all such variation as fall within the spirit and scope of the invention.
ABSTRACT OF THE DISCLOSURE

A method for making compound semiconductor devices including the use of a p-type dopant is disclosed wherein the dopant is co-implanted with an n-type donor species at the time the n-channel is deposited. Also disclosed are devices manufactured using the method. In the preferred embodiment n-MESFETs and other similar field effect transistor devices are manufactured using C ions implanted with Si atoms in GaAs to form an n-channel. C exhibits a unique characteristic in the context of the invention in that it exhibits a low activation efficiency (typically, 50% or less) as a p-type dopant, and consequently, it acts to sharpen the Si n-channel by compensating Si donors in the region the Si-channel tail, but does not contribute substantially to the acceptor concentration in the region of the buried p-implant. As a result, the invention provides for improved field effect transistor devices with enhancement of both DC and high-frequency performance.
Figure 1
(Prior Art)
FIGURE 2
FIGURE 3

![Graph showing ion concentration versus depth (Å). The graph plots logarithmic scales for both axes, with depth in Å and ions (carriers)/cm³. Four lines labeled A, B, C, and D are shown, each representing different concentrations at various depths.](image-url)
Figure 5

- $f_r$: C (low)
- $f_{max}$: C (low)
- $f_r$: Mg (low)
- $f_{max}$: Mg (low)
- $f_r$: C (high)
- $f_{max}$: C (high)
- $f_r$: Mg (high)
- $f_{max}$: Mg (high)

Frequency (GHz) vs. $V_{GS}$ (V)