SAN097-0062C

DIRECT OBSERVATION OF MOBILE PROTONS IN SiO_2 THIN FILMS: POTENTIAL APPLICATION IN A NOVEL MEMORY DEVICE

SAND--97-0062C

K. VANHEUSDEN*, W. L. WARREN*, R. A. B. DEVINE**, D. M. FLEETWOOD*,
J. R. SCHWANK*, P. S. WINOKUR*, Z. J. LEMNIOS***
*Sandia National Laboratories, Albuquerque, New Mexico 87185-1349
**France Télécom-CNET, B.P. 98, 38243 Meylan, France
***Defense Advanced Research Projects Agency, Arlington, VA 22203-1714

CONF-961202--25

ABSTRACT

In this work we show that annealing of silicon/silicon-dioxide/silicon structures in forming gas (N_2:H_2; 95:5) above 500°C leads to spontaneous incorporation of mobile H^+ ions in the buried SiO_2 layer. We demonstrate that, unlike the alkali ions feared as killer contaminants in the early days, the space charge distribution of these mobile protons within the buried oxide layer can be very well controlled and easily rearranged with relatively high speed at room temperature. The hysteresis in the flat band voltage shift provides a unique vehicle to study proton kinetics in silicon dioxide thin films. It is further shown how this effect can be used as the basis for a reliable nonvolatile FET memory device that has potential to be competitive with state-of-the-art Si-based memory technologies. The power of this novel device is its simplicity; it requires few processing steps, all of which are standard in Si integrated-circuit fabrication.

INTRODUCTION

The incorporation of atomic or molecular hydrogen into the technologically relevant Si/SiO_2 system is almost unavoidable during device processing. Hydrogen is present at the Si/SiO_2 interface, terminating dangling Si bonds (P_b centers [1]), and in the SiO_2 film, either bonded to the network (Si-OH) or in molecular form at interstitial sites (H_2, H_2O). Hydrogen is often introduced deliberately by annealing in an H_2 containing ambient to passivate interface traps. Negative effects may also result from the presence of hydrogen; post irradiation buildup of interface traps is assumed to be due to the interaction of radiation induced holes with hydrogen present in the SiO_2 layer, resulting in protons which drift to the interface where they can react with interfacial Si-H to form an interface trap [2]. The H and D isotope experiments of Saks and Rendell [3] have confirmed the involvement of hydrogen in the creation of interface traps following ionizing radiation. However, a clear understanding of proton transport kinetics and chemistry in the oxide layer is still lacking. For novel device structures or materials, the interactions with hydrogen are of great technological interest and are often surprising and complex. This is certainly the case for silicon-on-insulator (SOI) technology.

In the following, we explore the effects of annealing SOI, and even more generally, $Si/SiO_2/Si$ structures, in a hydrogen containing ambient over a wide temperature range. It is demonstrated that between 500 and 800 °C these forming-gas anneals introduce mobile H^+ ions into the buried SiO_2 layer of $Si/SiO_2/Si$ structures. Changes in the H^+ charge distribution within the buried SiO_2 layer were directly monitored by capacitance voltage and current-voltage measurements. These experiments enable us to directly observe proton drift in SiO_2 thin films, and thus study proton kinetics and chemistry. It is further demonstrated that this effect has great potential for application in a nonvolatile FET (NVFET) microelectronic memory device.

EXPERIMENTAL TECHNIQUES

Sample preparation

A variety of $Si/SiO_2/Si$ materials was investigated. One common feature is that they all were subjected to a high-temperature treatment (1100-1325 °C), prior to the forming gas anneals at much lower temperatures. Separation by implantation of oxygen (SIMOX) material was

DISCLAIMER

studied, formed by implanting a *p*-type Si(100) substrate with 190-keV O^+ ions to a dose of 1.8×10^{18} cm^{-2} followed by a subsequent anneal for 6 hours at 1325 °C in Ar + 1% O_2. This resulted in a 200-nm monocrystalline Si layer on top of a 400-nm buried amorphous SiO_2 layer. Another set of SOI samples was made by first growing a 1-μm thermal oxide, then covering this with a 330-nm thick layer of polycrystalline Si, which was subsequently zone-melt recrystallized (ZMR). Unibond® material was also investigated. This novel SOI material is formed by implanting hydrogen (~ 6×10^{17} cm^{-2}) into a wafer, below a thermally grown SiO_2 layer (300 nm thick), followed by bonding this wafer to another wafer. This bonding involves a low temperature anneal at 400-600 °C to split the first wafer at the boundary defined by the implant, followed by a high temperature anneal at 1100 °C to strengthen the bonding interface. Apart from these SOI materials we also studied standard thermal SiO_2 (40 nm thick) capped with a poly-Si layer (1-μm thick), chemical-vapor-deposited and annealed at 1200 °C for 2 h in Ar + 1% O_2.

To reduce leakage currents at the substrate edges and through the buried oxide layer during the top Si conductivity measurements, and to facilitate lateral diffusion of hydrogen into the buried oxide during the forming gas anneal, small islands of the top Si layer were created by etching the wafers in a HNO_3-CH_3COOH-HF mixture using a mask, which leaves behind small isolated strips (1 mm × 3 mm) of top Si layer. Lateral diffusion of hydrogen into the buried oxide is crucial because the amount of hydrogen reaching the buried oxide by diffusion through the top *c*-Si layer is negligible, due to the very low solubility of hydrogen in Si [4]. Forming-gas [N_2:H_2; 95:5 (by volume, 99.999% pure)] and nitrogen (N_2 99.999% pure) anneal treatments were performed for 30 min inside a quartz tube that was inserted into a tube furnace (200-1000 °C). After the anneal the samples were pulled out and quenched to room temperature in air.

Analysis techniques

Drain current-gate voltage (I_D-V_G) measurements on the resulting Si/SiO_2/Si structures were performed using the point-contact transistor method [5]. This simple test "device" is based on the upside-down MOS structure using the specific SOI configuration as shown in the inset in Fig. 1; the buried oxide plays the role of the gate oxide and the top Si layer represents the transistor body. Two metal probe tips are placed on the top Si layer to form the source and drain point contacts (V_D = 0.2 V), while the gate voltage (V_G) is applied to the back of the Si substrate.

Capacitance-voltage (*C*-*V*) measurements at 1 MHz were also performed. Gate contacts were formed using Al dots or a Hg probe, after removing the top-Si islands in KOH solution.

RESULTS AND DISCUSSION

Fundamental Characterization

Figure 1 shows the hysteresis in the I_D-V_G curves on SIMOX after it received a 550 °C forming gas anneal. Curve 1 was recorded with a *decreasing* gate (substrate) bias (from positive to negative). Subsequently, curve 2 was recorded using an *increasing* gate voltage sweep (from negative to positive). Both curves were recorded at room temperature after keeping the gate at the initial bias value for 5 min. Curve 3 was recorded after curve 2 using the same procedure as described for curve 1, showing the total reversibility of the process. We will use the term *hysteresis* in this work to describe the reversible shift of the I_D-V_G curve along the voltage axes by reversing the voltage sweep direction.

As can be seen from Fig. 2, similar features were observed for devices on the other SOI materials such as Unibond as well as standard poly-Si capped thermal oxides, following a 600 °C forming gas anneal. The observed hysteresis in the I_D-V_G curves is the result of an electric field induced migration of a charged ionic species from one Si/SiO_2 interface to the other [6]. The negative sign of the voltage shift ΔV_{FB} shows that the migrating ions are positive. The density

($\approx 2 \times 10^{12}$ cm^{-2}) was found to be rather independent of buried oxide thickness, suggesting that the mobile ionic species are generated at the interface rather than in the bulk.

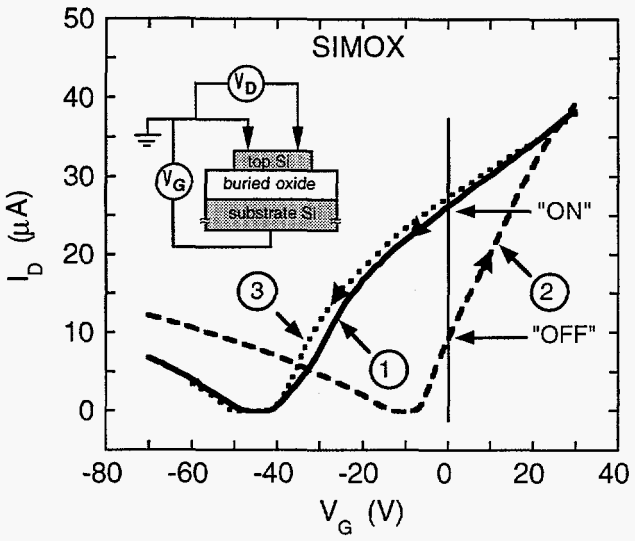

FIG. 1. I_D-V_G hysteresis measured on SIMOX after a 550 °C forming-gas anneal. The I_D-V_G curves were measured using a point-contact FET device as shown schematically in the inset. Curve 1 was recorded sweeping the gate bias from positive to negative. Curve 2 was recorded after curve 1 using the opposite gate voltage sweep direction. Curve 3 was recorded after curve 2 using the same sweep as for curve 1.

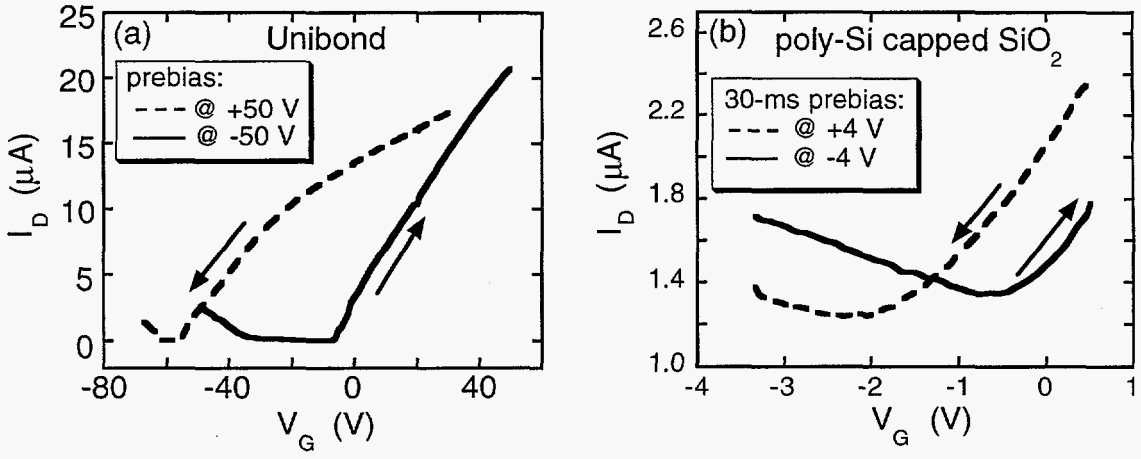

FIG. 2. I_D-V_G hysteresis measured on 300-nm thick Unibond (a) and 40-nm poly-Si capped thermal SiO_2 (b) after a 600 °C forming-gas anneal. The I_D-V_G curves were obtained as in Fig. 1.

Figure 3 plots the amount of hysteresis (i.e., mobile ions) as a function of isochronal anneal temperature in forming gas and in pure nitrogen. The data were obtained using point-contact devices on a SIMOX substrate. It shows that the hysteresis effect occurs over the temperature range from 500 to 800 °C. Figure 3 also shows that the effect is much stronger when hydrogen is added to the anneal ambient, with a pronounced peak at 600 °C. This shows that the presence of hydrogen in the anneal ambient is the cause of the hysteresis; it is due to the incorporation of mobile H^+ ions into the buried SiO_2, as has been demonstrated elsewhere [7], not to alkali ion

contaminants [6]. The much weaker effect observed when a pure N_2 ambient is used, is attributed to contamination from hydrogenous species present in the substrate or in the quartz furnace tube.

If the top Si layer is removed and a MOS capacitor is formed to perform *C-V* measurements, it is observed that the charged species escape the SiO_2 dielectric through the metal gate under negative gate bias. Given the much higher solubility of hydrogen in metal capacitor gates such as Al or Hg as compared to Si [8], this observation provides additional evidence that the mobile charge is H^+.

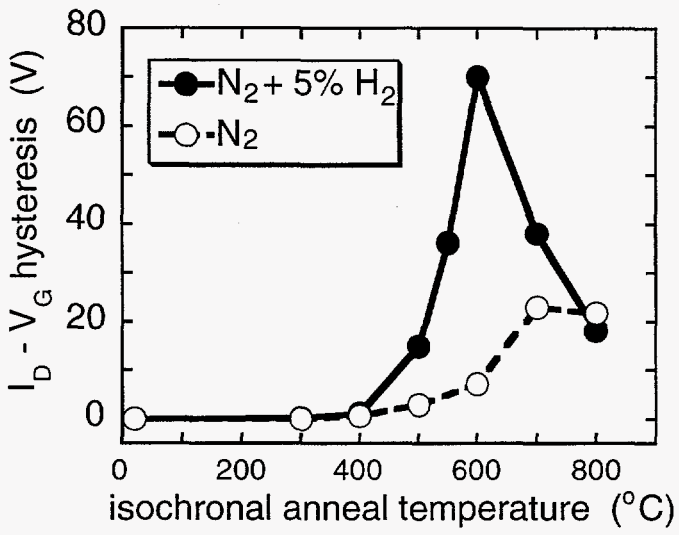

FIG. 3. Amount of I_D-V_G hysteresis as a function of isochronal anneal temperature in forming gas and in pure nitrogen. The I_D-V_G curves were measured with point-contact FET devices on SIMOX substrate material.

By analyzing the kinetics of charge migration as a function of time, gate voltage (V_G), oxide thickness (d), and temperature (T), as described in detail in an earlier work [7], it was found that the H^+ drift in the buried oxide is best described as space-charge-limited current [8,9]:

$$\frac{\Delta Q_{H^+}}{\Delta t} = J_{H^+} \propto \frac{V_G^2}{d^3} \mu_{H^+}, \qquad (1)$$

where $\Delta Q_{H^+}/\Delta t$ is the rate of decrease in the charge density accumulated at the top-Si/SiO_2 interface, J_{H^+} is the space charge limited ionic current density through the SiO_2 layer, and μ_{H^+} is the ionic mobility. The activation energy $E_a \approx 0.8$ eV for H^+ and D^+ drift, was derived from an Arrhenius plot, and found to be in good agreement with the expected drift behavior of H^+ and D^+ in standard thermal SiO_2 thin films [10].

Next, we discuss the proposed mechanism causing the incorporation of mobile H^+ ions in the buried SiO_2 layer of these Si/SiO_2/Si materials during the FG anneal. It is known that the high-temperature (1200-1325 °C) formation anneal step creates neutral O vacancies (Si-Si bonds) in the buried oxide via O out-diffusion from the SiO_2 into the top and substrate Si layers [11]. Because these strained Si-Si bonds can act as H_2 cracking sites [12] in the buried SiO_2, they are catalyst sites for the generation of atomic hydrogen. At a Si/SiO_2 interface a neutral H can either a) dimerise with a H passivating a dangling Si bond, resulting in a mobile H_2 molecule and an interface trap [1], or b) release its electron to the Si conduction band by interaction with the O in a Si-O-Si bridging bond. In the latter case a "free" H^+ results. Since the solubility of

hydrogen species in *c*-Si is low, once formed, the H^+ is confined in the buried SiO_2 layer, sandwiched between the two encapsulating Si layers; i.e., the interfaces form a diffusion barrier.

Application in a Memory Device

It is easy to see how the hysteresis effect observed in this work could be utilized in a nonvolatile FET memory device. An n-channel transistor can be changed to "normally on" or "normally off" by applying a positive or negative gate (substrate) bias which will drift the protons to the top-Si/SiO_2 or substrate-Si/SiO_2 interface, respectively. For a memory device this can be interpreted as writing the device to a bit state "1" or "0". To read the device, the zero bias drain current I_0 is simply measured (high current then corresponds to logic state "1", low current to "0"), as visualized in Fig. 1.

For memory devices, a short write time is desirable. It follows from Eq. 1 that the device speed will be proportional to V_G^2 and d^{-3}. For test devices fabricated using a poly-Si-capped 40-nm thermal oxide substrate, a write time of about 50 ms could easily be attained (write/erase voltage $V_G = \pm$ 4 V) at room temperature (see Fig. 2 b). Write times as fast as 1 ms can be extrapolated using Eq. 1 for 10-nm thermal oxides.

Fatigue characteristics on point-contact FETs using SIMOX substrate material are shown in Fig. 4 (a). Fatigue tests were performed by applying an alternating V_G, continuously drifting the protons from interface to interface at room temperature. The data show that the device easily endures over 10^4 write-erase cycles without any significant change in the flat-band voltage hysteresis. The I_D-V_G curves in the inset of Fig. 4 (a) further confirm that no degradation (proton loss, changes in current-voltage characteristics) occurred after subjecting the device to 10^4 write/erase cycles.

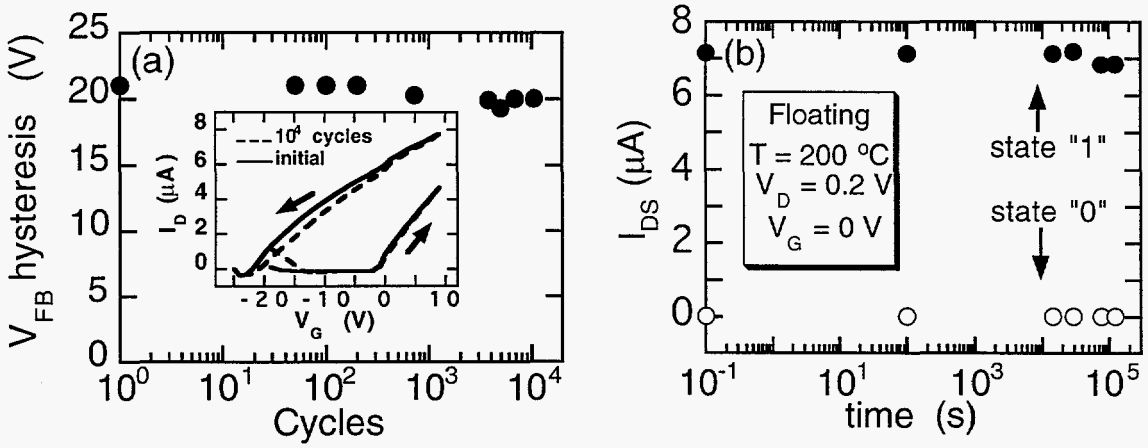

FIG. 4. Fatigue (a) and retention (b) behavior for memory test devices fabricated using point-contact FETs on SIMOX (a) and ZMR (b) substrate material. The devices were hydrogenated or deuterated at 600 °C. The inset in (a) compares the initial I_D-V_G curve to curves after 10^4 write/erase cycles.

The charge retention characteristics of a memory device fabricated on ZMR substrate material are illustrated in Fig. 4 (b). Retention tests were performed by drifting the protons to the top-Si/SiO_2 (state "1") or substrate-Si/SiO_2 (state "0") interface, followed by heating the device to 200 °C at floating gate for extended times. The zero bias drain current was monitored (at room temperature) for various anneal times. No instabilities in the initial I_D-V_G characteristic could be observed for anneal times up to 25 h. This is a very important observation as it is in contrast with the classical picture of instabilities associated with mobile ion contaminants in SiO_2 [6].

This NVFET device has potential advantages over state-of-the-art nonvolatile memory technologies such as Flash and EEPROM. While its speed, retention and lifetime performance are expected to be competitive with these existing technologies, it is simpler in design, requires fewer processing steps, can potentially operate at much lower voltages, and can be built using standard FET processing.

SUMMARY AND CONCLUSIONS

In summary, we find that annealing high-temperature-processed $Si/SiO_2/Si$ substrates in forming-gas in the 500-800 °C range introduces mobile H^+ ions which are imprisoned in the buried SiO_2 layer. The charge distribution of these species in the oxide is both stable and easily rearranged by applying an external field. From a fundamental point of view, this phenomenon offers a unique probe to study proton kinetics and reactions in the Si/SiO_2 system. From an applied point of view it has potential for application in the design of a new generation of nonvolatile memories.

ACKNOWLEDGMENTS

We would like to thank Craig Keast at MIT Lincoln Labs for the thermal oxide samples. The part of this work performed at Sandia National Laboratories was supported by the US Department of Energy under contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the US Department of Energy.

REFERENCES

[1] K. L. Brower, Phys. Rev. B **42**, 3444 (1990).
[2] F. B. McLean, IEEE Trans. Nucl. Sci. **NS-27**, 1651 (1980).
[3] N. S. Saks and R. W. Rendell, Appl. Phys. Lett. **61**, 3014 (1992).
[4] B. L. Sharma, in Diffusion in Semiconductors (Trans. Tech. Pub., Germany, 1970) p. 87.
[5] S. Cristoloveanu and S. S. Li, in Electrical characterization of silicon-on-insulator materials and devices (Kluwer Academic Publishers, Boston, MA, 1995) p.104.
[6] E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah, J. Appl. Phys. **36**, 1664 (1965).
[7] K. Vanheusden, W. L. Warren, D. M. Fleetwood, J. R. Schwank, M. R. Shaneyfelt, P. S. Winokur, R. A. B. Devine, and Z. J. Lemnios, (in press, 1997)
[8]. S. M. Sze, in Physics of Semiconductor Devices (John Wiley & Sons, NY, 1981).
[9] B. Jayant Baliga, in Modern Power Devices (John Wiley & Sons, NY, 1987) p.149.
[10] P. S. Winokur, H. E. Boesch, J. M. McGarrity, and F. B. McLean, IEEE Trans. Nucl. Sci. **NS-24**, 2113 (1977).
[11] R. A. B. Devine, W. L. Warren, J. B. Xu, I. H. Wilson, P. Paillet, and J.-L. Leray, J. Appl. Phys. **77**, 175 (1995).
[12] R. A. B. Devine, J.-L. Leray, and J. Margail, Appl. Phys. Lett. **59**, 2275 (1991).