M96015013

SAN096.2216C

August 1, 1996

CONF-961180--3

SAND-96-2216C

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Presented at the ASM International Symposium
for Testing and Failure Analysis, November 1996

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Failure Analysis of a Half-Micron CMOS IC Technology

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Abstract

We present the results of recent failure analysis of an advanced, 0.5 μm , fully planarized, triple metallization CMOS technology. A variety of failure analysis (FA) tools and techniques were used to localize and identify defects generated by wafer processing. These include light (photon) emission microscopy (LE), fluorescent microthermal imaging (FMI), focused ion beam cross sectioning, SEM/voltage contrast imaging, resistive contrast imaging (RCI), and e-beam testing using an IDS-5000 with an HP 82000. The defects identified included inter- and intra-metal shorts, gate oxide shorts due to plasma processing damage, and high contact resistance due to the contact etch and deposition process. Root causes of these defects were determined and corrective action was taken to improve yield and reliability.

Failure Analysis - A Key Element in Advanced IC Technology Development

One of the primary goals of advanced IC technology development is to determine and integrate tools and processes for fabrication of ICs with reduced dimensions. Defect identification and reduction is one of the most important tasks in achieving this goal. Defect reduction ultimately improves yield and reliability, reduces manufacturing cost, and increases the bottom line - profit for IC producers.

The use of new tools and their integration into fabrication processes often result in systematic defects

which cause yield loss and potential reliability problems. Thus, systematic yield limiting factors and defects need to be eliminated early in the development cycle before the initiation of production. In fact, many high quality manufacturers strictly demand that new wafer fabrication processes introduced by either on-site development or technology transfer has to reach a stable and reasonable yield and reliability before accepting them for manufacturing [1].

We present the results of failure analysis during the development of an advanced submicron CMOS technology. We describe in detail how the defects responsible for gross yield losses were identified and what specific FA tools were used for the identification. Root causes of these defects were subsequently determined. Corrective action was taken that improved yield and reliability.

Several systematic defects were identified during early process development. These included high percentage of interconnect defects causing inter- or intra-metal shorts, extensive gate oxide breakdown problems due to possible plasma damage, and a high contact resistance problem due to inadequacies in the contact etching and forming processes.

We used a variety of failure analysis tools and techniques to provide timely fault localization and defect analysis for selected low yielding wafers. Failure analysis was performed using either finished wafers or packaged dice. Techniques used include light emission microscopy (LE), fluorescent microthermal imaging (FMI), SEM/voltage contrast imaging, resistive contrast imaging (RCI), and focused ion beam (FIB) cross sectioning, as well as e-beam testing using an IDS-5000 with an HP 82000 for electrical stimulus.

Fabrication Process

16k and 256k SRAMs were used as test vehicles for submicron process development, yield and reliability enhancement, and qualification. Both SRAMs feature an n -well CMOS structure, 0.5 μm minimum dimension (silicided gates), and a six-transistor cell design. The 16k SRAM uses a single level Al-Cu interconnect scheme. The 256k SRAM uses a triple level Al-Cu interconnect scheme providing a more compact design.

The silicon wafers were 6 inch diameter with (100) orientation and p -type resistivity. A 3 μm thick epitaxial Si layer was grown on the Si substrate. A semi-recessed LOCOS oxide isolation scheme was used with a thickness of 450 nm. The gate oxide thickness was 11 nm and the minimum drawn gate length was 0.6 μm . The gate material was phosphorus-doped polysilicon. An LDD (lightly doped source/drain) process was utilized for both the n - and p -channel MOS transistors with a 180 nm silicon nitride spacer for the LDD implant. The polysilicon conductors and the n^+ and p^+ doped source and drain areas were silicided with TiSi_2 to achieve both low sheet resistance and low contact resistance.

After the BPSG (borophosphosilicate) interlevel dielectric deposition using PETEOS (plasma enhanced decomposition of tetraethyl orthosilicate), chemical-mechanical polishing (CMP) was used for planarization. Photolithography and reactive ion etching (RIE) were then used to open the contacts. The contacts have a drawn minimum feature size of 0.7 μm . Slight etching with diluted HF and Ar sputtering of the contacts was followed by a sputtering deposition of Ti/TiN. A tungsten chemical vapor deposition (CVD) process was then used and CMP planarized to form tungsten studs in all contacts. A sputtered Ti-AlCu-TiN metallization layer was deposited and etched with RIE to complete the first interconnect layer. The remaining two upper interconnect layers were also processed in a similar manner. Finally, a 2% CVD phosphosilicate glass (PSG) passivation of 800 nm thickness was deposited followed by a H_2/N_2 forming gas anneal at 450 $^\circ\text{C}$.

Yield Analysis Tools

To support defect reduction and quality control activities at Sandia's submicron wafer fab, particle contamination is routinely measured. A Tencor 6200 wafer scan tool is used to assess both cleanroom and tool/process generated particles using monitor wafers. Defects and particles on in-process or patterned wafers are assessed using a Tencor 7600 tool. The assessment of defects and contamination on ICs is accomplished using both defect density structures and SRAMs.

The 256k or the 16k SRAM reticles have augmented with various types of parametric test structures and defect density evaluation structures. The 256k SRAM consists of 16 blocks. Each block is a basic 16k SRAM. Within each block there are 256 pages, and for each page there are eight, 8-bit words (64 bits).

Defect monitoring structures and parametric data analysis tools were available to support yield and FA analysis. These tools include:

(1). Parametric data analysis structure: This consists of various MOS transistors and capacitors, junction diodes, contact chains, Van der Pauw sheet resistance structures, etc. These structures are valuable for monitoring both MOS device and interconnect parameters and for identifying gross processing problems.

(2). Defect density evaluation structure: These are large area structures to determine defect density of various basic device/interconnect elements, such as gate oxides, contacts and vias, and interconnecting lines.

(3). Wafer yield map: Single and stacked wafer yield maps are available to display SRAM failure categories. These include input pin short/open, V_{DD} -to- V_{SS} short, high I_{DDQ} , and functional or speed related failures.

(4). Memory bit map: Besides displaying topological location of all the failing bits in a memory array, these bit maps also indicate a bit's specific failure type, either stuck at high (1) or at low (0).

Yield and Failure Analysis Support

During the initial development, key process parameters were fine-tuned. These include threshold voltages, diode and punch-through leakage, polygate, n^+ and p^+ sheet and contact resistance, and thickness of all thin film layers. Their uniformity across the entire wafer were also examined and the corresponding processes were tuned to meet the required control limits.

Various defect density evaluation structures were used to detect defects and contamination using both short loop test wafers or finished product wafers. Although using short loop tests to estimate defect density can provide fast feedback, the yield and FA results of the SRAM wafers received the most attention.

The SRAMs have four major electrical failure categories; these are: 1) Input pin open/short, 2) V_{DD} -to- V_{SS} short, 3) high I_{DDQ} , and 4) functional failures. The following FA case studies are based on these major failure modes.

Case A: Inter- or Intra-connect Shorts

Fluorescent microthermal imaging (FMI) [2,3] was used for the diagnosis of failures with either high I_{DDQ} , V_{DD} -to- V_{SS} shorts, or high I/O leakage failures. FMI detects hot spots with high sensitivity and acceptable spatial resolution. Interconnect shorts are often the main reason for high current failures.

Several major defects detected using FMI are shown in Figs. 1 through 7. A typical FMI image of interconnect short is shown in Fig. 1. A gross tungsten residue defect that had shorted metal-1 to metal-2 is shown in Fig. 2. Another example of a similar inter-metal short detected with FMI and cross-sectioned with the FIB is shown in Fig. 3.

Fig. 1 - A typical FMI image of a failure site due to an interconnect short defect.

Fig. 2 - SOM (scanning optical microscope) images of a hot spot detected using FMI. A higher magnification SEM image of this defect after delayering is shown at the lower left corner. The defect is a tungsten short between metal-1 and metal-2 interconnects.

Fig. 3A - A piece of tungsten embedded between two AL-Cu interconnects. Fig. 3B - Another gross inter-metal short caused by a larger tungsten defect.

We observed during initial development that wafer scratches and CVD oxide adhesion problems had caused some cracking and delamination of interlevel dielectrics during or after CMP polishing. The defects shown in Fig. 3A and 3B are pieces of tungsten embedded between the metal-2 and the metal-3 interconnects. The root cause of these shorts is actually initiated by a thinning or voiding problem at the surface of the interlevel BPSG dielectrics. Improved via mask design which eliminated large W features (especially in the scribe area) has greatly reduced such defects. A factor of 3 reduction of inter-metal shorts occurred with the new contact/via mask combined with the deposition of a thin CVD oxide after interlevel dielectric polishing.

Fig. 4 - The top image shows an FMI detected defect (arrows). A FIB cross section of this defect is shown in the lower image. Gross metal-1 bridging defect is shown, probably caused by a patterning defect.

Fig. 5 - FIB cross section of an FMI detected particle which caused an intra-metal short. The image on the right is taken near the short where a gap between the metal bus lines is shown.

Defects due primarily to particles and photolithography processes also caused some of the observed intra-metal shorts. Examples of a metal patterning defect and a particle causing V_{DD} -to- V_{SS} shorts are shown in Fig. 4 and 5, respectively. These were detected with FMI and analyzed with FIB cross sectioning techniques.

Case B: High I_{DDQ} due to Gate Oxide Shorts

Light emission (LE) microscopy techniques [2,4] are also commonly used in certain cases of high I_{DDQ} failure for fault localization. In this study, I-V curves of ICs with high I_{DDQ} are used for detailed analysis and also for verifying automated test results. An ohmic short with extremely high I_{DDQ} (> 10 mA) usually indicates a metal bridging defects between V_{DD} and V_{SS} lines. If I_{DDQ} is in a lower range (between 10 mA and 1 μ A) and its I-V curve has an exponential characteristic, a gate oxide short is often the cause [5,14].

During initial process development, a high percentage of SRAMs failed I_{DDQ} standby leakage tests. Using LE we were able to locate the failure sites quickly. Fig. 6 shows a worst case where the failure sites were identified using LE. A plasma photoresist stripping machine was later identified as the cause for the gross gate oxide shorts and oxide integrity/quality problem.

In another case, the failure site of a gate oxide short was localized and analyzed using a combination of both FMI and EBIC techniques. The IC had a high I_{DDQ} of more than 15 mA during standby with a V_{DD} of 3.3 V. No detectable light emission was observed. It was determined later that the oxide defect was covered with a very wide V_{DD} metal bus. FMI detected a hot spot at one of the input pins, shown in Fig. 7. The device was later delayered and inspected again, with no obvious physical defect observed (see Fig. 8). The IC was then further examined with passive EBIC (electron beam induced current) analysis. A point gate oxide short between the gate and the substrate of a p -channel transistor was detected as shown in Fig. 9. A CMOS I/O buffer was apparently turned on due to its shorted gate to the p -channel substrate region, producing excessive I_{DDQ} leakage current.

Fig. 6 - Light emission sites due to ruptured gate oxide after plasma stripping of photoresist.

Fig. 7 - A hot spot detected with FMI on one of the high I_{DDQ} IC failures. A higher magnification view of the hot spot is shown in the insert.

Fig. 8 - After removal of upper metal layers of the IC in Fig. 7, underlying structure can be seen. No defect was observed.

Fig 9A - A gate oxide short detected with a passive EBIC technique (arrow). Fig. 9B - After removal of the polysilicon gate, an oxide defect site was observed.

Case C: Functional Failures Caused by High Contact Resistance

Several initial lots had a high percentage of functional failures (both 16k and 256k SRAMs). To diagnose functional failures of SRAMs, memory bit maps are very effective [6]. Bit maps provide a detailed, two dimensional display showing the memory array physical layout. In addition, the location and number of failing bits provide clues for the failure mechanisms. For example, a single-cell fault is the failure of an isolated cell. Single-cell faults are generally caused by defects in gate oxide or junctions, blocked vias or contacts, or by metal 1 opens or shorts. An adjacent-cell fault is the failure of paired cells (two adjacent cells). Adjacent-cell faults are often caused by either blocked vias or blocked contacts shared between the paired cells. Row or column failures can be caused by poly or upper level interconnect failures, or faults in decoders, multiplexers, or bit sensing circuits.

Bit map was used to analyze several failing SRAM lots with excessive functional failures. The bit maps of these failing ICs displayed a high percentage of "stuck-at" bit failures. A majority of these had adjacent-cell failures and only a few showed single-cell failures. The adjacent-cell failures consistently displayed a bit failure signature of low-high (0-1) pattern with very few low-low (0-0) or high-high (1-1) pattern. A display of this low-high pattern is illustrated in Fig. 10 with an IDS-5000 voltage contrast image. Since these failures occurred in both the 256k and the 16k SRAMs (there are no vias in 16 k design), the possible cause of the adjacent-cell failure was narrowed down to the integrity of shared contacts.

The cell layouts for the 256k and the 16k SRAMs showed that all of the adjacent-cell pairs share a single n^+ V_{SS} contact (Fig. 11). Through this shared n^+ contact, both NMOS sources of the adjacent cells were connected to the Vss bus. The layout also shows that there were no other shared contacts between adjacent cells. Using an HP 82000 tester, additional failing ICs were carefully tested and characterized. Interestingly, the number of adjacent-bit failures increased as V_{DD} increased. In contrast, we did not observe any bit or increasing failure with increased V_{DD} for functional SRAM devices from good wafer lots. Using the IDS-5000 with electrical stimulus from

an HP 82000, we analyzed memory bit voltages during write/read operations. We observed that the adjacent cells' bit pattern switched simultaneously to a "Low-Hi" pattern after a read operation of the other cell. This was observed and validated for all the adjacent-cell failures analyzed but did not occur with any of the functional cells in a failing IC. These results further indicated a high V_{SS} contact resistance was the cause of the observed adjacent-cell failures. A read disturb between the adjacent cells could have caused the functional failure if the resistance of the shared contact is too high.

We reviewed the n^+ contact resistance trend chart to investigate why it didn't warn us of the potential yield problem. The average contact resistance for several low yielding lots were acceptable with an extremely low percentage of open failures. The "average" contact resistance was marginally within both the manufacturing and the design specification, i.e., less than 10 ohm/per contact (Fig. 12). While correlating the contact resistance distribution to a stacked wafer yield map, we had noticed that most of the yielding ICs were located, however, around the edge where the contact resistance were the lowest. It was also determined that there are 3000 contacts within this contact chain structure. This is much less than the total number of contacts in the SRAMs. Moreover, the resistance distribution of all contacts (within a chain or a SRAM) is really unknown.

Fig 10. - Static voltage contrast image of some 16k SRAM cells is shown here. A Low-Hi bit pattern which emulates a "stuck-at" adjacent-cell failure is illustrated (arrow). Bit sites and V_{SS} buses are also shown.

A unit cell for the 16 k-bit SRAM design

Fig. 11 - The layout of a unit cell for the 16k SRAM. The shared V_{SS} contacts are indicated by arrows.

Unit N+ Contact Resistance Measured using a 3000 Contact Chain. Unit: ohm

Fig. 12 - Wafer stack map of the averaged, unit n^+ contact resistance distribution from all processed lots with yield problems. The contacts at the center show only marginally high resistance when compared to the edge. Most of the yielding dice, however, are located around the wafer edge.

Fig. 13 - Top: RCI image showing a contact chain with good uniformity among all the contacts. Bottom: RCI image showing an abrupt contrast change (arrow), indicating high resistance contacts.

Resistive contrast imaging (RCI) [2,7] was used to study the resistance uniformity among all the contacts within a contact chain. Contact chain structures, with 3000 contacts from the same wafer lot as the failed ICs, were packaged and analyzed. Fig. 13 shows the RCI image for a normal contact chain (top image) with good uniformity among all the contacts. A bad contact chain (bottom image) showed two abrupt contrast changes, one at the right-center and another at the left-lower areas of the chain (arrows). The contrast changes indicate the presence of some high resistance contacts within the contact chain.

Fig. 14 - High magnification images of a failing "bad" contact chain. On top is an RCI image and on the bottom is an SEM image showing the same region.

Fig. 14 shows a higher magnification image of another failing contact chain structure. The top image of Fig. 14 is an RCI image and the bottom is an SEM image showing the same region. RCI analysis indicated that there exists a "bad" contact in the contact chain that had extremely high contact resistance (arrow). The contact resistance of these high resistance contacts was estimated to be as high as 20 k Ω , based on changes in the RCI image contrast, compared to 2 ~ 4 Ω for a normal contact.

Results of SPICE simulation demonstrated that adjacent-cell faults could occur during read operation if the shared V_{SS} contact had a resistance higher than approximately 200 Ω . Therefore, it appeared that high resistance in the V_{SS} contact between adjacent cells was the cause of the observed functional failure (a read disturb between adjacent cells which shared a high resistance V_{SS} contact).

Fig. 15 - Circuit schematic illustrating the current paths and node voltages during a read operation for two adjacent cells.

Fig. 16 - SPICE simulation timing diagram showing a read disturb operation for $R_C=500$ ohm.

Fig. 15 is a circuit schematic that illustrates the current paths and node voltages during a read operation for adjacent-cell failures (See Fig. 11 for the cell layout). SPICE simulation timing diagrams which indicate a read-disturb condition are shown in Fig. 16 versus normal read operation is shown in Fig. 17.

The root cause of the high contact resistance problem was later identified. The contact resistance was reduced through several improvements in the manufacturing process. The high contact resistance was the result of a combination of several marginal processing steps in the areas of contact etch and metal deposition. These include the source and drain silicidation, the contact etch, the light HF etch and Ar sputtering clean, and the Ti/TiN liner deposition processes. The depth-to-width aspect ratio of these submicron contacts can also play an important role in the contact forming process. We have noticed that if this ratio is higher than 1.5, the thickness of the Ti liner deposited at the bottom of the contacts will be gradually reduced. Such reductions can affect the ability to form low resistance contacts. The use of a collimator during Ti sputtering is desirable if conventional sputtering tools and processes are used. Recent improvements in the contacts has reduced the average contact resistance to around 2 ohm/contact with good uniformity across the entire wafer.

Fig. 17 - SPICE simulation timing diagram showing a normal read operation with $R_C=0$ ohm.

Conclusion

Three types of major defects were analyzed for an advanced, 0.5 μm , fully planarized, triple metallization CMOS technology. These defect types included inter-level and intra-level metallization shorts (bridging defects), gate oxide shorts, and high contact resistance. These types of defects are representative of the primary yield and reliability problems for deep submicron CMOS IC technologies, including those going down to 0.35 μm and below. They are potential showstoppers for meeting time-to-market and production goals. They present the microelectronics industry with critical challenges for future testing and failure analysis. These challenges must be met with the development of new and improved failure analysis tools and techniques, as well as enhanced test models and diagnosis procedures. Evolutionary advances in failure analysis techniques have been made recently [e.g., 8-10], but a greater investment must be made by the industry for research and development on revolutionary capabilities. For example, automated IC diagnosis and signature analysis procedures are needed that use defect models and classes for failure site localization in addition to failure mechanism determination [11-13].

Acknowledgment

The authors would like to thank Richard E. Anderson and Daniel L. Barton for reviewing this manuscript. We are grateful to Jim Rife for providing FIB cross sectioning and Keith Yoneshige for data analysis. This work was performed at Sandia National Laboratories and is supported by the U.S. Department of Energy under contract DE-AC04-94AL85000.

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