Self-Stressing Structures for Wafer-Level Oxide Breakdown to 200 MHz

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Abstract—We have demonstrated for the first time high frequency (210 MHz) oxide breakdown at the wafer-level using on-chip, self-stressing test structures. This is the highest frequency oxide breakdown that has been reported. We used these structures to characterize the variation in oxide breakdown with frequency (from 1 Hz to over 200 MHz) and duty cycle (from 10% to 90%). Since the stress frequency, duty cycle and temperature are controlled by DC signals in these structures, we used conventional DC wafer-level equipment without any special modifications (such as high frequency cabling). This self-stressing structure significantly reduces the cost of performing realistic high frequency oxide breakdown experiments necessary for developing reliability models and building-in-reliability.

I. INTRODUCTION

As integrated circuits (ICs) are produced with feature sizes below 0.5 micron, clock speeds on complex microprocessors have increased above 200 MHz. However, reliability characterizations using test structures primarily consist of DC or low frequency stresses. Since reliability under high frequency (HF) use conditions can be significantly different than the DC results, actual circuit reliability may be significantly overestimated or underestimated.

Oxide breakdown is the failure of an insulating material. Figure 1 shows that typical fast, wafer-level tests utilize DC voltages (or currents). Since DC stresses result in the shortest time-to-failure, studies under these conditions are experimentally the easiest and most convenient to perform. However, IC building blocks (such as the inverter) operate with time-varying waveforms. A

Fig. 1. (a) Typical oxide breakdown tests use DC stress; while circuits (b) operate under time-varying conditions and (c) the voltage across the gate oxide capacitor also varies with time

closer examination of the p-channel device (in the inverter) shows the HF time-varying stress waveforms across the gate oxide during operation of the inverter.

ICs operate at frequencies greater than 200 MHz. Yet the highest frequency oxide stress reported to date is only 4 MHz [1]. This work showed that low frequency bipolar stress of oxides can result in 100 times longer lifetimes than an equivalent DC stress. However, there have been no investigations of breakdown at actual IC frequencies. Therefore, being able to develop and characterize high-frequency oxide breakdown models is the key for making quantitative tradeoffs between performance and reliability.

This work addresses a fundamental problem with HF reliability characterization: it is expensive and as a result is not often investigated. We will demonstrate a new cost-effective alternative for realistic oxide breakdown using on-chip self-stressing structures[†]. We will use these structures to quantitatively examine, for the first time, oxide breakdown, at high frequency (1 Hz to 210 MHz) and with varying duty cycle (10% to 90%).

We describe the self-stressing oxide structures in Section II. These structures will then be used to perform oxide breakdown at 200 MHz in Section III. This stress is about 100 times higher than published experiments. Finally, we summarize the key points in Section IV.

II. SELF-STRESSING OXIDE STRUCTURE

A. Block Diagram and Structure Layout

Figure 2 shows a block diagram of the self-stressing structures. An on-chip, DC-controlled oscillator produces signals from below 1 MHz to above 500 MHz. The maximum frequency scales with the technology in which the structures are built. We can also control the duty cycle of the stress waveform. This HF signal is routed on-chip to various circuits. These circuits can include logic elements (for hot carriers), metal structures (for electromigration) and oxide structures (for oxide breakdown). In addition to the circuit elements in Figure 2, the self-stressing structures can accommodate more functional blocks such as adders or comparators. We used a self-stressing hot

[†]Patent pending: E.S. Snyder and D.V. Campbell, "Self-stressing high frequency on-chip test structures"

Fig. 2. Self-stressing high-frequency reliability structures permit cost-effective at-speed reliability characterization for various reliability failure mechanisms.

carrier structure to examine HF transistor reliability models which was reported at the 1993 IRPS [2]. We have also built structures to study HF electromigration models. This work was described at the 1994 IRPS [3]. Finally, self-stressing HF oxide breakdown structures are presented in this work.

Self-stressing structures have unique advantages over externally applied HF signal techniques. First, we are able to stress at very high frequencies. Since all operations are performed on-chip, we are only limited by the IC technology being characterizing. The insertion losses and impedance matching problems normally associated with applying high bandwidth signals to structures disappear. We also achieve significant cost savings by using a DC wafer-level test system. In fact, all the HF oxide experiments were performed with an off-the-shelf DC wafer-prober and DC test system. We have also performed HF experiments by placing the structures in packaged parts and testing them with a DC test system. These self-stressing structures are implemented using standard digital CMOS, and we have built functioning structures in technologies with channel lengths from one micron to one-half micron. The structures also have on-chip heaters

Fig. 3. (a) Block diagram of self-stressing high-frequency oxide breakdown structure used with a DC wafer-level test system. (b) Microphotograph of structure built in a 0.8 micron CMOS process.

capable of 400 °C temperature stresses. This allows us to perform high temperature and HF stresses without expensive fixtures or ovens.

A HF oxide breakdown structure is in Figure 3. The block diagram shows the self-stressing DC-controlled oscillator to the left. The oscillator controls the signal frequency and duty cycle with DC currents. The HF signal is routed to a buffer. The buffer controls the stress waveform applied to the capacitor. The structure also contains an on-chip heater and temperature sensor. Figure 3 also shows a microphotograph of the self-stressing oxide structure. It is attached to 100 micron by 100 micron pads. By rearranging the pads, the structure can also be placed into the streets between product ICs.

B. DC Control of HF Parameters

The self-stressing structure controls a key number of oxide breakdown parameters with DC signals. We can vary the frequency from DC to over 500 MHz in a 0.8 micron CMOS process. Deep sub-micron processes will achieve frequencies higher than 500 MHz. The duty cycle is adjustable from 1% to 99%. This permits characterization of annealing effects. The temperature can be varied from room temperature to over 400 °C. We can also change the maximum applied electric field. Other self-stressing structures control additional parameters. For example, we can vary the rise and fall time of the hot-carrier self-stressing structure. The electromigration structure controls the peak current density and stress waveform type (unipolar, bipolar, asymmetric).

The self-stressing oscillator frequency is controlled with a DC current. Figure 4 illustrates this variation in frequency with DC control current. The frequency is directly proportional to the DC current until around 100 MHz. The frequency then rolls over and peaks at 500 MHz. The oscillator used to generate these signals is a modified ring-oscillator which is built using standard digital CMOS [4]. The oscillator can also vary the signal duty cycle.

We have developed a simple analytical model which describes the variation in frequency and duty cycle with DC current [4]. Figure 5 shows the model predictions as a

Fig. 4. Variation of on-chip oscillator frequency with DC control current. The observed maximum frequency of 500 MHz scales with the technology.

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Fig. 5. Model predictions (surface) and experimental data (spheres) demonstrate on-chip oscillator control of duty cycle and frequency with DC currents.

grayscaled surface. The duty cycle is plotted on the Z-axis while the DC control currents are plotted on the X-axis and Y-axis. The frequency is shown by the grayscale on the surface. The spheres are experimental data and are accurately predicted by the model. Figure 5 demonstrates the ability to predict and control the frequency and duty cycle with two DC currents.

C. Verification of HF Stress Waveform

The generated HF signals are routed on-chip to a test structure (in this case a capacitor). We verified the integrity of this HF signal by measuring it with an active probe. Figure 6 shows a secondary electron image of the stressed capacitor and driver circuitry. The oscillator signal enters from the left. This signal drives the buffer. The buffer provides the current necessary to charge and discharge the capacitor to the right. The stressed structure is a 30 micron by 30 micron gate oxide capacitor which is 30 to 40 times larger than the gate of a typical VLSI transistor.

To verify the signal applied to the capacitor, we "drilled" through the passivation to the metallization using a focused ion beam machine. We then contacted the metallization with a high frequency active probe. The active probe has a 1 GHz bandwidth and a 0.1 pF load

Fig. 6. High frequency stress waveform measured using a high bandwidth active probe. A secondary electron image shows the hole through the passivation made with a focused ion beam machine.

Fig. 7. Measured high frequency stress waveform applied to the capacitor in the self-stressing structure.

capacitance. Other internal probing techniques can be used (e.g. electron beam test system). However, this active probe technique has a higher bandwidth and yields more accurate results. Figure 7 shows the measured electric field across the capacitor using the active probe. The rise and fall times are approximately 0.8 ns. A simple calculation using actual capacitance and drive current predicts a rise or fall time greater than 0.7 ns. These transition times would decrease with a bigger buffer or smaller capacitor. Figure 7 demonstrates a controlled high-frequency waveform is applied to the capacitor using a simple DC wafer-prober. In contrast, applying high-bandwidth signals to a discrete test structure is a difficult and challenging proposition.

III. HIGH FREQUENCY OXIDE BREAKDOWN

We performed a series of HF oxide breakdown experiments using the self-stressing structure. Figure 8 depicts the typical results of this on-chip oxide stress. The average current through the capacitor is plotted versus stress time. Both a DC stress and a 210 MHz unipolar stress are shown. The current initially increases during the DC stress. It then decreases until breakdown. This current-time profile is typical of most reported oxide breakdown experiments. A 210 MHz unipolar stress results in a similar current profile. However, the initial average current is lower and the time-to-failure is longer. For this 50%

Fig. 8. (a) 210 MHz oxide breakdown performed with DC wafer-level system. (b) Microphotograph of capacitor before and after high frequency stress.

Fig. 9. Oxide breakdown from DC to 210 MHz performed with self-stressing structure and a DC wafer-level system. 20 separate experiments were performed at each frequency.

duty cycle waveform, the failure is about four times longer than the DC stress. Microphotographs of the capacitor before and after the 210 MHz stress illustrate the breakdown with a visible “hole” in the capacitor.

A. Oxide Breakdown from DC to 210 MHz

Unipolar stress experiments were repeated over a large range of frequencies (at a fixed duty cycle) to examine the dependency on oxide breakdown. Figure 9 shows the median-time-to-breakdown as a function of the stress frequency from 1 Hz to 210 MHz. Each square is the median of 20 separate experiments (at a given frequency); while the diamonds are the 98 % confidence bounds. All stresses were performed at 50 % duty cycle and with the same peak electric field (11.6 MV/cm). The DC stresses were also performed at 11.6 MV/cm. The median-time-to-failure (or lifetime) in Figure 9 is the raw stress time and has not been adjusted for duty cycle. From 1 Hz to 10 kHz we observed an increase in lifetime above the DC stress lifetime. From a stress frequency of 10 kHz to 210 MHz we noted no further increase in lifetime with frequency. With a 50 % duty cycle, the capacitors in Figure 9 are being stressed for one-half of the time. If there was no enhancement (or degradation) in the unipolar breakdown, all the oxide breakdown data should fall on the 2x line. However, for frequencies above 10 kHz, we observed a 4.4 times increase in lifetime (over the DC lifetime).

Fig. 10. Variation in oxide breakdown with duty cycle characterized using self-stressing structure. Inset shows measured stress waveform.

Fig. 11. On-chip temperature of test structure is varied by power applied to a polysilicon heater.

B. Oxide Breakdown with Duty Cycle

In order to investigate this lifetime enhancement, we performed a series of self-stressing oxide breakdowns at various duty cycles. At a fixed frequency (10 kHz) and peak electric field (11.6 MV/cm), we varied the duty cycle of the applied unipolar waveform. We performed 10 to 15 separate experiments at each duty cycle. Figure 10 shows results of the experiment. The enhancement in the oxide breakdown above the DC breakdown is plotted as a function of the duty cycle. The enhancement is the ratio of the unipolar lifetime to the DC lifetime. If the only change in lifetime is due to variation in the duty cycle, the lifetime would be inversely proportional to the duty cycle. That is, the data in Figure 10 would follow a line of slope -1. However, the data shows a marked enhancement. For example, a 10% duty cycle shows an enhancement of 40 times over the DC results. This result has significant implications for reliability modeling and simulation.

C. High Temperature Oxide Breakdown

The temperature of the self-stressing oxide structure is controlled with an on-chip heater. Figure 11 shows an increase in on-chip temperature to at least 400 °C. We then performed several experiments at high temperature and HF using the self-stressing structure. The results are summarized in Figure 12. This shows the average current as a function of stress time at 350 °C. The failure times are shorter than the room temperature results of Figure 8.

Fig. 12. High temperature and high frequency oxide breakdown performing using a DC wafer-prober without a hot chuck.

IV. SUMMARY

We have shown that self-stressing structures work at high frequency, high temperature and with existing DC test equipment. We have also quantified the enhancement due to unipolar waveforms over a large frequency and duty cycle range. These structures are useful for realistic high frequency reliability characterizations and for calibrating simulators necessary for maximizing performance without sacrificing reliability.

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