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rise time for framing camera deflection electronics**

Anthony T. Rivera
Stan Thomas

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MOSFET solid state switching circuit improves the 0 to 99% rise time for framing camera deflection electronics

Anthony T. Rivera and Stan Thomas

Lawrence Livermore National Laboratory
Electrical Engineering Department
7000 East Ave. P.O. Box 808 M/S 283
Livermore, California 94550

ABSTRACT

We have improved the 0 to 99% rise time voltage on our 2 frame deflection plates from 160nS to 65nS with the addition of a peaking circuit that works in conjunction with our primary 2 frame deflection circuitry. Our peaking technique has applications to other HV pulsed including those which must drive 51 ohm loads. Generally, rise time voltages are measured between 10 and 90%. To minimize the camera image blur resulting from the dynamic influence of deflection plate potentials acting on photocathode electrons, it was necessary to design a circuit that would rise from 0 to the 99% voltage level in under 100nS. Once this voltage was reached, it was necessary to stay within 1% of the attained voltage level for a duration of 1uS. This was accomplished with the use of MOSFET solid state switching.

Keywords: deflection plate, frame, MOSFET, solid state, high voltage, transformer, rise time, pulser, 51 ohm

2. CAMERA DESIGNATIONS

Our camera will image photons for two 1uS frames. For purposes of this discussion we will call one camera deflection plate "A", and the other camera deflection plate "B". We will refer to the pre camera trigger destination of electrons emitted by the photocathode as location "0", and the destination of electrons remaining after frame 2 data is collected as location "3". Locations "0" and "3" are pre and post camera deflection plate positions respectively. The deflection plates "A" and "B" have been simulated with a 1KV 10pF ceramic disk capacitor.

3. GENERAL DEFLECTION PLATE OPERATION

When powered on, plates "A" and "B" reach a voltage level of -435 V and +435 V respectively. The resulting differential potential of -870 V shown in fig. 1 as "A-B", deflects any prior photocathode electrons to location 0. The camera is now ready to be triggered. About 4uS before the arrival of frame 1 photons reaching our photocathode, plates "A" and "B" are switched to -145 V and +145 V respectively. The resulting "A-B" voltage is -290V. The deflection plates will now deflect electrons to frame 1. The first photons of frame one will arrive at the photocathode 5 time divisions in from the left of fig. 1. The circuit was designed to reach the voltage level required for frame 1 deflection in a few microseconds. Faster switching here

Fig. 1

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is not necessary because there will be few electrons generated at that point in time. Photocathode electrons are then deflected to frame 1 for a duration of 1 μ S. After 1 μ S deflection plates "A" and "B" are switched to +145 V and -145 V respectively. The "A-B" voltage is +290 V. This will deflect the photocathode electrons to frame 2. This frame 1 to frame 2 transition corresponds to the beginning of the 6th division in from the left of fig. 1 and is completed in 65nS. Frame 1 and 2 deflection plates stay within 1% of their reached voltage for a duration of 1 μ S each. The 65nS transition from frame 1 to frame 2 was necessary to minimize the blurring between frames. The deflection voltages for the two frames, which are 1 μ S each, needed to be "flat" to within 1% because amplitude variations would contribute to loss of resolution by wandering the image data in the 2 frames. When frame 2 photocathode electrons have been received for 1 μ S, deflection plates "A" and "B" switch to +435 V and -435 V respectively. This produces an "A-B" potential of +870 V. Photoelectrons after frame 2 are deflected to location "3". The deflection plates will keep photocathode electrons at location "3" for a sufficient length of time.

4. MOSFET PEAKING CIRCUIT

As a Metal Oxide Semiconductor Field Effect

Transistor (MOSFET) turns on, its source voltage approaches the power supply voltage, and the remaining drain to source voltage decreases. When the drain to source voltage nears 7 volts or less, the MOSFET internal capacitance rises dramatically. The result of such a rise in capacitance is a significant increase in rise time of the deflection circuit as the drain to source potential drops into this 7 volt range. The "conventional" rise time of 10-90% in our circuits frame 1 to frame 2 transition is 20nS. It is the 90-99% rise time period in which the MOSFET capacitance's increase our frame 1 to frame 2 transition time to 165nS. This was not acceptable, therefore a peaking circuit was added to the original design. Refer to fig. 2. Both waveforms begin (not shown) at the end of the first time division from the left of fig. 2. Figure 2 represents the transition time from frame 1 to frame 2 in the 90-100% region. The cursors shown represent the 1% window of amplitude tolerance for frame 2. A peaking circuit was added to deflection plate "A". Specifically, we connected a "secondary" parallel MOSFET switch with a drain capacitor charged to a slightly higher potential than the primary (original) MOSFET drain capacitor. The secondary drain capacitor is small in value compared to the primary MOSFET drain capacitor. The primary and secondary MOSFETs are gated by a mutual step-down pulse transformer. The 2 secondary windings of this transformer T3 in fig. 4 are isolated. By adjusting the secondary MOSFETs drain capacitor voltage, we can compensate for the unacceptable 0 to 99% rise time characteristics of the primary MOSFET.

Fig. 2

Transistor (MOSFET) turns on, its source voltage approaches the power supply voltage, and the remaining drain to source voltage decreases. When the drain to source voltage nears 7 volts or less, the MOSFET internal capacitance rises dramatically. The result of such a rise in capacitance is a significant increase in rise time of the deflection circuit as the drain to source potential drops into this 7 volt range. The "conventional" rise time of 10-90% in our circuits frame 1 to frame 2 transition is 20nS. It is the 90-99% rise time period in which the MOSFET capacitance's increase our frame 1 to frame 2 transition time to 165nS. This was not acceptable, therefore a peaking circuit was added to the original design. Refer to fig. 2. Both waveforms begin (not shown) at the end of the first time division from the left of fig. 2. Figure 2 represents the transition time from frame 1 to frame 2 in the 90-100% region. The cursors shown represent the 1% window of amplitude tolerance for frame 2. A peaking circuit was added to deflection plate "A". Specifically, we connected a "secondary" parallel MOSFET switch with a drain capacitor charged to a slightly higher potential than the primary (original) MOSFET drain capacitor. The secondary drain capacitor is small in value compared to the primary MOSFET drain capacitor. The primary and secondary MOSFETs are gated by a mutual step-down pulse transformer. The 2 secondary windings of this transformer T3 in fig. 4 are isolated. By adjusting the secondary MOSFETs drain capacitor voltage, we can compensate for the unacceptable 0 to 99% rise time characteristics of the primary MOSFET.

5. HIGH VOLTAGE 51 OHM PULSER/STEP GENERATOR APPLICATIONS

The MOSFET peaking circuit will also enhance the 0 to 99% rise time of higher current lower resistance loads. In fig. 3 there are 2 waveform voltages generated by a current transformer which was placed to view the full current of the 51 ohm load. Each vertical division is 400mA. The peak current for each of the 2 waveforms was about 1.84 A. The voltage amplitude for each waveform was 94 V. Both waveforms have approximately 20nS rise times as determined by the 10-90% convention. The 0-99% rise time is 60nS for the compensated 51 ohm pulser and 160nS for the uncompensated 51 ohm pulser. Again the same technique of using "primary" and "secondary" parallel MOSFETs was applied. The "primary" and "secondary" capacitor values and voltages will depend on the load impedance, duration of the pulse, and on amplitude "flatness" requirements.

6. 2-FRAME DEFLECTION CIRCUIT INFORMATION

The 2 frame deflection circuit in fig. 4 uses 800 V and 1KV N-channel MOSFETS. All 6 circuit triggers are gated by a multi-channel 50 ohm output delay generator. Each trigger, J1 through J6, is sent to a step-down isolated pulse transformer. The core material is 3E2A. The circuit triggers are gated in time as pairs in the following order: J1 J2, J3 J4, J5 J6. These 3 stages of gating control the timing and duration of photocathode electrons deflected from location 0 through location 3. In order to isolate and steer the 3 stages of MOSFET deflection voltages that occur on plates, "A" and "B", 30nS recovery 1KV diodes are used. The 6 High voltage power supplies (not shown) were DC to DC converters and are controlled by adjustable TO-220 regulators.

7. ACKNOWLEDGMENTS

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