Final Report of Contract No. DE-FGO2-91ER40680

Super Conductor Supercollider Front End Electronics Development;
Ring Imaging Cerenkov Studies; and Warm Liquid Calorimetry

The University of Pennsylvania group that was involved in SDC was responsible, jointly with the KEK Laboratory in Japan, for the design and production of the readout electronics for the SDC straw tube tracker (a \$12 million electronics effort). Our responsibilities included major contributions to the overall conceptual design, oversight of all the contributions from North America and direct responsibility for the HV/ASD assembly, the amplifier-shaper-discriminator chip, and HV distribution on the detector (the responsibility for the latter being shared with Colorado).

Amplifier-Shaper-Discriminator (ASD)

The very large number of channels in the SDC straw tracker (approximately 140,000) required that the amplifier-shaper-discriminators (ASDs) be densely packed and very low power. At the same time, the desired position resolution and very high counting rate required high performance and low noise. These combined requirements led to the development of a complete signal processing system—preamplifier, shaping amplifier, tail cancellation, and discriminator on a single integrated circuit with eight channels per chip. This is the first time (within the particle physics community) that such a high bandwidth system has been integrated on a single die.

The low noise of the circuit allowed excellent position resolution and efficiency to be obtained (Figure 1) at a voltage 200 volts lower than present commercial systems of much higher power, size, and cost.

Figure 1: Measured position resolution (a) and inefficiency (b) vs. HV for cosmic ray tracker in a 4m SDC straw module with integrated HV/ASD assembly. The cosmic ray trigger was placed at 60, 160, and 360 cm from the electronics.

Measurements of the straw-electronics system showed very good performance, without any threshold adjustment up to counting rates of 2 MHz per wire. Very satisfactory results on resolution are obtained at rates beyond this, up to about 8 MHz per wire, (Table 1) if the threshold is

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Threshold (fC)	0 MHz	2.5 MHz	5.0 MHz	7-8 MHz
3	129 ± 5	155 ± 5	175 ± 5	200 ± 5
2		145 ± 5	160 ± 5	
-1			155 ± 5	170 ± 5
-2				162 ± 5
Monte Carlo	129 ± 5	135 ± 5	145 ± 5	150 ± 5

Table 1: SDC Straw Module track residuals in μm vs. single wire hit rate for a cosmic ray trigger at 150 cm from the electronics, no termination. As can be seen in the table, the baseline shift associated with increasing rate can be largely compensated for by a DC change in effective threshold setting. The Monte Carlo calculation includes only time shadowing effects.

Figure 2: Baseline restored analog output from an SDC 4m module illuminated by a series of strong radioactive sources. Pulses are clearly resolvable even at maximum illumination ($\sim 8\text{MHz}$).

adjusted for the baseline shift which occurs because of the AC coupling of the ASD to the detector anode. In a large system the baseline shift will probably need to be eliminated by some kind of explicit baseline restoration circuit. Figure 2 shows the results of a prototype baseline restoration circuit, implemented with discrete devices, at a counting rate of approximately 8 MHz per wire. The baseline is unshifted and most of the pulses are clearly separated. Figure 3 shows individual pulse shapes for cosmic rays (taken at low rates). The baseline restoration operates at high frequencies as a bipolar shaping with relatively short time constant; this results in relatively narrow pulses. It may be seen that the majority of pulses are quite uniform and clean; this results from the fact that the ionization clusters in CF_4 are closely spaced and have a high drift velocity. Thus even though the integration time of the amplifier is only about 6 nsec, little evidence of individual clusters is seen.

The performance of the integrated 8 ch ASD met essentially all of the SDC requirements with the exception that baseline restoration was not included in the original version; a revised version of the integrated circuit including the baseline restoration and with a modification to allow for a larger dynamic range will be developed with other funds.

Figure 3: Individual minimum ionizing (cosmic ray) pulses as seen at the output of the prototype baseline restorer. The upper pulse is a time expanded version of the lower pulse—20 ns per division and 50 ns per division respectively.

TCC

In the initial conceptual design for the tracking electronics, it was intended to locate the time measurement and Level 1, Level 2 buffering circuits on the detector, only a few centimeters from the ASD's. We therefore developed a very low power (6mW/channel) Time-to-Charge Converter with analog memory, which included L1 and L2 storage, on-chip ADC, and logic for interfacing with the trigger and with a first level data collection chip (DCC) being developed by the University of Toronto.

Figure 4 shows the digitized time versus the time of the discriminator signal relative to a reference clock. The least count of the ADC is 107 psec/count and the worst case integral non-linearity is approximately ± 150 psec peak to peak. This is much better than the initial design goal of 0.5 nsec, and we believe that the inherent time resolution of the device is less than 50 psec. The variation from capacitor to capacitor is substantially less than 0.5 nsec.

Cables

While the initial conception of the overall electronics provided for the time measurement electronics to be located inside the tracking volume, we realized that a more conservative design in which the discriminated signals were shipped to time measurement electronics on back of the calorimeter was feasible with low power drivers and new developments in cable technology. We designed a low current differential driver which is capable of sending signals over 50–100 Ohm cable with a power consumption of less than 5 mW per differential pair. For a high density, radiation hard cable, we designed a kapton strip cable with the differential pairs on opposite sides of approximately 5 mil of dielectric. The key to maintaining a fast risetime after 5–7 meters of cable, given the limitations of the conductor, is that the cable must be 4–5 mils thick. While such cables are routinely fabricated in short lengths (e.g., 30 cm) for PC computers, few manufacturers have made such cable in 5–7 m lengths. We succeeded in locating one or two fabrication houses with such capability and had a prototype cable manufactured. The waveform after 5m is shown in Figure 5.

While the SSC has unfortunately been terminated, the ASD's and TCC/AMU have application to a wide variety of experiments. This includes CDF, E781 at Fermilab, the Z chamber upgrade for L3 at LEP, ATLAS at LHC, HERMES at HERA, PHENIX at RHIC, and several others.

Figure 4: ADC output counts vs. discriminator to clock delay in the TCC/AMU (a) and the integral nonlinearity for two different capacitors (b). Note that a large part of the integral nonlinearity appears to be pattern noise which may be eliminated in the next version.

Figure 5: Measured jitter for a low level differential signal at the end of a 5m low mass transmission line. The scope trace was integrated for 1,000 sweeps, corresponding, roughly, to a 3σ time jitter measurement - 630ps.