SAN099-0711J
Submitted to: J. European Optical Society
January 12, 1999

RECEIVED
APR 07 1999
OSTI

Comparison of Techniques for Bonding VCSELs Directly to ICs

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Abstract

This paper reports the successful bonding of 8 x 8 and 4 x 4 VCSEL arrays to Si CMOS and GaAs MESFET integrated circuits and to GaAs substrates. Three different bonding techniques are demonstrated and their electrical, optical and mechanical characteristics are compared. All three techniques remove the substrate from the VCSEL wafer, leaving individual VCSELs bonded directly to locations within the integrated circuit.

I. Introduction

VCSEL based smart pixel arrays are very desirable for parallel optoelectronic processing and board to board interconnection since they can overcome the electrical interconnect bandwidth bottleneck. The integration of VCSELs with foundry fabricated integrated circuits is the key technology required to fabricate the smart pixels. For large arrays, the VCSELs need to be bonded directly to the pixels. This has the advantage of low parasitic capacitance, better optical alignment and higher scalability. There have been a number of previous reports of techniques for bonding VCSELs to integrated circuits and other substrates. Pu et al. were the first to report the bonding of an array of VCSELs directly to a foundry fabricated integrated circuits [1]. The 8 x 8 array was bonded using a co-planar flip chip bonding process. More recently, Krishnamoorthy et al. reported bonding a 2 x 10 array of 970nm VCSELs to a CMOS chip [2]. This was also a co-planar bonding process, however the substrate was not removed and the VCSELs emitted through the GaAs substrate. Both of these co-planar techniques were based on previous work on the bonding of SEED arrays [3,4]. Matsuo et al. [5] bonded a VCSEL wafer to a silicon substrate with polyimide, removed the VCSEL substrate and processed the wafer in to individual VCSELs. Maracas and coworker [6,7] used a probe transfer technique to place individual VCSELs on a CMOS chip and Smith and coworkers [8] used a fluidic self-alignment technique. These earlier reports showed that VCSELs were robust and could be transferred to another substrate without significant change in electrical/optical characteristics. McLaren et al. [9] reported the thermosonic bonding of an 8 x 8 array to a fused quartz substrate which enabled the VCSEL output to be viewed through the transparent quartz. 90μm square bonding pads on a 250μm pitch were used and the substrate was not removed.

This paper reports three techniques for bonding arrays of individual VCSELs to integrated circuits. The optical and electrical measurements of these bonded structures are measured and results compared with each other and those reported by other research groups.

II. General Fabrication Considerations

Designing a process for bonding VCSELs directly to locations embedded in an integrated circuit requires making several fundamental fabrication decisions, such as 1) whether or not to remove the VCSEL substrate, 2) the method of current confinement in the VCSELs, 3) the wafer design and 4) the general bonding concept. These design decisions should be based on the specifications for speed of operation, thermal and electrical resistance, robustness of the bonding, the number and difficulty of the process steps and the scalability of the process. For the research presented here, scalability of the process to $\geq$ 1000 VCSELs was considered the most important design specification [10]. Since VCSELs are high speed devices [11], the design of the VCSEL driver circuit appears to be the frequency limiting factor and new driver designs are eliminating this problem [2,12]. The other specifications appear to be more a function of the bonding technique and thus scalability to large size appears to be the primary limiting factor..

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We have chosen to investigate bonding techniques that remove the substrate leaving individual VCSELs bonded to specific locations in the integrated circuit. Removing the substrate has the primary advantage of avoiding the stress that results from joining two large dissimilar chips with multiple bonds. This stress can cause bonding failure and even crack the chips [13]. In addition the problem of covering photodetectors monolithically integrated on the electronic chip is also avoided.

Three basic bonding concepts using substrate removal are reported in this paper. All three concepts resulted in operational VCSELs bonded to either foundry fabricated integrated circuit chips or GaAs substrates. The VCSEL wafer design used in the research reported here is similar to that of a standard λ = 850nm VCSEL wafer, except the n-mirror has fewer layers than the p-mirror. This allows emission from the bottom side of the VCSEL stack after substrate removal. The VCSEL wafer also has an AlAs stop etch layer between the VCSEL stack and the substrate. The VCSELs used in this type of bonding process can be of a standard oxide or proton implantation defined design or have an air post structure. Electrical confinement by ion implantation requires the proton implantation energy to be increased over that required for top emitting VCSELs since the p-mirror is more highly reflecting and hence thicker than the n-mirror. It is also not desirable to proton implant the VCSELs from the n-mirror side after bonding and substrate removal, since the non-planar surface makes it difficult to pattern small apertures. Thus, we have chosen to use oxide confinement since it appears to be best suited for the present integrated bonding techniques and generally results in a lower threshold current. On the other hand, if the bonding process requires bonding the VCSELs to the chips before oxidation, then degradation of the VCSEL to electronic chip bonds may occur due to heating the structure to 420°C in an oxidizing atmosphere. Obtaining a smooth surface after substrate removal is also required for lasing. We have found that PA solution (H_2O_2:NH_4OH) spray etch provides an extremely good selectivity at the AlAs etch stop layer and consequently a very smooth top emitting surface. It has been suggested that several smoothing layers maybe needed in order to obtain a good lasing surface [6] , however we have found that these layers are not necessary.

All of the optical/electrical results reported here were obtained from VCSELs bonded in 4 x 4 or 8 x 8 arrays with a 250μm pitch, i.e. a density of 1600 VCSELs/cm^2. All of the VCSELs in each array were tested and 50 to 90% of the VCSELs showed good characteristics. The cause of the failed VCSELs appears to be poor contact between the VCSEL and electronic chip because of the non-parallelism between the VCSEL and electronic chip introduced by the mask aligner used to attach the two chips. The use of specialize bonding equipment should lead to a much higher bonding yield, even with much larger arrays. Improved metallurgy should also increase the yield. The bonding pads for all of the VCSELs were 30μm x 30μm.

III. Fabrication techniques

A. Co-planar flip chip bonding

The coplanar bonding process is illustrated in Figure 1 and an SEM photomicrograph of bonded VCSELs to an GaAs chip in Figure 2. The oxide confined VCSELs were fabricated by dry etching the device mesa down to the n-mirror and wet oxidizing the confinement layers. After the etch , the wafer surface has 4-5 μm steps which decrease the resolution of photolithography. Fortunately only a few micrometer resolution is required to fabricate the VCSELs and thus the photolithographic resolution is not a critical issue. The p- and n-contacts were then deposited and annealed, and a Au post was electroplated on the n-contact to a height approximately level with the p-contact. The accuracy of the electroplated Au must be controlled within 0.1μm, otherwise the bonding process has a low yield. Additional Au posts are electroplated on both n- and p-contacts in order to enhance the bonding. Another mesa surrounding this structure was then formed by dry etching down to the substrate as illustrated in Figure 1 in order to allow separation of the VCSELs when the substrate is removed by etching.

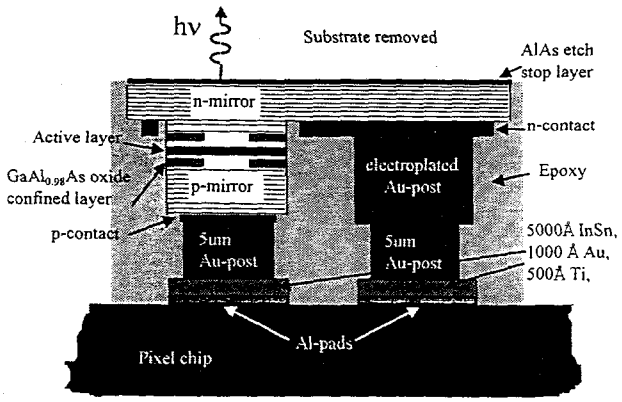

Fig.1 Schematic of co-planar flip chip bonding structure

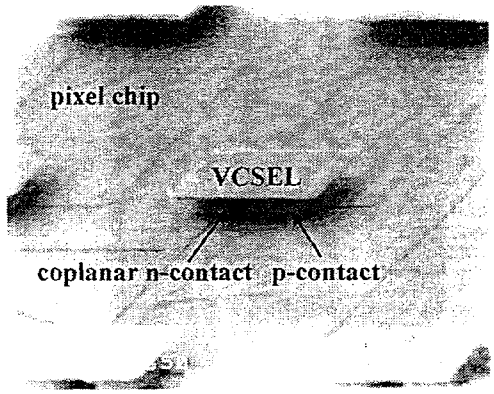

Fig.2. SEM Photomicrograph of VCSEL's co-planar bonded to a GaAs chip

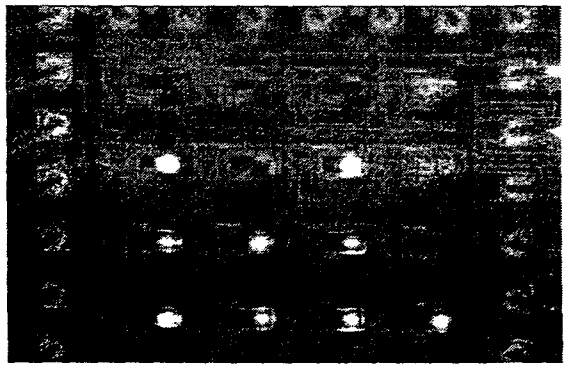

Fig.3 A 4 x 4 array of VCSELs co-planar bonded to a CMOS transmitter chip with 9 of the VCSELs turned on.

Since the bonding pads of foundry fabricated ICs are Al, Ti/Au/InSn was deposited onto these pads in order to form a strong bond with the VCSEL chip. The flip-chip bonding of the VCSELs was accomplished by mounting the VCSEL and pixel chip onto separate glass plates with crystal bond, aligning them in a mask aligner using IR and then bonding the two chips together with pressure. After the alignment, the unit is transferred to a hot plate and heated to 180°C for 15min which melts the InSn and forms a eutectic with the Au pad. After the bonding, epoxy is wicked in between the chips to enhance the robustness of the structure and protect the pixel chip from attack by the subsequent polish and selective etch used to remove the GaAs substrate. This process leaves free standing VCSEL mesas bonded to the electronic chip as shown for a GaAs chip in Figure 2 and 0.5μm CMOS chip in Figure 3.

Figure 3 shows a 4 x 4 array of VCSELs bonded to a CMOS transmitter chip with nine of the VCSELs turned on. Although this structure does not appear robust, the VCSELs operated for several months in the laboratory with I_{th} as low as 2.4mA and V_{th} = 2.1V. This demonstrates that this technology is workable without sacrificing the fundamental characteristics of the VCSELs.

The VCSEL/CMOS bonded chips were composed of a 4 x 4 array of electrically driven pixels. Each pixel contained a four stage CMOS voltage amplifier and an NMOS single stage current driver with a parallel pre-biasing transistor. The CMOS chips were fabricated with 0.5μm design rules by Hewlett Packard through the MOSIS Foundry Service. The VCSEL/MESFET bonded chips were 8 x 8 arrays of pixels with each pixel composed of three MSM photodetectors, an XNOR gate, an AND gate and a four stage VCSEL driver. The pixels performed the logic required for a database filtering system. The GaAs MESFET chips were fabricated by Vitesse through the MOSIS Foundry Service.

B. Top-Bottom contact bonding

The top-bottom contact bonding process is illustrated in figure 4. This process is simpler than co-planar flip chip bonding since the coplanar electroplating is not necessary and only one mesa etch is required. The simple square shape of the VCSEL mesa also makes the structure more robust. Depositing the p-contacts is the first step in the process followed by electroplating Au posts. The VCSELs mesas were then isolated by dry etching into the substrate and oxide confinement formed by heating in steam at 430C. The metalization were carried out before the etching, because these VCSEL mesas are about 9um high which reduces the resolution of the photolithography. Ti/Pt/Au were used for the p-contact instead of Ti/Au. Pt serves as a diffusion barrier to prevent Au diffusing deeply into the device during the 430°C oxidization. The electroplated Au post also protects the ohmic contact from the corrosive environment. An additional Au-post on the pixel chip was electroplated in order to facilitate the formation of the top contact.

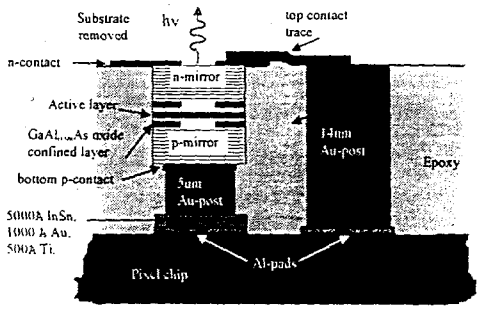

Fig.4. Schematic of top-bottom contacts structure

Fig.5. SEM Photomicrograph of VCSEL's top-bottom contacts bonded to a GaAs chip

The bonding and substrate removal process is similar to that used in the coplanar flip chip, except the bonding alignment is not as critical, because there is only one solder bonding pad for each VCSEL. Furthermore, there is no co-planar height accuracy problem. Thus, higher bonding yield can be expected.
After substrate removal, the epoxy, which covers the top of the Au-posts on the pixel chip, was removed with plasma etching. Then, the n-contacts of the VCSELs and the contact trace between the VCSEL n-contact and the Au-posts of the pixel chip were deposited and annealed. The surface metal serves as a mask for the epoxy plasma etch. The epoxy between the VCSEL and the Au-post is left to support the top contact metalization.

Figure 5 illustrates part of an 8 x 8 array of VCSELs bonded by this technique to a GaAs substrate. These VCSELs had ~ 0.7mW of output power and low resistance and threshold current.

C. Top-top contacts bonding

Another approach to attaching individual VCSELs to an electronic chip is to "glue" the entire wafer, VCSEL layers face down, on to the electronic wafer using an non-conducting material such as epoxy or polyimide [5] as shown in Figure 6. The non-conductive bonding material should be able to withstand the 430C oxidation temperture and have low shrinkage after curing, otherwise the very thin epitaxial layer will be distorted by the bonding material. The processing begins by attaching the VCSEL wafer with epoxy, removing the substrate from the wafer, depositing the n-contacts and then dry etching down to the p-mirror forming an array of 40μm x 40μm mesas. These mesas are not as tall as those of the co-planar flip chip structure because the n-mirror is thinner than the p-mirror. P-contacts were then deposited and isolation mesas were wet etched. The epoxy served as an wet etch stop layer and was removed with a plasma etch. After the mesas were oxidized to form the electrical confinement, polyimide was employed to cover these separated VCSEL mesas and to better hold them in place. Then the polyimide was patterned and gold traces were evaporated and electroplated

to connect the p- and n-contacts to their corresponding bonding pads on the pixel chip. The polyimide planarizes the surface and the etched sidewalls are 45°, thus there is no step coverage problem. The resolution of photolithography is limited by the non-parallelism of the epitaxial layer after it is bonded on the electric chip.

Figure 7 illustrates part of an 8 x 8 array of VCSELs bonded to a GaAs substrate. Individual VCSELs in this array produced up to 7mW of optical power although the resistance and V_{th} for these VCSELs is somewhat higher than for the other bonding techniques. This is in part due to the large 20μm aperture.

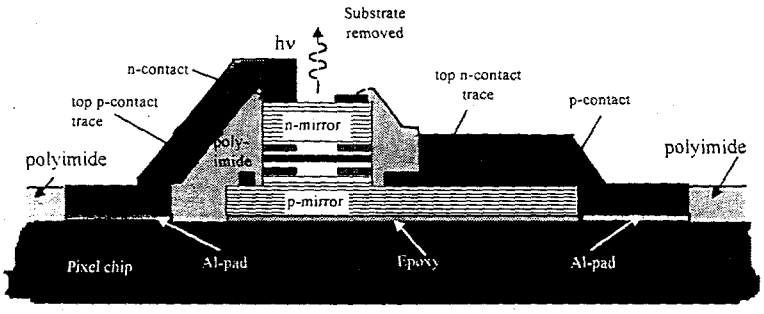

Fig 6. Schematic of non-conductive bonding structure

Fig.7. SEM Photomicrograph of VCSEL's top-contacts bonded to a GaAs chip

IV. Measured Electrical and Optical Results

Typical V-I and L-I characteristics were obtained from all of the bonded VCSELs. >50% of the VCSELs lased with good characteristics, i.e. they had a sharp lasing threshold, high output power and reasonably low threshold current/voltage. Typical values (there was only a small variation on a given chip) for the three bonding techniques of the present research are listed in Table I along with published values for bonded VCSELs from other research groups. Also listed are data from a package Honeywell commercial product and VCSELs from standard (non flip-chip) VCSEL arrays.In comparing the results listed in Table I, one must take into account the difference in aperture, since I_{th} and P_{out} increase with aperture size while the series resistance decreases [15]. In addition, different wafers and electrical confinement were used. In reality, what we want to evaluate is the bonding techniques and the effect bonding has on VCSEL performance and not the performance of the VCSEL itself. Comparing the VCSEL characteristics before and after bonding would provide the most information and would be the best method of evaluation. However, this is not possible for our techniques since our VCSELs are bottom emitting and thus the substrate has to be removed before the measurements can be made. The series resistance and V_{th} can be used to elvaluate the bonding. Table I shows that these parameters for our VCSELs are in the same range as reported for bonded VCSELs by other groups. These values can be improved by the addition of intracavity contact layers. It is also observed that series resistance of all of the flip-chip bonded VCSELs shown in the table are much higher (50-200Ω) than the standard/commercial VCSELs (20-32Ω) and the V_{th} of the bonded VCSELs is also usually higher. There several possible causes for the higher values for the bonded VCSELs: 1) The VCSEL wafers for flip chip bonding were not designed properly to reduce the contact/mirror resistance, 2) The ohmic contacts were not annealed properly, 3) The contact metallurgy is introducing a voltage drop/resistance due to the oxidation of one or more of the metal layers or 4) The bonding metal are introducing a junction. This is an area of research for all types of flip chip bonding of VCSELs.

Preliminary measurements of the bonded VCSEL capacitance gave a value of ~3pF at 1 MHz and zero bias. The value of the parasitic capacitance added by the flip chip bonding could not be obtained, but it appears to be very small.

In reviewing all of the parameters for the three bonding techniques of the present paper, it is seen that there is wide variation. This is due in large part to the use of three different VCSEL wafers and significantly different apertures. Thus, it is not possible to determine which is the best technique based on the present data.

We are presently fabricating all three structures from the same wafer with the same aperture formed to the same size at the same time. This should provided a more definitive answer to the question of "best".

Table I. Comparison of the electrical characteristics of the three bonding technique with those of other researchers.

Group	Resistance, Ω	I_{th}, mA	V_{th}, V	Aperture, μm - P_{out}, mW
Pu [1] Colorado State				
• co-planar	90Ω	3.8mA	2.1V	14μm –3.1mW
• top-bottom	50	0.8	1.5	6 – 0.7
• top-top	120	4.8	3.4	20 – 7
Kishnamoorthy [2] Lucent	150	0.9-1.0	1.4-1.5	? – 5
Matsuo [5] NTT	70	3.5	2.3	15 – 1.2
Maracas [6,7] Arizona State	90	5.5-6.4	3	40 – 1
McLaren [9] Univ. Colorado	200	1.5	1.9	? - >0.4
Smith [8] UC Berkeley	70	30	17	40 – 0.03
Morgan [14] Honeywell (Proton implanted)	29	2.7	1.55	? - 8
Choquette [15] Sandia (Oxide confined)	32	4	2.0	14 - 5
Honeywell Product HFE 4080-321	20	3.8	1.5	? - 5

V. Processing and Mechanical Characteristics

All of the bonding techniques require many processing step, some of which are simple and routine while others are difficult and can limit the yield of the array. In discussing these difficult processing steps and the quality of the bonds, it must be realized that what is difficult for a university lab, may be simple for an industrial production line. Also, the work presented here is based on a limited number of process runs and thus the processes have not been optimized.

Table II summarizes some characteristics of the three bonding techniques. The difficulties listed in the table indicate which of the processing steps require special attention, however, none of the techniques have processing difficulties that can not be sufficiently mitigated to allow the fabrication of large arrays with high yield. Probably the most important processing consideration is to make sure that the processing does not degrade the performance of the VCSELs and the electronic chip to which they are bonded. It would seem that oxidation at high temperature after metalization should be avoided if possible since it could lead to higher series resistance, although the top-bottom contact bonding technique had the lowest measured series resistance and V_{th} of the three techniques.

With regard to thermal resistance, all three of the bonding techniques and those of refs 2 and 5 should have somewhat higher resistance since the VCSELs have been etched into mesas which reduces the lateral heat flow [17]. Of the three, the co-planar flip chip bonded VCSELs should have the lowest thermal resistance since both contacts are solder bonded to the electronic chip and metal is an excellent thermal conductor. However,

the thermal resistance depends on bonding quality, i.e. the presents of an oxide or the lack of contact over the whole bonding pad. The top-top contact bonding technique should have the largest thermal resistance due to the non-conductive bonding material.

Table II. Comparison of three VCSEL bonding techniques.

Structure	Processing difficulties	Thermal resistance	Robustness
Co-planar flip chip	• Accurate height of the electroplated Au posts • Need to carefully handle after bonding	Similar to unbonded VCSELs	Thin wafer protruding out from the surface
Top-bottom contacts	• Oxidation after contact metal deposition	Similar to unbonded VCSELs	Can be surrounded with epoxy
Top-top contacts	• Metal step coverage • Oxidation after bonding & contact metal deposition	Could be high due to the high resistance of polyimide/epoxy	Large mesa "glued" to the electronic chip

Table II provides a qualitative description of the robustness of the bonding structures. The top-top bonding appears to be the most robust since the VCSELs are attached across a large area whereas the co-planar structure has the thin p-mirror layers supported 10 to 20μm above the contacting bonds. And thus, while all of these hybrid structures require careful handling, more care must be provided for the co-planar bonded VCSELs.

V. Summary

It has been shown that VCSEL arrays with good lasing characteristics can be bonded to electronic chips by three different techniques. The VCSEL characteristics of the three techniques show that the series resistance and Vth are comparable with previously reported bonding results but higher that than for unbonded VCSELs. Although the bonding qualities need further investigation to lead these techniques into practice, the techniques have the potential to make large optoelectronic arrays and maintain the high quality of VCSELs.

Acknowledgment: This project was founded in part by NSF Grant ECD9015120 and NSF/ERC Grant #9485502.

References

[1] Rui Pu, et. al., "VCSEL's bonded directly to foundry fabricated GaAs Smart Pixel Arrays", IEEE Photon. Tech. Lett. Vol.9, No.12, pp1622-4, 1997.

[2] A.V. Kishnamoorthy, L.M.F. Chirovsky, W.S. Hobson, R.E. Leibenguth, S.P. Hui, G. J. Zydzik, K.W. Goossen, J.D. Wynn, B.J. Tseng, J. Lopata, J.A. Walker, J.E. Cunningham and L.A. D'Asaro, "Vertical cavity surface-emitting lasers flip-chip bonded to gigabit-per second CMOS circuits", IEEE Photon. Tech. Lett. Vol.11, No.1, pp128-130, 1999

[3] K. W. Goossen, J, E. Cunningham, W. Y. Jan, " GaAs 850nm Modulators Solder-bonded to Silicon", IEEE Photon. Tech. Lett., vol.5, pp.776-778, July 1993.

[4] K. W. Goossen, J. A. Walker, L. A. D'Asaro, S. P. Hui, B. Tseng, R. Leibenguth, D. Kossives, D. D. Bacon, D. Dahringer, L. M. F. Chirovshky, A. L. Lentine and D. A. B. Miller, "GaAs MOW Modulators Integrated with Silicon CMOS", IEEE Photon. Tech. Lett., vol.7, pp.360-362. April 1995.

[5] S. Matsuo, T. Nakahara, K. Tateno and T. Kurodawa, " Novel technology for hybrid integration of photonic and electronic circuits", IEEE Photon. Tech. Lett., vol.8, pp1507-1509, November 1996.

[6] S. Daryanani, H. Fathollahnejad, D.L. Mathine, R. Droopad, A. Kubes and G.N. Maracas, "Integration of a single vertical cavity surface emitting lasers integrated onto a CMOS inverter chip", Electronics Letters, vol.30, 35-36, 1995.

[7] D. L. Mathine, R.Droopad and G. N. Maracas, " A vertical-cavity surface-emitting laser appliquéd to a

0.8um NMOS driver", IEEE. Photon. Tech. Lett., vol.9, pp. 869-871, July 1997.
[8] H-J. J. Yeh and J. S. Smith, " Integration of GaAs vertical-cavity surface-emitting laser on Si by substrate removal", Applied Physics Letters, vol.64, pp.1466-1468, March 1994.
[9] T.S. McLaren, S. Y. Kang, W. Zhang, T.H. Ju and Y.C. Lee, "Thermosonic bonding of optical transceiver based on an 8 x 8 vertical cavity surface emitting laser array", IEEE Trans. Comp., Pack., Manufact, Technol., vol. 20, pp. 152159, 1997.
[10] A.V. Kishnamoorthy and D.A.B. Miller, "Scaling optoelectronic-VLSI circuits into the 21st century:A technology roadmap", IEEE J. Selected Topics Quanum Electronics, vol.2, 55-76, 1996.
[11] B.J. Thibeault, K Bertilsson, E.R. Hegblon, E.M. Strzelecka, Y. Akulova and L.A. Coldren, "High speed characteristics of low-optical loss oxide apertured vertical cavity lasers", IEEE Photon. Tech. Lett. Vol.9, pp11-13, 1997.
[12] T.C. Banwell, A. C. Von Lehmen and R.R. Cordell, "VCSE Laser Transmitters for Parallel Data Links", IEEE J. Quantum Electronics, vol. 29, pp. 635-644, February, 1993.
[13] Daniel Baldwin, "In process stress analysis of flip chip assemblies during underfill cure and environmental stress testing", seminar , University of Colorado, Sept 1998.
[14] R.A. Morgan, M.K. Hibbs-Brenner, R. A. Walterson, J.A. Lehman, T.M. Marta, S. Bounnak, E.L. Kalweit, T. Akinwande and J.C. Nohava, "Producible GaAs-base top surface emitting lasers with record record performance", Electronics Letters, vol.31 (6), 462-463, 1995.
[15] Unpublished data.
[16] K.L. Lear. K.D. Choquette, R.P. Schneider, Jr., S.P. Kilcoyne and K.M. Geib, "Selectively oxidized vertical cavity surface emitting lasers with 50% power conversion efficiency", Electronics Letters, 31 (3), 208-209, 1995.
[17] K.D. Choquette, G. Hasnain, J.P. Mannaerts, J.D Wynn, R.C. Wetzel, M Hong, R.S. Freund and R.E. Leibenguth, "Vertical cavity surface emitting lasers fabricated by vacuum integrated processing", IEEE Photon. Tech. Lett. Vol.4, No.9, pp 951-953, 1992.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.