Comparative hot carrier induced degradation in 0.25 μm MOSFETs with H or D passivated interfaces


* LPM, UMR CNRS 5511, INSA de Lyon, 69621 Villeurbanne cedex, France
** France Telecom - CNET, BP 98, 38243 Meylan cedex, France
*** Sandia National Laboratories, Advanced Materials Laboratory, Albuquerque, NM 87185-1349, USA

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Abstract

Hot electron induced degradation in 0.25 μm, n-channel MOSFETs annealed in H2 or D2 containing atmospheres is reported. Threshold voltage and channel transconductance variations correlate with the growth of the interface state density. The spectral density of the stress induced interface states in the Si bandgap does not depend upon the anneal gas but the transistor lifetime (for a 20 % transconductance variation) is ~ 40 times shorter for H2 as opposed to D2 annealed devices.

Introduction

It has been recently demonstrated [1] that hot-electron induced degradation of the threshold voltage and channel transconductance in n-channel MOSFETs may be substantially reduced if the forming gas used to passivate the Si/SiO2 interface contains D2 rather than H2. Data was presented for devices with channel lengths ≥ 0.5 μm. In the present work, we have carried out similar experiments on 0.25 μm technology devices and characterized the degradation induced by hot-electron injection by studying threshold voltage and channel transconductance variation. Two and three level charge pumping have been used to determine the evolution of the density of interface states in the Si bandgap. The results of these studies are presented in the following.

Experiment

n-channel MOSFETs with 0.25 μm channel lengths and 10 μm widths were fabricated. The gate oxide thickness was 5.8 nm and the gate electrode, a Si/TiSi2/W stack. Single metal level devices were first outgassed by annealing in a vacuum ~10⁻⁷ torr for at least 48 hours at 550 °C. The furnace temperature was then reduced to 425 °C and backfilled with H2 or D2 containing forming gas. Annealing of the transistors in either the H2 or D2 atmospheres was carried out for one hour. Stress conditions were ascertained by applying a fixed source-drain voltage (Vsd) and varying the gate-source potential (Vgs) to obtain a maximum substrate current. Typical values of Vsd were 2.5 ≤ Vsd ≤ 4 V. The threshold voltage (Vth), channel transconductance (gmn) and interface state density (Dit) were measured as a function of electrical stress time. The Dit values were obtained using standard (two level) charge pumping with sinusoidal pulses [2] and its energy distribution in the Si bandgap via three level charge pumping [3].

Results

In Fig. 1, we show a typical curve of the normalized transconductance as a function of stress time for devices with Vth = 4 V and Vgs = 1.85 V. The filled circles are for H2 annealed transistors and the open circles for D2. If we take a 20 % gmn degradation as a lifetime criterion, we see that the D2 annealed devices have lifetimes ~ 30-40 times larger than the H2 annealed ones.

In Fig. 2, we show the energy distribution of the interface state density in the Si bandgap for a virgin device and for D2 and H2 annealed devices subjected to a 4 V Vth stress for 1272 minutes. This data was obtained using the three level charge pumping technique with an intermediate step duration of 1.2 ms [3]. After stress, we observe similar Dit distributions in terms of curve shape and energy peak positions (two broad peaks at ~ Et - 0.25 eV and ~ Et + 0.2 eV). Only the Dit level of the H2 and D2 spectra is clearly different, which seems to indicate that similar interface defects are created during hot electron injection with two different generation rates between samples annealed in H2 or D2.

Discussion

It is clear from Fig. 1 that annealing of devices in D2 containing atmospheres strongly enhances the resistance to hot electron degradation when compared to H2 annealed devices. Various sources of device degradation due to hot electron injection should be considered. At least two "intrinsic" modes involve the creation of
fixed oxide charge (of density $\Delta N_0$) and interface states (of number of states $\Delta N_i$). The evolution of the threshold voltage $V_t$ and channel transconductance can be written [4]:

$$\Delta V_t = -\frac{q\Delta N_{st}}{C_{ox}} + \frac{\alpha L \Delta N_i}{\mu_0 W C_{ox} V_{ds}}$$

(1)

and

$$\Delta g_m = \left(\frac{\alpha \Delta N_i}{1 + \alpha \Delta N_i}\right) g_m^0$$

(2)

where $\Delta N_i$ is the number of interface states averaged over the channel length $L$. $\alpha$ is a coefficient depending upon the technology, $W$ is the channel width, $C_{ox}$ the gate capacitance and $V_{ds}$ the source-drain current. For the determination of $V_t$ we assume a constant value of $I_{ds}$. If we assume that the fixed oxide charge term is negligible for a thin oxide (which may or may not be the case), then we can write:

$$\Delta V_t = \frac{K}{\alpha} \left(\frac{\Delta g_m}{g_m^0}\right) \left(1 - \frac{\Delta g_m}{g_m^0}\right)$$

(3)

where $K$ contains the constant terms in the bracket of equation (1). In Fig. 3, we plot the measured variation of the threshold voltage as a function of the parameter $-(\Delta g_m/g_m^0)/(1-\Delta g_m/g_m^0)$ with $g_m^0$ the channel transconductance prior to stress. Each point corresponds to a stress time of the same device (here the stressing $V_{ds}$ was 3.5 V). It appears that i) there is a linear relationship as expected from equation (3) if oxide charge effects are absent and ii) the slope is essentially the same for both the D$_2$ and H$_2$ annealed devices even though the stress times in the two cases differed by factors $\sim$ 30. We thus confirm that the hot electron induced degradation arises from interface state generation and the magnitude of the generation is reflected by the data shown in Fig. 2.

**Conclusion**

The present data confirms earlier measurements [1] which indicate that significant gains in device lifetime can be obtained if they are annealed in D$_2$ containing forming gas rather than the conventional H$_2$ form. Furthermore, we confirm that hot electron induced interface state creation is the primary mechanism in our case. At the present time, only a tentative model has been put forward to explain the difference between the D$_2$ and H$_2$ annealed interfaces [5], this clearly requires confirmation. Our previous experiments involving photo-assisted electron injection [6] indicated no difference in the rate of generation of interface states between samples annealed in H$_2$ or D$_2$. The present data becomes consistent with the previous only if we consider that it is the injected electron current density which is important, i.e. for the very large current densities present in the drain area where electron injection occurs, there are differences between the rates at which Si-D and Si-H bonds can absorb and dissipate energy prior to cleavage and release of H or D resulting in interface state creation. Clearly more fundamental work is necessary to elucidate the subtle differences in Si-D and Si-H bondings.

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**References**


