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0.5 μm E/D AlGaAs/GaAs HETEROSTRUCTURE FIELD EFFECT TRANSISTOR TECHNOLOGY WITH DFET THRESHOLD ADJUST IMPLANT

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A doped-channel heterostructure field effect transistor (HFET) technology has been developed with self-aligned refractory gate processing and using both enhancement- and depletion-mode transistors. D-HFET devices are obtained with a threshold voltage adjust implant into material designed for E-HFET operation. Both E- and D-HFETs utilize W/WSi bilayer gates, sidewall spacers, and rapid thermal annealing for controlling short channel effects. The 0.5 μm E-HFETs (D-HFETs) have been demonstrated with transconductance of 425 mS/mm (265-310 mS/mm) and f_t of 45-50 GHz. Ring oscillator gate delays of 19 ps with a power of 0.6 mW have been demonstrated using direct coupled FET logic. These results are comparable to previous doped-channel HFET devices and circuits fabricated by selective reactive ion etching rather than ion implantation for threshold voltage adjustment.

INTRODUCTION

GaAs-based Heterostructure Field Effect Transistors (HFETs) can provide performance advantages over MESFETs (metal-semiconductor FETs) and are becoming more widely used with the recent advances in high volume epitaxial growth systems. For many digital and analog applications, self-aligned HFET technology is advantageous for reasons of device uniformity, minimizing parasitic source resistances, and the ability to use optical lithography for sub 0.5 μm gates. Short channel effects are dealt with by utilizing a lightly doped drain (LDD) technology with sidewall spacers and although breakdown voltages are not as good as recessed-gate technology, they are suitable for many applications.

Doped-channel HFETs with undoped AlGaAs barriers and doped GaAs channels were first investigated by Hida *et al.*, demonstrating f_t of 45 GHz for 0.5 μm gates [1,2]. These depletion-mode devices were primarily designed for microwave applications. The first digital circuits using doped-channel HFETs were based on enhancement-mode HFETs and implanted load resistors with direct-coupled FET logic (DCFL) [3]. Gate delays of 24 ps were obtained for 0.8 μm HFETs. Analogous to MESFET circuit topologies, Enhancement/Depletion (E/D) technology provides more circuit options than either D-mode or E-mode technology alone. E/D HFET technology in AlGaAs/GaAs materials with doped channel HFETs has been reported with selective reactive ion etching to produce E-mode FETs from material designed for D-FET operation [4]. E/D HFETs with 0.5 μm gate lengths were used to fabricated ring oscillator circuits with gate delays of 15 ps at a power of 1 mW. In the present work, we have developed an E/D HFET technology with epitaxial structures designed for E-HFET operation and we use ion implantation to adjust the threshold voltage for the D-HFET. Using this process, fabrication is simplified relative to the selective RIE method and multiple threshold voltages can be provided without degrading the characteristics of the E-HFET.

MATERIAL GROWTH AND CIRCUIT FABRICATION

The HFET structure is comprised of a 80 Å Si-doped ($2x10^{18}$ cm^{-3}) GaAs channel grown on top of a p-type GaAs buffer (Be:$1x10^{16}$ cm^{-3}), an undoped, 150 Å $Al_{0.5}Ga_{0.5}As$ barrier, and a 100 Å undoped GaAs cap layer. A 600 Å undoped GaAs region separates the buffer from the channel and a 50 Å undoped GaAs spacer separates the channel from the barrier layer. The Si doping was chosen for an E-mode threshold voltage (V_{th}) of approximately 0.3 V. The structures were grown on 3" semi-insulating GaAs substrates in a Varian Gen II MBE system.

Circuit fabrication consisted of the following steps. First alignment marks were formed by wet chemical etching. Then Si was selectively ion implanted (1.5 or 2.2 x 10^{12} cm^{-2}, 50 KeV) in the D-HFET regions for V_{th} of either -0.5 and -0.9 V. Next came gate formation with sputter deposition of 2000 Å of $WSi_{0.45}$ followed by 2000 Å of W. The 0.5 μm bilayer gates were patterned by e-beam lithography and formed reactive ion etching [5]. Ion implantation of SiF and P was used for the LDD region (SiF, 9 x 10^{12} cm^{-2}, 40 KeV), followed by sidewall formation (0.1 μm thick silicon nitride). The source and drain implants consisted of 50 KeV Si (2.8 x 10^{13} cm^{-2}) co-implanted with P (1.5x Si dose with overlapping depth profile). The samples were rapid thermal annealed at 900 °C for 20 s in a rapid thermal annealer with the samples enclosed in a graphite-coated SiC susceptor. Ohmic contacts were formed by evaporating GeAuNiAu and alloying at 400°C for 15 sec. Two levels of metal interconnects were formed with TiPtAu metal and silicon nitride dielectric. Critical dimensions used were 3 μm lines, 2 μm spaces and 1.5 μm via holes.

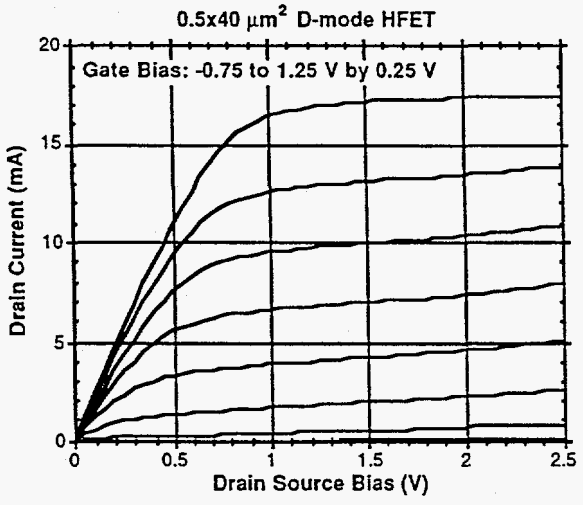

Figure 1. D-HFET I_{DS}-V_{DS} characteristics.

RESULTS

Representative DC I-V test data for the D-HFET and E-HFET are shown in Figures 1 and 2. It is seen that the HFET characteristics are well behaved with low knee voltage and good pinchoff. The E-HFET has V_{th} of 0.36 V and a high maximum transconductance, g_m (max), of 425 mS/mm, which is somewhat higher than g_m (max) of the D-HFETs. A summary of key DC parameters is given in Table 1, along with rf values for f_t and f_{max}, which come from S-parameter data that has been corrected for parasitic pad capacitances. The f_t of 47 GHz compares favorably with the 45-50 GHz values reported by Hida *et al.* [1,2], while our f_{max} values are somewhat better due to our use of the W/WSi bilayer gate for lower gate resistance. Short channel effects are controlled for the E-HFET. The Vth shift is only 0.12 V from 1 μm down to 0.5 μm for the E-HFET and 0.35-0.49 V for the D-HFET. The gate turn-on voltage V_{to}, defined as the voltage at which 1 mA/mm of gate current is

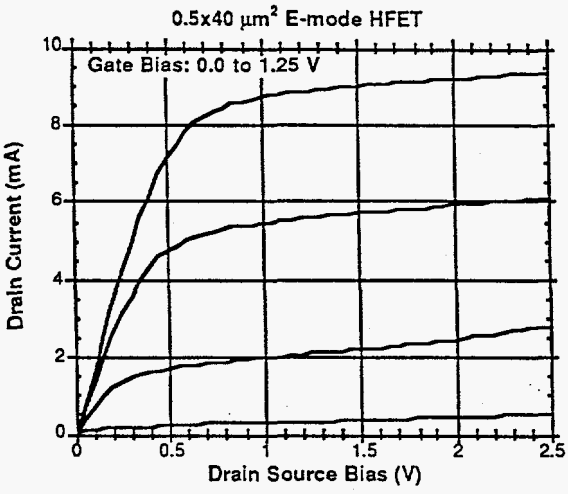

Figure 2. E-HFET I_{DS}-V_{DS} characteristics.

measured, is 0.83 V for the E-HFET. Comparable gate turn-on voltages for FETs fabricated in our laboratory are in excess of 1 V for E-HFETs without the D-HFET implant adjust step but only about 0.6 V for MESFETs. The effect of a lower gate turn-on voltage can be a reduced noise margin in digital circuits. The causes for the gate V_{to} degradation relative to E-HFETs in E-only technology are not known at present.

The performance of this technology has been demonstrated for direct coupled FET logic (DCFL), although other circuit topologies such as source coupled FET logic can be used as well. Unloaded 51-stage ring oscillators and loaded 31 stage ring oscillators with DCFL inverters were fabricated and characterized. The loaded ring oscillators were designed with 200 or 500 μm of wire between each stage. E-HFET drivers with 0.5 x 25 μm^2 gates and D-HFET loads with 0.5 x 10 μm^2 gates were used. Figure 3 summarizes the performance of these ring oscillators for power supply voltages between 1.0 and 2.0 V. Gate delays of 19 ps were obtained at 1.0 V with a power of 0.6 mW. Wire loading delays of 15 ps/mm were obtained. These results compare with 15 ps gate delays by Hida *et al.* [4]. The most likely reason for the speed difference is our use of a high V_{th} E-HFET. Proper optimization would involve adjusting the material structure so that V_{th} of the E-HFET is 0.15 - 0.2 V, resulting in higher I_D of 130-140 mA/mm and improved gate delays.

Table 1. DC and rf parameters for the doped-channel HFETs.

Device	V_{th} (V)	I_D (mA/mm) (V_G=0 V)	I_D (mA/mm) (V_G=0.9 V)	g_m (max) (mS/mm)	f_t (GHz)	f_{max} (GHz)
E-HFET	0.36	n/a	100	425	47	75
D-HFET 1	-0.50	50	n/a	265	n/a	n/a
D-HFET 2	-0.90	125	n/a	310	47	73

CONCLUSION

Self-aligned E/D HFET technology has been demonstrated by optimizing an E-HFET structure and using a D-HFET threshold adjust implant. Excellent 0.5 μm transistor characteristics have been obtained with g_m (max) of 425 mS/mm for the E-HFET, 265-310 mS/mm for the D-HFET, and f_t of 45-50 GHz for both devices. DCFL ring oscillators with 19 ps gate delays have been obtained for unloaded conditions in addition to 15 ps/mm added delay for wire loading. These results demonstrate the potential for using ion implantation for providing load or buffer transistors in any E/D HFET technology.

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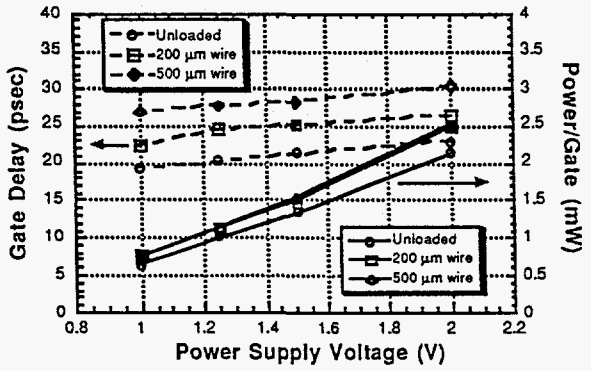

Figure 3. Ring oscillator gate delays and power consumption for a self-aligned HFET technology with a DFET

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