SEMIANNUAL REPORT # 2

"On-Chip IR Spectral Sensors By Superconducting Detector Arrays"

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TABLE OF CONTENTS

I. Project Objectives	2
II. Project Task Descriptions	3
III. Report of Progress	4
IV. Activity With Consultants and Others	15
V. Report of Non-Federal Support	15
VI. Cumulative List of Project Reports & Publications	16

ATTACHMENT :

Preprint of manuscript for : *European Conference on Applied Superconductivity.*

I. PROJECT OBJECTIVES (as stated in the Phase II Proposal)

The overall objective is to bring this new spectrometer-on-a-chip technology concept to a sufficiently mature stage of development that it can attract commercial support and be carried to market. The specific technical missions of the Phase II program are those for the *Project Tasks* listed below. These mission objectives are:

1) To establish and prove-out the fabrication processing of silicon wafers into arrays of interference-filter plates. The maturity and robustness of silicon micromachining technology will underscore the potential for meeting this goal.

2) To demonstrate that our linear-array HTS detector technology can be scaled up into square arrays of sufficient size and performance to meet the design requirements developed in the Phase I effort.

Phase II will bring the proven design through R&D, so as to demonstrate it as a viable technology with commercially attractive functionality and fabricability.

3) To expand our view of the technology so as to see it in a full engineering-systems context, and thus ensure that at the earliest stage possible conflicts can be resolved. Thus, a systems design can be accomplished that will realistically encompass all the interacting components.

4) To demonstrate, by fabrication and testing, that the components in this systems design can be combined and will deliver the functionality (e.g., spectral region, bandwidth, and

resolution) predicted by the design, and in the context of one or two simple emission-line-spectroscopy prototype applications.

5) To identify and resolve conflicts in the design and fabrication methods/processes such that the new spectrometer can meet the desired goal of multiple applications potential.

II. PROJECT TASK DESCRIPTIONS (as stated in the Phase II Proposal)

TASK 1. *GIF Micromachining R&D.* Develop processes to etch silicon wafers into large arrays of flat-plate filter elements (GIF). Use concepts and designs from Phase I for 16x16 element arrays with 256 different thicknesses. In particular we will devise an effective method to fabricate a single silicon wafer piece into this 16x16 array, by using our existing micromachining processes and facilities that utilize conventional photolithography and wet-etching methods. The target design is one with fabricated filter elements in an increasing thicknesses series, having the mode spacing of the multiple interference in each element incremented uniformly from element to element. The silicon wafer design base will be conventional semiconductor-grade, 50-mm diameter, (001) orientation, and nominally 10- Ω -cm resistivity. Note, that this processing method would lead to as many GIF elements as desired by essentially one silicon-etching step. Such, would be a powerful tool in manufacturing, at a much later stage of the technology development.

TASK 2. *Detector Array R&D.* Develop the initial design from Phase I, for 16-element HTS bolometer arrays, and extend it to 16x16-element arrays. Methods will also be developed to adapt our existing multilayer-oxide film technology to crossover connections of the square-layout arrays. The bolometers will be fabricated according to lithography design rules of 5- μ m minimum-feature-size (MFS), with layout on silicon wafers of conventional semiconductor-grade, 50-mm diameter, (001) orientation, and nominally 10- Ω -cm resistivity. Each detector element is targeted to be nominally 1x1 mm², with no less than a 25% optical-area fill factor, within the array layout. Thus, the entire bolometer array will occupy an area of nominally 32x32 mm², with the remainder of the 50-mm silicon wafer substrate devoted to lead fanout and contact-pad arrays.

TASK 3. *Spectrometer Systems Design.* Develop a complete engineering systems design for the spectrometer device and its support subsystems, including:

- a) the cryogenics,
- b) temperature control,
- c) signal multiplexing,
- d) preamplification,
- e) analog-to-digital conversion (ADC),
- f) PC software for digital signal conditioning, inverse-transform calculation, and display.

TASK 4. *Spectrometer System Integration.* Develop first prototype systems using early test units for the various system components. Characterize the component and system performance and compare with the expected functionality from the systems design base. Two prototypes will be evaluated: one for the mid-IR, and a second for the far-IR. The expected design tradeoffs are expected to be substantially different in these two ranges. Together, however, they will make clear the adaptability of the basic design to a wide range of applications areas.

TASK 5. Spectrometer Design Verification. Identify problem areas, especially areas where the system performance depends strongly on the fabrication uniformity and tolerance. Adjust and augment the design so that the system performance is more nearly balanced (optimized) in its reliance on performance tolerance of individual components and subsystems.

III. REPORT OF PROGRESS (by Task)

TASK 1. *GIF Micromachining R&D.*

We have considered two possible methods to reduce the number of processing steps required for fabrication of large silicon etalon arrays. These methods both start with silicon wafers that are ground and polished with one surface on-axis, either (001) or (111) surface normal, and with the other surface a few degrees off-axis and thus not parallel to the first side. These wedged wafers may have the property that upon anisotropic etching of the off-axis surface, with a suitable mask in place, local regions will etch differentially, becoming on-axis, and thus become re-aligned with the opposite surface. Such regions, made parallel again, would individually form etalons. If, in addition, this etalon array is laid out along the sloping direction of the wafer's wedge, the etalons will have thicknesses which step over the range of thickness of the wedge. The advantage comes in that a single processing etch step can form this complete structure. Figures 1 and 2, below illustrate our concept at this stage of its development.

In order to design the masking and etch processing more effectively, we have developed a simulator for silicon etching that is based on the Monte Carlo mathematical method. A slab of silicon atoms is established as a three-dimensional array, and the Monte Carlo routine visits each surface site (surface atom) evaluating a random number (probability) that the atom is etched. Repetitions across the surface can have many of the principal features of silicon etching if the diamond lattice rules are followed, i.e., each (001) surface site has two dangling bonds and each (111) site has a single dangling bond. This bond-count difference leads to the differential etch rate for these surface orientations. Figures 3 - 5 show side and top-down views of an etch pit being formed in a surface with (001) orientation and having a single square mask opening. The three figures show the surface at three time intervals after initiation of the etch. Note that the side view is essentially equivalent to what one would expect from a surface profilometry measurement. Figures 6 - 9 show the (001) surface being etched with a mask that has nine uniformly arrayed squares, similar to a tic-tac-toe game board. In the last time snapshot (Figure 9) the etching has arrived at "V"-shaped grooves in the silicon, as expected. Additionally, issues like surface roughness due to the etching randomness can be evaluated. We will be reporting more detailed results on these issued in future Interim Reports and in publications to come.

We have used this Monte Carlo etch simulator to predict the consequences of etching off-axis surfaces for both (001) and (111) wafers. Many of the features proposed in the schematics of Figures 1 and 2 are reproduced in the simulations, but some important differences occurred. We find that for the wedged (001) wafers, as the pits etched down, the initially wedged surface in the mask openings do not re-orient toward the (001) direction, as we show in the bottom panel of Figure 1, rather they proceed downward keeping the initial wedge tilt, and thus look much like the pits sketched in the top (on-axis) panel of Figure 1. The

simulations of etching wedged (111) surfaces also have revealed some interesting features. Here the off-axis (111) surface exposed in the mask openings etches by (slowly) forming small triangular pits, one atomic layer deep, which then widen rapidly to sweep off that top-most layer of atoms. The large differential etch rates, having a higher in-plane rate relative to a lower out-of-plane (surface normal) rate, causes the etching of the off-axis surface to progressively reorient back toward the on-axis (111) orientation. This is exactly what we are seeking. It also turns out that after the etched pit bottoms reorient toward on-axis (111), the triangular pits point up the slope, rather than down as shown in the illustration of Figure 2.

TASK 2. *Detector Array R&D.*

There was considerable activity during this performance period in a major service and repair effort for our pulsed laser deposition (PLD) system. The quadrupled Nd:YAG laser had gradually lost about half of its fluence due to progressive burns on the YAG rods and other optical surfaces. These were repaired which fully restored the beam energy. In addition, the vacuum chamber was thoroughly cleaned and the laser-beam optical delivery re-built with several improvements. Recent test films of YBCO on silicon wafers have the excellent quality we had established several years' ago, but began to lose in the Spring of this year.

FIGURE 1. SILICON (001) CRYSTAL SURFACE ETCH PITS

FIGURE 2. SILICON (111) CRYSTAL SURFACE ETCH PITS

FIGURE 3. Monte Carlo simulation of etching Si(001) crystal. Time step # one.

FIGURE 4. Monte Carlo simulation of etching Si(001) crystal. Time step # two.

FIGURE 5. Monte Carlo simulation of etching Si(001) crystal. Time step # three.

FIGURE 6. Monte Carlo simulation of etching Si(001) crystal. Time step # one.

FIGURE 7. Monte Carlo simulation of etching Si(001) crystal. Time step # two.

FIGURE 8. Monte Carlo simulation of etching Si(001) crystal. Time step # three.

FIGURE 9. Monte Carlo simulation of etching Si(001) crystal. Time step # four.

TASK 3. *Spectrometer Systems Design.*

We have carried out new modeling of etalon arrays with only 16 elements, but restricted to a narrow bandwidth of IR wavelengths near the CO₂ line at 667 cm⁻¹ (15 μm). The results indicate that such a device is promising as a first test structure for more realistic evaluation of our on-chip-spectrometer design. With a bandwidth of 150 cm⁻¹ the silicon etalon thicknesses required run from about 5 μm thick up to about 80 μm, and will function best for spectroscopy if they are *not* coated for higher reflectivity. The simulations indicate that this spectrometer will resolve Lorentzian lines down to a full-width-half-maximum (FWHM) of about 10 cm⁻¹. Eventual scaling up to 256 elements (16x16) will greatly improve on the FWHM, but at this stage a prototype with only 16 elements is an attractive possibility since it will be relatively easy to fabricate.

TASK 4. *Spectrometer System Integration.*

No work was done in this area of the program.

TASK 5. *Spectrometer Design Verification.*

No work was done in this area of the program.

IV. ACTIVITY WITH CONSULTANTS AND OTHERS

Both Professors J. I. Budnick and H. D. Drew of The Universities of Connecticut and Maryland, respectively, have interacted with this project during this reporting period, offering their professional services. (They were listed as consultants in the Phase II Proposal, and more information about them is contained there.) Fenner and Professor Budnick interact on a frequent basis (almost weekly) concerning the several joint projects they are currently involved with, including the present one. On August 17, 1995, Professor Drew visited AFR, spending the day with us, during which we reviewed many aspects of the current project. We also still have an active collaboration with Professor Drew, ongoing since 1991, concerning the nature of magneto-optical effects in our thin superconducting films.

In other activity, Fenner attended both the European Conference on Applied Superconductivity (EUCAS '95) in Edinburgh, Scotland, and the combined IEEE Transducers '95 and Eurosensors IX conference in Stockholm, Sweden. These were held in concurrent weeks at the end of June and beginning of July. At both meetings there was considerable interest in the type of sensor system being addressed in this program. Fenner presented a paper at the EUCAS '95, a copy of which is attached below. The IEEE Transducers '95 is nearly all microelectromechanical systems (MEMS) science and engineering, and thus afforded an excellent opportunity to learn considerably more about the intricate details of processing and fabrication in silicon micromachining.

V. REPORT OF NON-FEDERAL SUPPORT

During this reporting period, no non-federal support has been obtained or requested for this present DOE program.

VI. CUMULATIVE LIST of PROJECT REPORTS & PUBLICATIONS

New Technical Conference Reports From This Project (a copy is in *Attachment*, below)

1. D.B. Fenner, R.M. Carangelo, D.G. Hamblen, P.-J. Kung, and J.I. Budnick, "Infrared Bolometer and Silicon-Etalon Arrays For Transform Spectrometer On-A-Chip", *European Conference on Applied Superconductivity (EUCAS '95)*, Edinburgh, Scotland, July 1995, (and submitted for publication in conference proceedings).

Previous Technical Conference Reports From This Project

1. D.B. Fenner, R.M. Carangelo, Q. Li, D.G. Hamblen, W.D. Hamblen, J. Luo, and J.I. Budnick, "Design of IR Detector and Filter Arrays For A Transform Spectrometer On-A-Chip", *Materials Research Society* meeting, selected for oral presentation in Symp. H, Boston, MA, 29 November 1994.
2. D.B. Fenner, "Critical Technologies For Connecticut, Opportunities in Advanced Opto-Electronic Materials", invited talk given to the Institute of Materials Science, University of Connecticut, Storrs, CT, 9 December, 1994.
3. D.B. Fenner, R.M. Carangelo, Q. Li, P.A. Rosenthal, and J.I. Budnick, "Infrared Spectrometer On-A-Chip Utilizing High-Tc Superconductor Thin Films", abstract submitted and accepted for oral presentation, *Connecticut Microelectronics and Optoelectronics Consortium Symposium*, Yale University, 16 March 1995.
4. D.B. Fenner, R.M. Carangelo, Qi Li, P.A. Rosenthal, and J.I. Budnick, "IR Transform Spectrometer-On-A-Chip", *American Physical Society*, San Jose, Mar. 1995, abstract in *Bull. Am. Phys. Soc.*, Vol. 40, p. 161 (1995).
5. F.J. Dunmore, H.D. Drew, Qi Li, and D.B. Fenner, "Plasmons and Magneto-Plasmons In Superconducting YBCO Films", *American Physical Society*, San Jose, Mar 1995, abstract in *Bull. Amer. Phys. Soc.*, Vol. 40, p. 570 (1995).

Infrared Bolometer And Silicon-Etalon Arrays For Transform Spectrometer On-A-Chip *

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Abstract. This paper describes a new application for HTS thin-film bolometers in instrumentation for infrared (IR) spectroscopy. The design and a development feasibility study for this spectrometer are presented. The bolometers are fabricated in an array from a single thin film of YBCO, epitaxially grown on a suitable substrate. An array of silicon plates (i.e., array of solid etalons) is used to introduce interference fringes into the IR irradiation incident on each detector element. The instrument utilizes the transform technique and thus will enjoy both the high-optical-throughput and the multiplex advantages. Model simulations show that arrays of 256 elements can yield excellent calculated spectra (inverse transforms) based on realistic design parameters. No dispersive or moving optical parts are used, which is of great practical value and will allow a very compact and rugged on-chip spectrometer.

1. Introduction

Infrared (IR) spectroscopy provides a powerful, flexible and widely used method of compositional chemical analysis. This is especially true for spectroscopy techniques that rely on transform methods, which can deliver both excellent sensitivity and resolution. Existing instrumentation technologies for IR spectroscopy include scanned dispersive monochromators and Fourier-transform IR (FT-IR) instruments, but these have limitations intrinsic to their design. IR spectrometers typically use dispersive optical elements or beamsplitters and mechanically-scanned mirrors. The dispersive methods are limited in optical throughput due to the slit entrance, and the transform methods currently suffer from large size, high cost, and slow data acquisition. Both methods also suffer from relatively narrow wavelength ranges inherent in the choice of optical materials, relatively complex designs, and bandwidth of the required high-sensitivity detectors (e.g., HgCdTe).

2. Spectrometer Instrument Design

We describe here a new application for HTS thin-film IR detectors, as bolometer arrays in IR spectroscopy instrumentation [1,2]. In the basic design, an array of solid-plate Fabry-Perot etalons is micromachined from a silicon wafer. Each element of the etalon array is then optically aligned with an element of an array of HTS broadband IR detectors [3]. A schematic view of this spectrometer concept is shown Fig. 1. The insert there shows cross-

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sectional views of the silicon wafers, one fabricated into the etalon array, and the other used as a substrate for the HTS bolometer array. For bolometers formed on silicon, an yttrium-stabilized zirconia (YSZ) buffer layer is used [3,5].

Fabry-Perot interferometers have been proposed with multiple-mirror designs [6], and it has been suggested that if an etalon is scanned over mirror spacings that are a large multiple of the minimum distance then a Fourier transform is effected [7]. In our design, no mirror scanning occurs, rather many fixed (solid) etalons operate optically in parallel and have a large multiple in the range of etalon plate thicknesses. With a suitable choice of (distinct) thicknesses for these silicon etalons, the array of outputs from the bolometers constitutes a spectral transform of the incident IR, i.e., the interferogram [4]. Computer transform-inversion reconstructs the incident spectrum based on a knowledge of the fringe pattern of each etalon. The high-throughput and multiplex advantages of Fourier-transform infrared (FT-IR) spectrometers are obtained, in addition to the advantage of electronic scanning without moving opto-mechanical components. Silicon is well known to have excellent transmission properties throughout most of the IR, and cryogenic operation freezes out the free carriers improving suitability as an etalon [8].

3. Experimental

HTS thin films of $\text{YBa}_2\text{Cu}_3\text{O}_{(7-8)}$ (YBCO) are formed epitaxially by pulsed laser deposition (PLD), and patterned into arrays in a single mask-layer lithography and wet etching, as

Figure 1. Schematic of spectrometer-on-a-chip instrument design, with four elements.

previously described [3,5]. Four-element arrays have been operated as transition-edge detectors with small pieces of various thin silicon wafers on each, and indeed the fringes were observed in the mid-IR spectra with spacings as expected [1]. We are currently exploring methods to fabricate 16-element and then 256-element etalon arrays from single 50-mm dia. silicon wafers using bulk silicon etching (e.g., anisotropic KOH solution) [9]. These methods will combine the advantages of array batch processing, and HTS thin-film uniformity and device simplicity, with those of overall system ruggedness and projected low cost relative to conventional FT-IR.

Silicon etching must maintain a high quality to the wafer surfaces that will serve as faces for the etalons. Etching to completion at an etch-stop layer will likely be necessary for the highest optical quality, although operation at longer wavelengths relaxes somewhat this requirement. We find that high-finesse will not be needed or desired in our spectrometer, and hence surface quality, parallelism, and reflectivity are not expected to be difficult issues in fabrication and processing.

4. Spectrometer Simulations

A detailed mathematical model has been constructed of the optical (IR) and electronic function of an array of silicon etalons, together with a spectrally-integrating, HTS detector array [4]. Model simulations show that arrays of 16x16 (256 elements) can yield excellent calculated spectra (inverse transform) based on realistic design parameters. The solid etalon thicknesses must be carefully selected so that the resulting fringes optimally sample the spectrum of the incident IR radiation. A typical choice of array thicknesses would be a uniformly-stepped wafer surface, but we have evaluated other possibilities as well. Front- and back-side coating (e.g., gold film) of the etalon array can increase the finesse of each etalon, as needed, and we include this as a model parameter. As with conventional FT-IR, the interferograms can be processed by various schemes, including utilization of the technique of apodization, as we have shown. The electronic scanning method of our design will allow additional smart-sensor interferogram manipulation for adaptation to specific user needs.

The fringe pattern transmitted through a simple etalon follows the well known Airy's formula, which is readily adapted to asymmetric front and back reflectivities as may be useful in our design [10]. Let the thicknesses of the M -element etalon array be d_j , for $j = 0, 1, 2, \dots, M-1$ ($j=0$ is an unfiltered reference etalon). Then the fringe mode spacings will be Δv_j , and the transmission spectral functions $T_j(v)$, where typically $\Delta v_1 \approx$ bandwidth of interest, and $v_{M-1} \ll \Delta v_1$. Next we cast the IR frequency v into discrete form as v_i , for $i = 1, 2, \dots, N$ ($N \gg M$), and the incident irradiation $I(v)$ becomes I_i and the transmissions $T_j(v)$ become the rectangular matrix Ω_{ij} . We can define an instrument function $Z_{mn} = \Omega_{mi}^T \Omega_{in}$, where ideally $Z_{mn} = 0$, for $m \neq n$, i.e., functions $T_j(v)$ are orthogonal. The interferogram, or transform of $I(v)$, is then $V_j = \Omega_{ji}^T I_i$ (i.e., the voltages from the detector array). This can be adjusted with respect to the instrument function, as $U_k = Z_{kj}^{-1} V_j$, and an inverse transform calculated as $P_i = 2 \Omega_{ik} U_k$, where ideally $\text{Limit } P_i \rightarrow I_i$, for sufficiently large M . Figure 2 shows two examples of computed inverse transforms for a 128-element design, with etalon surface reflectivity 0.35, operated in the mid-IR. Results for two incident spectra are shown, the first has a single Lorentzian peak and the second was composed of three such peaks with distinct widths and center frequencies. No apodization or other filters were used.

Overall quality in P_i is dependent on obtaining both near orthogonality (sharply peaked Z_{mn}) and spectral-sampling completeness in the bandwidth of interest. Optimum design requires a compromise in the etalon parameters, and for a fixed number of array elements it is found that high finesse can give excellent orthogonality but results in very poor sampling completeness and hence poor spectrometer performance. Low-finesse requirements

Figure 2. Simulated inverse transform spectra (X) for two incident spectra (solid lines).

assist greatly in achieving a practical design, since minor surface roughness and a small optical loss in the bulk silicon primarily just reduce the maximum attainable finesse.

5. Conclusions

We have shown that this new spectrometer concept is feasible if careful attention is paid to overall system design. Model simulations have allowed us to explore detailed configurations and reject many that do not provide an acceptable transform function. Silicon wafers at 80-90 K and bulk-etching methods will provide suitable etalon arrays, and YBCO thin films will enable arrays of broadband-IR detectors that can readily be integrated with the etalon array. Prototype components for this spectrometer have been successfully fabricated.

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