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Ultracapacitor/Battery Electronic Interface Development

Final Report

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1. Executive Summary

A flexible, highly efficient laboratory "proof-of-concept" Ultracapacitor/Battery Interface power electronic circuit with associated controls was developed on a cost-shared contract funded by the U.S. Department of Energy (DOE), the New York State Energy Research and Development Authority (NYSERDA), and the General Electric Company (GE). This power electronic interface translates the varying dc voltage on an ultracapacitor with bi-directional power flow to the dc bus of an inverter-supplied ac propulsion system in an electric vehicle application. In a related application, the electronic interface can also be utilized to interface a low-voltage battery to a dc bus of an inverter-supplied ac propulsion system. Variations in voltage for these two intended applications occur (1) while extracting energy (discharge) or supplying energy (charge) to an ultracapacitor, and (2) while extracting energy (discharge) or supplying energy (charge) to a low-voltage battery.

The control electronics of this interface is designed to be operated as a stand-alone unit acting in response to an external power command. However, the interface unit's control is not configured to provide any of the vehicle system control functions associated with load leveling or power splitting between the propulsion battery and the ultracapacitor in an electric or hybrid vehicle application.

A system study/preliminary design effort contained two sub-tasks:

1. Established the functional specification of the interface unit, including voltage, current, and power ratings, to meet the program objectives and technical goals for the development of a highly efficient ultracapacitor/battery electronic interface unit.
2. Performed a system/application study of a hybrid-electric transit bus including an ultracapacitor and appropriate electronic interface.

The maximum power capability of the ultracapacitor/battery electronic interface unit is 25 kW. A hard-switched dc-dc converter topology using Integrated Power Module (IPM) technology was selected based on a size, weight, cost, and efficiency trade-off analysis performed during the preliminary design. System design of the bi-directional interface constrained the maximum dc voltage of the ultracapacitor or low-voltage battery to be less than the minimum voltage on the dc link of the ac propulsion system, even during transient conditions. System analysis showed that an advanced hybrid-electric propulsion system utilizing an ultracapacitor, with near-term electrical characteristics, provides substantial improvement in fuel economy and battery life. Improvements in fuel economy and battery life are functions of the actual driving cycles. For example, using an ultracapacitor to provide a power boost function for operation on the Central Business Cycle (CBD-14) projects a 21% increase in fuel economy and a 118% improvement in traction battery life, compared to a transit bus with a similar hybrid propulsion system without an ultracapacitor. Analysis for a heavily congested urban cycle typical of the M15 cycle in New York City projects a 19% increase in fuel economy and a 190% increase in traction battery life.

Two Ultracapacitor/Battery electronic interface units were fabricated and functionally tested in the laboratory using a 25 Farad, 150-V ultracapacitor. GE laboratory tests showed that program goals to develop a highly efficient interface system have been achieved. For example, measurements show the interface unit's efficiency to vary from 95.3% to 98.4% for a range of 20% to 100% of rated power over the majority of rated current/voltage plane. The first interface unit was delivered to DOE laboratories in Idaho Falls, Idaho and is fully operational. With the submittal of the final report, all deliverable items on the contract have been completed on schedule.

Figure 1. Power circuit schematic.

voltage, allowing 75% of the total stored energy to be controlled. This reduction of capacitor voltage over a two-to-one range also requires the capacitor current to vary over a two-to-one range to achieve a constant maximum power charge and discharge capability. Beyond the two to one range, separate voltage and current limits are provided to protect the interface and the energy storage components.

During conditions of regenerative braking, the dc bus acts as the source and provides power to charge the ultracapacitor or low-voltage battery. The voltage on the dc bus varies over a less than two-to-one range from motoring to regenerating.

For the purpose of the specification, it is assumed that the voltage range of the ultracapacitor is from 150 V to 300 V. The dc current into the interface varies from 83.3 A at 300 V to 166.7 A at 150 V. The voltage range of the low-voltage battery is also assumed to vary from 300 V to 150 V, resulting in the same current requirements for the interface circuit as in the ultracapacitor interface. The voltage from the dc bus is assumed to vary over a range of 300 V to 400 V. To maintain a maximum power capability of 25 kW requires a current rating of 83.3 A at 300 V and 62.5 A at 400 V.

The same power electronic components are used in all conditions. The controls must be capable of controlling the maximum voltage and the maximum current; i.e. 400 V and 166.7 A. If it is desired to test and evaluate an ultracapacitor or low-voltage battery with a dc voltage capability of, for example, 125 V, then the maximum dc current would be limited by the interface to 166.7 A, and the maximum power would be limited to 20.8 kW. Duty cycle limitations in the dc to dc circuitry will provide a lower limit on the minimum value of ultracapacitor voltage. Although the dc-dc hardware is capable of operating down to approximately 10 V, the minimum value of the ultracapacitor voltage is currently limited to 25 V in the software.

2.1.1 Input Power Requirements – Low Side DC Bus

Ultracapacitor/Battery Interface electronics is required to have a bi-directional current capability to allow both discharge and charge of the respective energy storage system. Maximum input power

rating for this laboratory breadboard unit is 25 kW, i.e., 25 kW output from an ultracapacitor or from a low-voltage battery and also 25 kW output from the inverter when the energy storage unit is being charged during regenerative braking.

2.1.2 Ultracapacitor

The ultracapacitor is assumed to operate over a voltage range to utilize and extract 75% of its stored energy. Therefore, the terminal voltage of the ultracapacitor device and also the interface circuit varies over a 2:1 range. Preliminary interface requirements (consistent with the EGG-EP-11039 report requiring the ultracapacitor terminal voltage to always be less than the dc link of the inverter) are to operate the ultracapacitor device from a minimum of 150 V to a maximum of 300 V. The maximum current and voltage envelope is plotted in Figure 2. Since the dc voltage on the ultracapacitor, battery, and dc bus do not change sign, the direction of the dc current must reverse in order to provide a bi-directional power capability at the electronic interface. This is shown as an area of capability with a negative current. It is a design goal for the interface circuit to be capable of bench testing ultracapacitors with voltage ratings below 150 V at reduced power levels, provided that the interface circuit maximum current limit is not exceeded, as shown by the dotted lines in Figure 2. In addition, there will be a duty cycle limitation that will ultimately limit the absolute minimum voltage of the ultracapacitor during these tests outside the "normal" operating range.

2.1.3 Battery

The low-voltage battery power is limited by the interface capability to a maximum value of 25 kW. The battery voltage is also constrained to operate within the same two-to-one voltage range (150 to 300 V) as the ultracapacitor. Therefore the interface current requirements are the same and the operating area is as shown in Figure 2.

2.1.4 High Side DC Bus

The regenerated power returned to the "high side" dc bus (i.e., traction drive dc link) is also limited by the interface capability to a maximum value of 25 kW. The dc voltage at the interface ranges from a minimum of 300 V during motoring to a maximum of 400 V during regeneration. Maintaining a constant 25 kW requires the current to be 83.3 A at 300 V and 62.5 A at 400 V. The area of capability is shown on Figure 3. Notice that there is no overlap in the areas shown on Figures 2 and 3. This is because the voltage on the low voltage side of the interface must always be less than the voltage on the high voltage side of the interface as shown on Figure 1.

2.1.5 Under and Overvoltage Limiters and Protection

Undervoltage limiters are integrated into the controls to maintain a minimum voltage on the low-voltage side of the interface. During a discharge of the low-side bus, voltage on the ultracapacitor or battery will gradually collapse as stored energy is removed. As the voltage approaches the undervoltage limit, the control will begin to inhibit further discharges of the low-voltage bus and maintain the minimum voltage.

2.2.1 Transit Bus Driving Cycles

A system/configuration study was performed to determine the relative merits of using an ultracapacitor local energy storage system in an advanced hybrid-electric propulsion system on a full-size 40-ft transit bus. Three different transient driving cycles were used for this system study. The Central Business District Cycle (CBD-14) is the cycle commonly used for emissions testing of transit buses on chassis dynamometers. This cycle contains 14 sub-cycles; each sub-cycle is 40 seconds in duration. The CBD-14 sub-cycle requires the vehicle to accelerate from zero to 32 km/hr (20 mph) in 10 seconds. Total time for the CBD-14 cycle is 580 seconds, while the theoretical distance is 3.3 km (2.05 miles). Average speed for the CBD-14 drive cycle is 20.3 km/hr (12.6 mph), as summarized in Figure 4.

Figure 4. Driving cycles used in system/configuration study.

A second driving cycle used in this system analysis is representative of a highly congested urban cycle, derived from the New York City Transit (NYCT) M15 route. The M15 route in Manhattan is one of the most heavily traveled transit routes in the country. Approximately 58,000 people ride the M15 route each business day. The route traverses many of Manhattan's busiest and most congested neighborhoods including Harlem, the Upper East Side, east Midtown, Grammercy Park, the East Village, Chinatown, Foely Square and the Financial District of Lower Manhattan. The M15 Route is depicted on Figure 5, which also highlights interconnections with other bus and subway lines in New York City. Given the extent and variety of areas served by the M15, the route has very high passenger loadings throughout the day and requires about 76 buses to maintain service during peak hours.

The route is approximately 8.1 miles long from 126th Street Depot to South Ferry. NYCT has introduced limited stop (express) service along the First and Second Avenue segments of the route in addition to regular local bus service to accommodate those passengers traveling longer distances along the route. Running times for the M15 vary substantially by both time of day and direction. Running times on a normal weekday take from 1 to 1.5 hours between 126th Street and South Ferry, while limited stop buses typically save from 11 to 17 minutes over local buses on weekday runs. Stops for local service are every 2 to 3 blocks, while the average stop spacing for the limited service (express) bus is every 7 to 8 blocks, or 0.6 km (0.375 mile). Average speed for buses on the M15 route varies from approximately 8.6 km/hr (5.4 mph) to 17.3 km/hr (10.8 mph). A brief study² of actual transit bus service on the M15 route was undertaken using existing NYCT buses in revenue service. This study indicated that buses on the M15 route spend on average over fifty percent of their time either accelerating or decelerating. Only approximately six percent of their time is spent at cruising conditions, and the remainder of the time is spent stopped at bus stops, traffic lights, or in traffic congestion. Based on this analysis, load leveling of the transit bus propulsion source in a hybrid vehicle for routes or driving cycles similar to the M15 is expected to be advantageous in the reduction of exhaust emissions.

An M15 driving cycle, based on the above detailed description of the M15 route and bus operation, was developed for further system analysis and computer simulation using ultracapacitors to load level the propulsion source in an advanced hybrid transit bus. Figure 4 shows the resulting M15 bus driving cycle speed versus time profile. Average speed of the M15 driving cycle is approximately 10.4 km/hr (6.4 mph) and the total cycle is assumed to be 1500 seconds duration. This M15 drive cycle represents both suburban and heavily congested urban driving with average speed within the range reported for the NYCT M15 route.

A third driving cycle used in this system analysis is representative of an urban cycle, derived from a Capital District Transportation Authority (CDTA) route. This drive cycle was derived from an actual transit bus while operating on a route near Schenectady, in upstate New York. Driving cycle speed versus time profile was based on data recorded by instrumentation on a CDTA transit bus during revenue service operation at rush hour on September 12, 1997 while driving its normal route. Maximum speed recorded while operating the route was 64 km/hr (40 mph). This route contained several high rate accelerations and also a significant amount of idle time. Time duration of the portion of the measured speed versus time profile used to represent this drive cycle was 663 seconds, while the average speed was only 9.1 km/hr (5.7 mph). Figure 4 shows the resulting CDTA drive cycle speed versus time profile. The CDTA cycle is the most aggressive of the three transit bus driving cycles shown in Figure 4 and requires the highest power during acceleration.

Figure 5. M-15 bus route, New York City.

2.2.2 System Simulation Analysis

System analysis, using computer simulation tools developed on other GE projects, is used to project the potential benefits by using an ultracapacitor to load-level the hybrid bus propulsion source for each of the three driving cycles shown in Figure 4. Computer system simulations were run for each of the three driving cycles shown in Figure 4 to establish a baseline. Transit bus (vehicle) parameters³ for the system simulation were based on the New York State Consortium true-low floor hybrid-electric transit bus, as summarized in Table 2.

2.2.3 Ultracapacitor and Electronic Interface Model

A simple RC model is used in the simulation to represent an ultracapacitor for providing a "power boost" during periods of vehicle acceleration and a "power absorber" during regenerative retarding while the vehicle is decelerating or holding speed on a downhill grade. Interface of the ultracapacitor to the hybrid-electric drive system and energy storage battery is provided by an ultracapacitor/battery electronic interface unit, similar to the unit being developed on this project. For the purpose of this system study, the ultracapacitor interface unit is assumed to have a constant, one-way efficiency of 96%.

The value of the ultracapacitor time constant (internal resistance multiplied by capacitance) used in this system analysis is based on near-term projections of ultracapacitors that are being developed for research purposes. Voltage rating of the high voltage side of the interface is assumed to be 400 V dc, while the operating range of the ultracapacitor is assumed to be limited to a minimum value of one half of the ultracapacitor maximum designed operating voltage, thus allowing 75% of the energy stored in an ideal ultracapacitor to be extracted. Ultracapacitor parameters used in the simulation are summarized in Table 3.

Table 2. Hybrid-electric transit bus parameters

Parameter	Description/Value
Vehicle Size	40 ft (12.2 m) Transit Bus
Frontal Area, A	84.3 ft ² (7.83 m ²)
Drag Coefficient, Cd	0.55
Tire	Michelin 305/70R22.5 XZU2 (525.4 Rev/Mile, 18.34" Loaded Radius)
Tire Friction	0.11 lb/lb
Seated Load Weight (SLW)	35,000 lb* (15,900 kg)
Gross Vehicle Weight (GVW)	44,000 lb (20,000 kg)
System Voltage	255V _{dc} - 400V _{dc}

Seated Load Weight (SLW) refers to the bus weight with a 150 lb (68.2 kg) driver plus a 150 lb (68.2 kg) passenger in each seat of the bus.

Table 3. Ultracapacitor parameters for system study analysis

Ultracapacitor Parameter	Assumed Value
Capacitance, C _{uc} (F)	80
Internal Resistance, R _{internal} (m ohms)	35
Ultracapacitor Voltage, V _{uc} (V _{dc})	150 < V _{uc} < 300 V
Maximum Ultracapacitor Power, P _{uc} (kW)	+/-100
Ideal Ultracapacitor Energy Storage (W-hr)	1,000

2.2.4 System Study Methodology

The methodology utilized to analyze the potential benefits of an advanced hybrid-electric propulsion system containing an ultracapacitor and appropriate electronic interface is based on performing a detailed computer simulation of the hybrid vehicle and associated propulsion system. Experience and knowledge gained on the New York State Consortium Hybrid Bus Development Program showed a strong dependence on vehicle fuel economy to the driving cycles as well as the vehicle accessory loads. To minimize the variables, this analysis assumed the total hybrid bus accessory loads to be a constant 15 kW at the battery terminals. Baseline simulations were run for each of the three driving cycles described in Section 2.2.1 with the 270 cell Ni-Cd traction battery as the only on-board energy storage unit. A second set of hybrid vehicle computer simulations were run for each of the three driving cycles using an on-board energy storage system consisting of a 270 cell Ni-Cd traction battery augmented with an ultracapacitor and associated electronic interface as described in Section 2.2.3. Control strategy, used in both the baseline and ultracapacitor augmented system simulations, forces the State-of-Charge (SOC) of all the energy storage devices to be the same at the end of the driving cycle as the initial SOC at the start of the driving cycle. This feature allows a direct comparison of projected fuel economy improvements resulting from the ultracapacitor augmented system for each driving cycle. Results from these computer simulations are shown below in Section 2.2.5.

2.2.5 System Simulation Results

Computer system simulation analysis, using a MATLAB Simulink simulation program developed by GE, of a 40 ft (12.2 m) hybrid transit bus operating at Seated Load Weight (SLW) was performed for each of the three driving cycles, i.e., CBD-14, M15, and CDTA urban cycle, as defined in Section 2.2.1. A baseline case simulation was run with the 270-cell Ni-Cd traction battery as the only energy storage unit for each of the three driving cycles. Each simulation case was repeated for an advanced system where the traction battery was augmented with a 100 kW peak power rated ultracapacitor and associated electronic interface as described in Section 2.2.3. The initial battery State-of-Charge (SOC) was set to 80% for both the baseline and the ultracapacitor augmented simulations. The initial condition for the ultracapacitor, when used in the simulation, was set for 80% of its rated stored energy, or approximately 90% of its rated voltage. At the end of the simulated driving cycle, the final battery SOC and the ultracapacitor's stored energy were the same as the initial conditions at the start of the driving cycle; i.e., the energy storage system is not depleted during the simulated driving cycle. Projection of traction battery life, via operating the system simulation over the three prescribed urban driving cycles, is based on the manufacturer's specification of battery cycle life versus depth of discharge (%C) (see Appendix B3) and SAFT's STX-600 test results⁷ that show 600,000 cycle life @ 2% Depth of Discharge and 30 °C temperature. Auxiliary Power Unit (APU) modeling of control strategy and fuel consumption in the GE Simulink system simulation is based on constant power dynamometer tests of a 100 kW alternator coupled to a Cummins 5.9 l turbo-charged diesel engine performed during the development of the APU for the New York State Consortium Hybrid-Electric Transit Bus Development Program^{3,4}. Table 4 summarizes the results of GE's Simulink system simulations.

System simulation results summarized in Table 4 show the ultracapacitor with interface very effectively load-levels the traction battery. For example, the peak traction battery discharge power is reduced by approximately 40-60% over the three driving cycles simulated, while the average traction

Table 4. Hybrid-electric transit bus/ultracapacitor system study summary

Cycle	CBD-14	CBD-14	M15	M15	CDTA	CDTA
Ultracapacitor	No	Yes	No	Yes	No	Yes
Battery Peak Power (kW _{disch} /kW _{chg})	88/144	34/121	152/122	80/96	179/272	110/166
Battery Current pk disch/chrq (A)	283/380	101/320	543/326	251/259	646/718	356/442
rms (A)	98	54	100	47	162	73
Net Energy Economy (kW-hr/mile)	4.10	3.46	6.35	5.38	8.47	6.64
Projected Fuel Economy (mpg)	3.48	4.23	2.18	2.59	1.64	2.11
(% Improvement)	-	21.5	-	18.8	-	29.1
Projected Battery Life Improvement (%)	-	118	-	191	-	294

battery current is reduced by approximately 45-55%. Likewise, net energy per mile of the hybrid transit bus per these simulations is reduced by 15-22 %, depending on the drive cycle, with the ultracapacitor augmented system. Projected fuel economy is increased by 19-29% with the ultracapacitor augmented system. Improved fuel economy is a result of the load-leveling effect on the Auxiliary Power Unit (APU). An additional benefit of the ultracapacitor augmented system is a significant improvement in the projected traction battery life during operation on the respective driving cycles. As shown by the simulation result summary in Table 4, the projected traction battery life for the advanced hybrid-electric bus is increased 118%, 191%, and 294% for the CBD-14, M15, and CDTA driving cycles, respectively for the ultracapacitor augmented system compared to the baseline system.

2.2.6 Ultracapacitor System Energy and Power Density Analysis

An ultracapacitor system is comprised of an ultracapacitor device plus a dc-dc converter and associated controls, that provides the electronic interface between the ultracapacitor and the dc link of a traction drive. Energy density (Wh/kg) of an ultracapacitor is typically shown as the total energy stored in the ultracapacitor ($E=0.5*CV^2$), expressed in units of Wh, divided by the mass of the ultracapacitor in kg. A practical design goal is to operate the ultracapacitor over a range of rated voltage down to 1/2 of rated voltage, thereby extracting 75% of the total stored energy. Energy density for a practical ultracapacitor system is therefore 0.75 times the total energy storage (Wh) divided by the sum of the ultracapacitor mass plus the mass of the electronic interface, expressed in kg. Table 5 is a summary of energy density and power density for an ultracapacitor, electronic interface, and overall energy storage system. The energy and power densities of the ultracapacitor device used in Table 5 are based on prototype units that are currently being developed for research purposes. The mass and power density for a 100 kW electronic interface unit is based on a full-scale version of the GE 25 kW electronic interface that was developed in this program.

As shown in Table 5, the energy density of the storage system is limited primarily by the energy density of the ultracapacitor device itself. Results show energy densities of the ultracapacitor system

Table 5. Projected energy and power density for a 1 kWh, 100 kW ultracapacitor system

Component/System	Mass (kg)	Energy Density ¹ (W-hr/kg)	Power Density (W/kg)
Ultracapacitor ²	200	5	500
Electronic Interface ³	50	-	2,000
Ultracapacitor System	250	4	400

1. Ultracapacitor device energy density is based on discharges to one-half of the initial voltage, i.e., $V_e \rightarrow 1/2V_e$ (extract 75% of total stored energy).
2. Ultracapacitor energy density based on DOE's near-term ultracapacitor goals, i.e., 5 W-hr/kg after de-rating for operation over half of rated voltage.
3. Liquid-cooled electronic interface, includes projected mass of unit with liquid-cooled heat-sink, but does not include external fans, pumps, or heat exchanger.

to be less than a typical EV lead-acid battery. However, power density of 400 W/kg or higher for the combined ultracapacitor system is expected to have applications in "power boost" applications to provide load leveling of systems containing high-power pulsed loads for short duration, i.e., during vehicle acceleration or regenerative braking while decelerating or holding speed on a downhill grade.

Today's ultracapacitor devices designed for automotive and hybrid propulsion systems appear to be somewhat limited in their energy density rather than in their power density. For example, if the assumed ultracapacitor's energy storage requirement in Table 3 was reduced to 500 Wh, while still providing 100 kW of peak power, then a 100 kg ultracapacitor with a power density of 1,000 W/kg would be required, and the resulting power density of the system increases to 667 W/kg. Today's Ultracapacitor devices have demonstrated power densities in excess of 1,000 W/kg.

3. Ultracapacitor/Battery Interface Hardware and Control

3.1 General Description

Today's high power 37-75 kW (50-100 hp) electric vehicle (EV) ac drives typically require dc nominal system voltages of 300-400 V. Conventional EV drives store all of the energy in the on-board traction battery. Most EV's extend their range by recovering a portion of the energy back into the battery during vehicle deceleration by using a regenerative braking technique. Figure 6 shows a block diagram of a conventional ac propulsion for a typical electric vehicle (this is also the configuration of the drive used for the Modular Electric Vehicle Program⁵, MEVP). Peak battery power of approximately 65 kW is required by the propulsion drive system (load) during vehicle accelerations. Figure 7 shows a block diagram of a system that uses two energy storage devices, i.e., a traction

Figure 6. Block diagram of conventional ac propulsion for a typical electric vehicle.

Figure 7. Block diagram of system using traction battery and ultracapacitor.

battery and an ultracapacitor. The ultracapacitor can be used to load-level the traction battery, therefore reducing the peak power that the battery is required to supply during vehicle accelerations and accept during vehicle decelerations. A power electronic interface and associated controls are used to couple the ultracapacitor to the traction battery and the load (ac propulsion system as shown in Figure 6).

3.2 Ultracapacitor/Battery Interface Control Functional Description

A functional block diagram of the laboratory "proof-of-concept" ultracapacitor interface controller developed on this contract is shown in Figure 8. External components, including the ultracapacitor, 12 V dc control power, plus external control interface are shown in this block diagram. Three major functions included in the GE design are the Ultracapacitor (UC) Interface front panel, the UC interface controller, and the UC interface power circuit. The ultracapacitor/battery interface power circuit, shown conceptually in Figure 1, also contains current and voltage sensors, plus protective circuits including dc contactors to isolate both the high and low voltage interface "positive" power terminals. Precharge/discharge relays are utilized in the start-up/shutdown sequencing of internal passive components in the interface unit. In Figure 8, the "lower voltage bus" side of the interface circuit is where the ultracapacitor or low-voltage battery is connected. The traction battery and dc link of an ac propulsion system are expected to be connected to the "higher voltage bus" in a full-scale implementation. A hard-switched dc-dc converter was selected based on size, weight, cost, and efficiency tradeoffs during the preliminary design phase of the project. An Intelligent Power Module (IPM) with integral gate drive and built-in protection circuitry was selected for the power electronic phase-leg in this prototype ultracapacitor interface unit. DC contactors plus an additional IPM switch were included to allow fast shutdown protection of the circuit during improper operation of this prototype interface unit. Production versions of the electronic interface are not expected to require the second IPM switch.

A flow-through liquid-cooled heat sink incorporated in the hardware design provides the mounting surface and thermal management for the power semiconductor (IPM) phase-leg and allows the interface to be conveniently tested on both GE-CRD and INEEL laboratory benches. The unit is packaged to allow functional, performance, and efficiency tests to be performed in the respective laboratories. The deliverable interface hardware and control software is designed for laboratory bench testing only and is not designed or packaged to be incorporated into an electric or hybrid vehicle.

Although the electronic interface unit is designed as a single 25 kW unit, a design goal is to develop a modular interface system. In future projects, ultracapacitor/battery interface units with higher power capabilities can build on the concepts demonstrated in this project. Two approaches to increasing the interface power level are (1) operate multiple, 25 kW units in parallel, or (2) modify the control design to allow operation of multiple 25 kW "phase-legs" within a single unit. The second approach has a benefit of synchronizing the individual switching devices with the potential to further reduce the ripple currents and ripple voltages on the traction battery, in comparison to the first approach where the power device switching between phase-legs is assumed to be independent from each other.

Figure 8. Proof-of-concept ultracapacitor interface controller.

3.3 Ultracapacitor/Battery Interface Design/Packaging

The objective of the project was to develop a laboratory "Proof-of-Concept" 25 kW ultracapacitor/battery interface circuit. A program goal was to demonstrate a modular design approach of an ultra-high-efficiency solid-state converter that operates with bi-directional power flow. The configuration selected "boosts" the ultracapacitor voltage up to the dc link when power flows in the direction from the ultracapacitor to the dc link, and "bucks" the dc link down to the ultracapacitor voltage when power flows in the direction from the dc link to the ultracapacitor. Packaging of the hardware is designed to allow the interface circuit to be tested on the bench both at GE and at the Department of Energy (DOE) Idaho National Engineering and Environmental Laboratory (INEEL) in Idaho Falls, Idaho. Additional control features designed into the system allow DOE to use the interface unit as a general-purpose laboratory test equipment for electrical characterization of different manufacturers' prototype ultracapacitors. Low-voltage ultracapacitors, with voltage rating less than the default minimum value of 150 V (up to the maximum current limit of 167 A), can be tested using the special "Extended Range" design features of the custom designed interface control software.

A compact flow-through liquid-cooled heat sink was selected for the interface hardware. The design of the heat sink layout allowed for future expansion to increase the interface unit's power level from 25 kW to 75-100 kW via populating the heat sink with two additional phase-legs. Figure 9 shows the final ultracapacitor/battery interface packaging. Enclosure and packaging of the prototype interface unit was based on the GE EV2000 ac propulsion drive components used in the New York State Consortium Hybrid Bus Development Program^{3,4}. Inductor L1 is mounted on the bottom side of the liquid-cooled heat sink. Laboratory development and performance test of the interface unit were performed using a prototype 25-Farad, 150-V ultracapacitor, as shown in Figure 10. DC power for these laboratory tests was supplied by a combination of dc power supply (shown in Figure 10) and a 360-V lead-acid traction battery.

Figure 9. GE 25 kW Ultracapacitor/battery electronic interface unit

Figure 10. Prototype ultracapacitor (25 Farad, 150-V) and dc power supply

4. Ultracapacitor Device Development

A sub-scale ultracapacitor device was fabricated by GE-CRD based on the technology developed on a program partially funded by the US Department of Energy (DOE), NYSERDA, and GE. This technology was developed as part of the US Hybrid Propulsion Systems Development Program⁵, which sponsored competitive research and development of technologies for alternative automotive propulsion. The GE effort on this current DOE, NYSERDA, GE funded program (contract # DE-FC07-96ID13406) fabricated a compact high-power density ultracapacitor stack with a design goal to achieve in excess of 2500 Watt peak pulse power. It should be emphasized that the fabricated ultracapacitor stack was an unpackaged laboratory prototype to demonstrate proof-of-concept. Bench testing of this device in the GE-CRD laboratory was performed primarily to demonstrate the flexibility of the ultracapacitor/battery electronic interface unit, and is not intended to indicate that a commercial ultracapacitor product based on this technology is available.

Individual ultracapacitor cells were $19.5\text{ cm} \times 19.5\text{ cm} \times \sim 0.53\text{ cm}$ ($7.5" \times 7.5" \times \sim 0.021"$) with a central active area of $16.51\text{ cm} \times 16.51\text{ cm}$ ($6.5" \times 6.5"$), the remainder being a perimeter seal. The ultracapacitor device was comprised of two modules, with 25 cells in each, connected in series. Figure 11 shows a photograph of the 50 cell stack that was fabricated. Electrical connection was accomplished via copper foil sheets, 0.01 cm ($0.004"$) in thickness and equal to the active area, placed on the ends of each of the modules. Thus, the two modules could be connected either in series or parallel. The modules were pneumatically compressed to 159 kP (23 psi) between 1.27 cm ($1/2"$) thick aluminum plates, sized to the cell active area.

The capacitance of each cell was measured via cyclic voltammetry between +2 and -2 volts at 100 mV/s scan rate. Table 6 shows selected physical and electrical properties of the cells and modules for

Figure 11. GE prototype ultracapacitor stack unpackaged

Table 6. Physical and electrical properties of cells and modules of 2500 watt device

Cell Parameters	
Cell Dimensions, cm (in)	19.5 x 19.5 x ~0.53 (7.5 x 7.5 x ~0.021)
Active Area Size, cm (in)	16.51 x 16.51 (6.5 x 6.5)
Cell Active Area, sq cm	270
Ave. Cell Capacitance, F	103.1
Capacitance Standard Deviation, F	3
Capacitance Range, F	99.5-110
Ave. Cell AC Resistance @ 1 kHz, Ω	0.012
Ave. Cell DC Resistance, Ω	0.018
Rated Cell Voltage, V	2.4
2500 W Stack Parameters	
Volume, l	1.014 (without compression plates)
Weight, kg	1.340 (without compression plates)
Modular Capacitance, F	4.48 and 4.40
Rated Module Voltage, V	60
Modular DC Resistance, Ω	0.44
Calculated Energy Content, Wh	4.44
Calculated Maximum Power, W	4100
Rated Energy Density, Wh/kg & Wh/l	3.31 & 4.38 (@ rated voltage)
Rated Power Density, W/kg & W/l	1865 & 2465 (@ 2500 W)
1 Second Constant Power, W	~2900 (for 60-30 volts in 1 second)
10 Second Constant Power, W	~900 (for 60-30 volts in 10 seconds)

the 2500 Watt device. Figure 12 shows the spread in capacitance for the 60 cells, fabricated at GE-CRD by personnel on the Ultracapacitor Development Team, and the 50 central-most selected for use in the device. By placing the 25 closest in capacitance cells in each module, the voltage spread between the highest and lowest capacitance of the 25 was minimized at full charge of 60 volts, and is calculated at 2.35-2.47 volts/cell for one module and 2.33-2.45 for the other.

Discharge performance was documented with a 250 watt constant power test, with the modules connected in parallel. These parameters were dictated by equipment limitations of 250 watts and 100 volts, the latter of which did not allow a 120 volt test of the modules in series. Figure 13 shows a discharge time of 44 seconds between 60 and 30 volts, or an energy delivery of 3.05 Watt-hours vs a theoretical 3.33 Wh ($0.75 * 4.44$ Wh).

Laboratory test of the GE ultracapacitor stack, connected to the electronic interface unit, was performed at GE-CRD and demonstrated to the NYSERDA project manager in March 1998. Current and voltage waveforms of the GE ultracapacitor stack operated with the electronic interface unit for 1 kW constant power charge and discharge is shown in Figure 14. Pulse testing of the GE ultracapacitor stack at a 1 kW power level, representing a power density of 0.75 kW/kg for the unpackaged prototype ultracapacitor stack, was successfully completed in the laboratory.

Figure 12. Cell ranking by capacitance.

Figure 13. 250 watt constant power discharge of the two 25-cell modules connected in parallel.

Figure 14. Current and voltage waveforms of the GE ultracapacitor stack operated with the electronic interface unit for 1 kW constant power charge and discharge

5. Laboratory Test Results

Laboratory tests were performed throughout the entire development of the Ultracapacitor/Battery electronic interface system. Three specific types of laboratory tests were performed: thermal characterization tests on the heat sink, functional/bench control tests of the interface unit coupled to a laboratory ultracapacitor, and efficiency tests of the power electronic interface unit.

5.1 GE-CRD Laboratory Tests

5.1.1 Thermal Tests

A custom liquid-cooled aluminum heat sink was fabricated for the ultracapacitor/battery interface unit. This liquid-cooled heat sink is a scaled version of a prototype heat sink originally developed by GE for another power electronic research project. Since the objective of the overall project was to develop the ultracapacitor/battery electronic interface unit as a general-purpose laboratory bench test unit, and not for any specific vehicle, flow-through water cooling was selected. Laboratory tests were performed to measure the pressure drop versus water flow rate and also to characterize both steady-state and transient thermal performance of the heat sink for selected water flow rates and thermal loads, including 150% of the projected losses at full power operation.

Table 7 shows the results of the heat sink hydraulic measurements for various water flow rates, including inlet pressure, outlet pressure, and pressure drop across the liquid-cooled heat sink. This data is provided to the end-user to help size a pump and heat exchanger if a closed-loop thermal system is developed.

Thermal performance of the heat sink was systematically tested in the laboratory using temperature sensors mounted in the following locations: inlet and outlet water tubes, top (component) surface of the heat sink, and the base plate of the Intelligent Power Modules (IPMs). In addition, an infra-red (IR) camera was focused on the IPM module for one selected case to provide a measurement of the internal temperature and an estimation of the IGBT junction temperature. Thermal load was applied to the heat sink via conduction loss from both of the IGBTs in the IPM module. A 500 A, current-limited, adjustable-voltage, laboratory dc supply provided power directly to the collector of the "upper" IGBT device and the emitter of the "lower" IGBT device. For example, when both IGBT's are continuously gated "on," approximately 400 A of current flows through both switches in the IPM module, producing a voltage drop across the module of 3.91 V and a total conduction loss of 1564 W. This dissipation is approximately 150% of the projected interface unit's loss when operating at 25 kW under the worst-case conditions. Results of these heat sink thermal tests for steady-state loads versus cooling water inlet flow rate and temperature are shown in Table 8.

Table 7. Heat sink hydraulic measurement test results

Water Flow Rate (gallons/minute)	Inlet Pressure (psi)	Outlet Pressure (psi)	Pressure Drop (psi)
1	0.2	0	0.2
2	1.3	0	1.3
3	8.0	3.0	5.0
4	16.5	7.7	8.8
5	25.5	10.5	15.0

Table 8. Steady-state thermal test results of liquid-cooled heat sink

Water Flow Rate (gallons/minute)	Heat Sink Inlet Water Temp. (°C)	Heat Sink Outlet Water Temp. (°C)	Heat Sink Temp. IPM Case Temp. (°C)	IPM Case Temp. (°C)
1	12.1	18.8	25	47.6
2	11.2	14.4	20	39.1
3	10.9	12.9	17.2	34.9
4	10.8	12.3	15.5	32.2
5	11.6	12.7	15	30.1

Internal device temperature, as measured with the IR camera for one selected case in Table 8 with 3 gallons per minute, indicated a temperature of approximately 124 °C. If the measured internal temperature is assumed to be approximately the junction temperature, then 3 gallons per minute of water flow is a safe operating point, even with 150% of the projected worst-case losses at the interface unit's maximum power level of 25 kW.

The final thermal bench test verified operation of the over-temperature shutdown protection feature designed into the Intelligent Power Module. Initially, the water flow rate was reduced to 1 gallon per minute with 450 A through the IPM producing a total voltage drop of 4.2 V and 1890 W dissipation. After 9 minutes of operation, the base plate temperature stabilized at 54 °C and the IR camera showed an internal device temperatures in excess of 185 °C, without any thermal shutdown. A second test was performed at 400 A, 3.9 V, and 1560 W dissipation with no water flowing through the heat sink. Within 4 minutes, a thermal shutdown occurred at a base plate temperature of approximately 96 °C, and an internal device temperature, as measured by the IR camera, of 147 °C. After cooling the IPM, a test verified that the device was not harmed by the thermal test and still functions correctly.

5.1.2 Interface Unit Functional Tests

Laboratory bench test of the interface unit was initially performed with a dc power supply and a resistive load to verify correct operation of the power circuit, front panel, closed-loop controls, and external sequencing and control signal functions. Bench tests were performed to verify calibration of the sensors and feedback parameters. Full-power laboratory tests performed at GE utilized an electric vehicle lead-acid traction battery in parallel with a 60 kW dc power supply, a 100 kW resistive load bank, and a 25 Farad, 150-V laboratory ultracapacitor. Functional tests were performed to verify correct operation of the controls, including start-up/shut-down sequencing and input control signals. Tests were performed over the entire range of electrical operating conditions (as shown in Figure 2 and Figure 3), including high-side and low-side voltage, bi-directional current, and bi-directional power using a combination of resistive, battery, and ultracapacitor loads. Stable operation of the electronic interface was observed for all of the functional tests.

5.1.3 Ultracapacitor Charge/Discharge Tests

A special test mode ("Signature" Test) was configured to facilitate Ultracapacitor/Battery interface system tests using prototype laboratory ultracapacitors at both the GE-CRD laboratory in Schenectady, NY and also at the DOE INEEL laboratory in Idaho Falls, Idaho after the interface unit delivery.

This ultracapacitor “signature” test mode is under software control and performs a precisely repeatable discharge-charge-discharge cycle of the ultracapacitor connected to the low-voltage-side of the interface unit. After the initial discharge portion of the cycle, the ultracapacitor is charged and discharged at a constant power specified by the operator via a PC interface. The charge time and discharge times for this cycle are also specified by the operator during this “Signature” test. System test of the interface unit with an ultracapacitor using the “Signature” test is representative of expected operation for load-leveling a traction battery in an electric or hybrid-electric propulsion drive; i.e., the ultracapacitor is charged during vehicle deceleration via regenerative braking and supplies a power boost during vehicle acceleration. Figure 15 shows ultracapacitor current and voltage waveforms for a “Signature” test using a 25 Farad ultracapacitor. In this example case, the ultracapacitor is charged at 10 kW constant power for a 15 second time interval, and after a 5 second interval is discharged at 10 kW constant power for 7 seconds. Figure 16 shows a test where the 25 Farad capacitor is charged at the interface rated maximum power of 25 kW, and then discharged at a 25 kW maximum power level. During both the charge and discharge portions of this test, the system operated between the software controlled minimum and maximum voltage levels.

5.1.4 Electronic Interface Efficiency Tests

Efficiency of the electronic interface unit was measured in the GE laboratory over a representative portion of the design operating voltage, current, and power range. Equipment used for the efficiency tests included a Xitron Technologies model 2503AH 3-channel Power Analysis System, a 4-channel LeCroy Oscilloscope, (model 9354 AM), and a Voltech PM3000A Universal Power Analyzer. No ultracapacitor was utilized in the circuit during efficiency testing of the electronic interface unit.

Figure 15. Ultracapacitor current and voltage waveforms for a 10 kW “Signature” test (25 Farad ultracapacitor, time = 5 sec/div, I = 50 A/div, V = 50 V/div.)

Figure 16. Ultracapacitor 25 kW charge/discharge waveforms
 (25 Farad ultracapacitor, time = 5 sec/div, I = 50 A/div, V = 50 V/div.)

The test methodology followed during the electronic interface efficiency tests operated the system at steady-state voltage, current, and power conditions. Figure 17a is a block diagram of the GE laboratory test set-up used for the electronic interface efficiency tests when the direction of power flow is from the high-side to the low-side, i.e., in the direction to “charge” an ultracapacitor in a vehicle application. Figure 17b is a block diagram of the laboratory test set-up used for the electronic interface efficiency tests when the direction of power flow is from the low-side to the high-side, i.e., in the direction to “discharge” an ultracapacitor in a vehicle application. Figure 18 shows a plot of the low-side voltage/current operating points for the efficiency measurements. The label on the chart identifies approximate high-side and low-side voltage levels and also the direction of power flow for the operating points where efficiency measurements were performed.

Figure 19 is a plot of the measured electronic interface efficiency (one-way) versus power level for power flow in the direction from the higher voltage source to the lower voltage sink, i.e., in the direction to charge the ultracapacitor or low-voltage battery from the traction battery or from the propulsion system during regenerative braking. Figure 20 is a plot of the measured electronic interface efficiency (one-way) versus power level for power flow in the direction from the lower voltage source to the higher voltage sink, i.e., in the direction to discharge the ultracapacitor or low-voltage battery while supplying power during vehicle acceleration.

Figure 17a. Block diagram of test setup used for electronic interface efficiency tests with the direction of power flow from high side to low side.

Figure 18. Ultracapacitor interface efficiency test points, low-side voltage (positive current = U.C. charge, negative current = U.C. discharge)

5.2 DOE Laboratory Test Support

GE-CRD provided engineering support to DOE Idaho during initial start-up and bench testing of the deliverable Ultracapacitor/Battery electronic interface unit. Functional tests were performed on the bench and verified correct operation of the hardware after shipment. A laboratory electric vehicle traction battery was utilized as the high-side voltage supply for these tests. The low-side of the interface unit was coupled to a 25 Farad ultracapacitor bank, similar to the unit used for laboratory tests at GE-CRD. After completion of functional testing, an external DOE data acquisition system was used to verify sensors and computed output parameters from the interface unit.

Figure 19. Ultracapacitor/battery interface efficiency versus charge power (power flows from higher voltage source to lower voltage sink)

Figure 20. Ultracapacitor/battery interface efficiency versus discharge power (power flows from lower voltage source to higher voltage sink)

6.0 Ultracapacitor/Battery Electronic Interface Cost Projections

Cost projections for the ultracapacitor/battery electronic interface unit are given in terms of a relative cost to the dc-ac inverter in a conventional ac drive train for an electric vehicle. As shown in Figure 1, with the exception of the inductor L1, the power circuit for the modular 25 kW interface is very similar to the power circuit for one phase of a 3-phase dc-ac inverter. A 50 kW ultracapacitor/battery electronic interface requires two modular 25 kW phase legs. Heat sink, microprocessor controller, wiring, and assembly costs for a 25 kW - 50 kW ultracapacitor/battery electronic interface are estimated to be the same as the corresponding component cost in a conventional 56 kW (75 hp) dc-ac inverter as used in an Ecostar sized vehicle. The low-loss high-frequency inductor cost for small quantity (prototype) production of a 50 kW electronic interface is estimated at \$1,000 - \$1,500, based primarily on material costs. Using the dc-ac inverter (motor controller electronics) production cost goal¹ (10,000+ quantity) of \$1,000 for a 56 kW unit as a reference, the estimate for a 50 kW ultracapacitor/battery electronic interface in 10,000+ quantity production is \$1,200 - \$1,500. Further cost and weight reduction is anticipated for advanced systems that combine the functions of the dc-ac traction drive inverter with the ultracapacitor/battery electronic interface unit.

7.0 Recommendations for Future Effort

Based on the success of this program that demonstrated a highly efficient 25 kW modular ultracapacitor/battery electronic interface and the potential to substantially increase battery life in heavy-duty hybrid vehicles, it is recommended that research and development be continued. Specifically, the following is GE's recommendation:

1. Increase the power level of the modular 25 kW ultracapacitor/battery electronic interface to 50 kW - 100 kW for applications in heavy-duty vehicles, including transit buses and trucks, for example, Class 6 (UPS/Federal Express size) urban pickup/delivery vans and heavy-duty refuse trucks.
2. Laboratory test this 50 kW - 100 kW electronic interface with prototype ultracapacitors rated for peak power levels of 50 kW - 100 kW and total energy storage of 500 Wh - 1,000 Wh.
3. Perform vehicle testing and associated weight and cost analysis of an advanced heavy-duty hybrid propulsion system using the prototype 50 kW - 100 kW ultracapacitor/battery system developed in (1) and (2) above.

8.0 Conclusions

A highly efficient ultracapacitor/battery electronic interface unit was developed and tested on this program. This interface unit is designed to be used as general-purpose test equipment for evaluating prototype ultracapacitors in the laboratory environment. The electronic interface unit design allows provision for a customer supplied external controller to be coupled to the delivered hardware to perform a battery or energy management function. Rigorous testing in the laboratories at GE-CRD and DOE Idaho National Engineering and Environmental Laboratory (INEEL) shows the electronic interface to be very reliable. The associated controls produce stable operation for energy storage loads including ultracapacitors, traction batteries, and resistors.

System study analysis performed on this program projects significant efficiency and fuel economy improvements for an advanced heavy-duty hybrid propulsion systems that utilizes the emerging ultracapacitor technology, in combination with the power electronic interface, as a power boosting device to load level the conventional traction battery and Auxiliary Power Unit (APU). System simulation results also show an improvement in projected battery life for a heavy-duty hybrid transit bus in excess of 100% to well over 200% (depending on the driving cycle), based on this analysis using an advanced ultracapacitor with assumed near-term electrical characteristics. A sub-scale ultracapacitor, based on the technology developed on the Ford Hybrid Vehicle Propulsion contract, was fabricated and laboratory bench tested using the electronic interface unit.

As shown in Section 5, detailed laboratory measurements were performed to experimentally measure the efficiency of the ultracapacitor/battery electronic interface unit over the majority of rated current/voltage plane for both the unit's low-voltage side terminals and the high-voltage side terminals. As shown from the efficiency test results, the design goal to achieve a highly efficient interface unit has been achieved. For bi-directional power flow, when operating the unit from 5 kW to 25 kW, the "one-way" system efficiency of the interface unit varies from 95.3% to 98.4%. Also, as shown from the test results, the interface unit's efficiency tends to increase with increased power levels and as the voltage difference between the low-voltage side and high-voltage side is minimized. For example, when power flows from the high-voltage side to the low-voltage side, with the high side at 300-V dc and the low side is at 265-V dc, the one-way efficiency of the unit varies from 98% to 98.4% for a range of power levels of 5 to 25 kW.

General Electric fulfilled the following Contract Deliverable Items: A Kickoff/Preliminary Design Review (PDR) was held at DOE Idaho Operations, Idaho Falls, Idaho in July 1996. A Critical Design Review was held with DOE at GE-CRD in Schenectady, NY November 15, 1996. On December 16, 1996, a Kickoff/Project Design Status meeting was held at GE-CRD with NYSERDA in Schenectady, NY.

In late August, 1997, the deliverable Ultracapacitor/Battery Electronic Interface was shipped to DOE Idaho Operations Idaho Falls, Idaho. GE-CRD provided on-site engineering test support at the DOE laboratory in Idaho Falls, Idaho in early September, 1997. Bench integration, start-up, and preliminary system test were completed within 2.5 days by GE-CRD and DOE employees at the DOE laboratory. Preliminary system tests, up to and including full-rated power of 25 kW, were run using a 25 Farad, 150-V laboratory Ultracapacitor, (similar to the laboratory ultracapacitor unit that was used for initial laboratory system integration at GE-CRD in Schenectady, NY). A conventional electric vehicle propulsion battery was used as the high-side source/sink for bench integration tests at DOE.

A Final Hardware Review/Laboratory Demonstration was held with NYSERDA at GE-CRD in Schenectady, NY on March 31, 1998. Operation of the second Ultracapacitor/Battery Electronic Interface unit was demonstrated at full-rated power of 25 kW using the 25-Farad, 150-V laboratory Ultracapacitor and a laboratory lead-acid battery in parallel with a dc power supply. After successfully demonstrating the ultracapacitor/battery interface unit with the 25 Farad ultracapacitor, the electrical parameters were adjusted, and several system test were run with the GE-CRD developed sub-scale ultracapacitor (2-Farad) stack.

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**Appendix A1:
Ultracapacitor/Battery Electronic Interface Functional Specification**

**Ultracapacitor Battery Interface
Functional Specification**

Rev 1

November 11, 1996

for

**Department of Energy
Idaho Operations Office
850 Energy Drive
Idaho Falls, Idaho 83401-1563**

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Ultracapacitor Battery Interface

Functional Specification

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1.0 General

A flexible, high efficient laboratory breadboard "proof-of-concept" Ultracapacitor/Battery Interface power electronic circuit with associated controls is being developed for this contract. This power electronic interface performs the function of translating the varying dc voltage on the ultracapacitor while extracting energy (discharge) or supplying energy (charge), and during the varying dc voltage of a battery as it is being discharged or charged. The interface matches the voltage level of the dc bus of an inverter supplied ac propulsion system in an electric vehicle application. The electronic control portion of the interface is designed to operate with a varying dc voltage ultracapacitor and a varying voltage dc bus. The control electronics capability is described in greater detail in Sections 4, 5, and 6. The control electronics is not configured to provide any of the functions associated with load leveling or power splitting between the propulsion battery and the ultracapacitor device through its interface. System design of the bi-directional interface is constrained such that the maximum dc voltage of the ultracapacitor or the battery is less than the minimum voltage on the dc bus, even during transient conditions of operation. This feature provides for a reduction in power electronic and control system complexity resulting in higher efficiency, smaller size, lighter weight and reduced costs. The maximum power capability of the ultracapacitor/battery interface power electronic breadboard is 25 kW. In addition to the maximum power rating, the power electronic breadboard will have both dc voltage and dc current ratings that also cannot be exceeded.

The energy stored in a fixed value of capacitor is proportional to the square of the capacitor voltage. The present design allows the ultracapacitor voltage to vary from full voltage to one-half of full voltage, allowing 75% of the total stored energy to be controlled. This reduction of capacitor voltage over a two-to-one range requires the capacitor current to also vary over a two-to-one range to achieve a constant maximum power charge and discharge capability. Beyond the two to one range, separate voltage and current limits are provided to protect the interface and the energy storage components.

During conditions of regenerative braking, the dc bus acts as the source and provide power to charge the ultracapacitor or low-voltage battery. The voltage on the dc bus varies over a less than two-to-one range from motoring to regenerating.

For the purpose of the specification, it is assumed that the voltage range of the ultracapacitor is from 150 volts to 300 volts. The dc current into the interface varies from 83.3 amps at 300 volts to 166.7 amps at 150 volts. The voltage range of the low voltage battery is also assumed to vary from 300 volts to 150 volts, resulting in the same current requirements for the interface circuit as in the ultracapacitor interface. The voltage from the dc bus is assumed to vary over a range of 300 volts to 400 volts. To maintain a maximum power capability of 25 kW will require a current rating of 83.3 amps at 300 volts and 62.5 amps at 400 volts.

The same power electronic components are used in all conditions. The controls must be capable of controlling the maximum voltage and the maximum current; i.e. 400 volts and 166.7 amps. If it is desired to test and evaluate an ultracapacitor or low-voltage battery with a dc voltage capability of, for example, 125 volts, then the maximum dc current would be limited by the interface to 166.7 amps, and the maximum power would be limited to 20.8 kW. Duty cycle limitations in the dc to dc circuitry will provide a lower (TBD) limit on the minimum value of ultracapacitor voltage.

The power electronic interface is shown schematically on Figure 1. It is composed of two controlled switches, Q1 and Q2, shown as IGBT's; two uncontrolled switches, D1 and D2, shown as diodes; one inductor, L1, and one conventional capacitor, C1. The connection of power semiconductors, Q1, Q2, D1, and D2 is called a "phase-leg," and these four components can be purchased as a single three-terminal assembly. It is important to note that the lower voltage dc component, that is, the ultracapacitor or the battery, be attached in parallel with the conventional capacitor C1. Since ohmic isolation is not required, the dc systems have a common negative terminal. The auxiliary circuitry to provide for snubbing is not shown on Figure 1 for clarity. Also not shown are the current and voltage sensors required by the control system or the switchgear (contactors and fuses) provided for protection. If the "lower" dc voltage of the ultracapacitor or low-voltage battery exceeds the "higher" dc voltage of the dc link, an uncontrolled current would flow through diode D1. Control logic and circuitry will be implemented to prevent component damage in the unlikely event that the "lower" voltage side of the interface exceeds the "higher" voltage side of the interface circuit.

A flow-through water cooled heat sink for the power semiconductors will allow the interface to be tested on both GE-CRD and INEL laboratory benches. The unit will be packaged to allow functional performance and efficiency tests to be performed in the respective laboratories. The deliverable interface hardware and control software is designed for laboratory testing only and is not designed to be incorporated into an electric or hybrid vehicle.

Although the electronic interface unit is being designed as a single 25 kW unit, it is a design goal to develop a modular interface system that can achieve higher power capabilities by operating multiple, 25 kW units in parallel with their associated controls. Section 4.5 of this specification has a more detailed discussion.

2.0 Input Power Requirements – Low Side DC Bus

Ultracapacitor/Battery Interface electronics is required to have a bi-directional current capability to allow both discharge and charge of the respective energy storage system. Maximum input power rating for this laboratory breadboard unit is 25 kW; i.e., 25 kW output from an ultracapacitor or from a low-voltage battery and also 25 kW output from the inverter when the energy storage unit is being charged during regenerative braking.

2.1 Ultracapacitor

The ultracapacitor is assumed to operate over a voltage range to utilize and extract 75% of its stored energy. Therefore, the terminal voltage of the ultracapacitor device and also the interface circuit varies over a 2:1 range. Preliminary interface requirements (consistent with the EGG-EP-11039 report requiring the ultracapacitor terminal voltage to always be less than the DC link of the inverter) are to operate the ultracapacitor device from a minimum of 150 V to a maximum of 300 V. The maximum current and voltage envelope is plotted in Figure 2. Since the dc voltage on the ultracapacitor, battery, and dc bus do not change sign, the direction of the dc current must reverse in order to provide a bi-directional power capability at the electronic interface. This is shown as an area of capability with a negative current. It is a design goal for the interface circuit to be capable of bench testing ultracapacitors with voltage ratings below 150 volts at reduced power levels, provided that the interface circuit maximum current limit is not exceeded, as shown by the dotted lines in Figure 2. In addition, there will be a (TBD) duty cycle limitation that will ultimately limit the absolute minimum voltage of the ultracapacitor during these tests outside the “normal” operating range.

2.2 Battery

The battery power is limited by the interface capability to a maximum value of 25 kW. The battery voltage is also constrained to operate within the same two-to-one voltage range (150 to 300 volts) as the ultracapacitor. Therefore the interface current requirements are the same and the operating area is as shown in Figure 2.

2.3 DC Bus

The regenerated power returned to the dc bus is also limited by the interface capability to a maximum value of 25 kW. The dc voltage at the interface ranges from a minimum of 300 volts during motoring to a maximum of 400 volts during regeneration. Maintaining a constant 25 kW requires the current to be 83.3 amps at 300 volts and 62.5 amps at 400 volts. The area of capability is shown on Figure 3. Notice that there is no overlap in the areas shown on Figures 2 and 3. This is because the voltage on the low voltage side of the interface must always be less than the voltage on the high voltage side of the interface as shown on Figure 1.

2.4 Under and Overvoltage Limiters and Protection

Undervoltage limiters will be integrated into the controls to maintain a minimum voltage on the low voltage side of the interface. During a discharge of the low side bus, voltage on the ultracapacitor or battery will

gradually collapse as stored energy is removed. As the voltage approaches the undervoltage limit, the control will begin to inhibit further discharges of the low voltage bus and maintain the minimum voltage. A control system boolean will be set whenever the low side voltage is less than 125% of the undervoltage limit. This will approximately equal 20% of the total energy remaining in the ultracapacitor under nominal operating conditions. The boolean may be viewed through the serial port monitor. No control shutdown will occur due to an undervoltage condition on the low side bus.

An overvoltage limiter will be provided in the interface system. The limiter will act within the control loop to maintain safe operating voltages on the low side dc bus by inhibiting further charging of the low side bus. Adjustable limit setpoints for the dc bus may be set by the operator at run time (up to a maximum of 300 V). A software boolean will be set which may be viewed with the serial port monitor whenever the low side voltage approaches 90% of the limiter setpoint.

Overvoltage protection is provided as a protective backup to the control limiters when a control action fails to maintain the voltage within the safe operating limits of the interface equipment. Whenever the voltage on the low side bus exceeds 105% of the overvoltage limiter setpoint, a protective shutdown and isolate fault sequence will occur (protection fault).

During power up and cpu reset conditions, factory default limits will be used as the overvoltage/undervoltage limit settings. The user may override these settings with other values of overvoltage limit settings that are less than factory default limits, or undervoltage limit settings that are less than factory default settings. Software will prevent the user from exceeding maximum or minimum settings and clamp the user supplied values to a bounded value (See Table I.)

Protection faults will be latched in software indefinitely until the user initiates a protection fault reset through the serial monitor. Protection faults, once detected and latched by the software, will simultaneously inhibit all IGBT gating and open the isolating contactors.

2.5 Input Power Source

The input power source is the source of power for the test, and it can be connected to either the low voltage or the high voltage side of the interface.

2.5.1 GE-CRD Laboratory Bench Test

Since an ultracapacitor or low voltage battery is not available at GE-CRD, it will be replaced with a 25 kW adjustable dc voltage (150 to 300 volts) laboratory power supply. A linear, series resistor can be added external to the power supply to simulate the internal resistance of the ultracapacitor. To simulate the dc bus as an input power source, a 25 kW adjustable dc voltage (300 to 400 volts) laboratory power supply is connected to the high voltage side of the interface.

The interface can be tested for performance and functionality and the efficiency can be measured at various values of input voltage and power.

2.5.2 INEL Laboratory Bench Test

The INEL ultracapacitor is expected to be used as the low voltage power source. As discussed in Section 2.1, and shown graphically in Figure 2, to achieve the full power rating of 25 kW, the ultracapacitor must operate over a voltage range from 150 to 300 volts dc (solid envelope). The high voltage power source, i.e., the high side dc bus, can be simulated with a dc load/source or a programmable charge/discharge tester which is within the 25 kW, 83.3 A and 300-400 V rating.

In general, the interface will functionally operate as a power converter, as long as the high side output power voltage and current specifications are met. Dynamics and transient responses for loads other than "stiff" DC loads/sources are outside the scope of this document.

An extended range of interface circuit operation is provided to allow test of ultracapacitors with a voltage range between TBD volts and 150 volts dc, as shown within the dotted lines of Figure 2. A design goal for this interface circuit is for the TBD (absolute minimum value of ultracapacitor voltage) in this extended range of operation to be 25 volts dc. As stated in Section 2.1., this depends on duty cycle limitations, and the actual minimum voltage of the ultracapacitor used in this interface will be assigned after GE-CRD's bench test is completed.

3.0 Output Power Requirements – High Side DC Bus

The output power requirements of the ultracapacitor/battery interface are equal to the input power of 25 kW minus the losses in the interface.

3.1 Under and Overvoltage Protection

When the high side bus exceeds 420 V (105% of 400 V) (non configurable), the software will declare a protection fault which inhibits IGBT switching and isolates as described in Section 2.4.

Undervoltage protection will isolate the interface from both dc busses by opening series contactors and placing the interface controller in a protection fault state whenever the differential voltage between the high and low side busses < 10 V. This setting is not user configurable.

The overvoltage protection is designed to protect the interface from damaging voltages. System/battery protection is to be provided by equipment external to the interface. Similarly, undervoltage protection is not critical for the operation of the interface as long as the voltage of the high side bus $>$ low side bus + 10.

3.2 Output Power Load Description

The output load, representing vehicle road load, dissipates the power for the test and is expected to be connected to the high voltage side of the interface. During bench testing of the interface circuit, a load may be connected to the low voltage side of the circuit.

3.2.1 GE-CRD Laboratory Bench Test

The load, composed of adjustable resistors, has a maximum power dissipation capability of 25 kW over a voltage and current range as shown on Figure 3 when the load is connected to the high voltage side of the interface. When the load is connected to the low voltage side of the interface, the range of voltage and current is shown on Figure 2.

3.2.2 INEL Laboratory Bench Test

When the load, composed of suitable resistors or an electronic load, is connected to the high voltage side of the interface, the control electronics regulates the power to the desired value, discharging the ultracapacitor. When the high voltage side of the interface is supplied from an adjustable dc voltage power supply or electronic source or charging circuit, then the ultracapacitor is the load and its voltage increases as its energy is increased. Both of these tests are transient and the data and measurements are taken during dynamic operation.

3.3 Energy Storage Limitations

Over and undervoltage protection provided for the ultracapacitor (Section 2.4) and the single level of voltage protection provided for the high voltage dc bus (Section 3.1) protect the interface and the ultracapacitor from excess energy or reduced energy caused by operation of the system beyond the limits of its capability.

4.0 Interface Electronics Functionality

This section describes via block diagrams several connections of the bi-directional battery/ultracapacitor interface working with a battery, ultracapacitor, and inverter dc link of an electrically propelled vehicle.

Figures 4 through 7 show block diagrams of several systems using batteries and/or ultracapacitors with electronic interfaces. The equipment supplied under this contract includes only one power electronic interface and the controls associated with an ultracapacitor. The second power electronic interface, the controls associated with a battery management system and the controls to provide system level functions are not provided. These figures are intended to show possible configurations. The CRD and INEL bench tests are described in Sections 2.5.1; 2.5.2; 3.2.1. and 3.2.2.

4.1 Ultracapacitor to Inverter DC Link Interface

This configuration is shown Figure 4. The combined ultracapacitor and inverter interface are connected in parallel with the battery powered inverter dc link of a vehicle drive in the laboratory. The battery-inverter dc link forms a conventional inverter-powered electric vehicle. Without the ultracapacitor, the battery must not only supply all of the energy to propel the vehicle but also provide the peak power required for acceleration and accept the peak power returned during vehicle braking.

The function of the ultracapacitor and its connected interface is to provide the high peak power required during acceleration and absorb the peak power returned during braking. The battery can now be optimized to provide its maximum energy capability.

The rating of the interface is a maximum of 25 kW when the ultracapacitor operates over a range of voltage from 150 to 300 volts. The dc bus voltage varies from 300 volt during motoring to 400 volts during regeneration.

The advantage of the Figure 4 connection is that an existing electric vehicle drive system could be bench tested in the laboratory both with and without the ultracapacitor and its associated interface. With the addition of the system-level controls including battery energy management and power sharing algorithms, the advantages of the ultracapacitor could be measured and quantified in a realistic vehicle drive system in the laboratory.

4.2 Ultracapacitor to Battery Interface

This configuration is shown in Figure 5. A conventional high-voltage (336 V nominal) battery is connected to a low voltage ultracapacitor through the bi-directional interface. This test set-up would be more appropriate for the laboratory test and evaluation of various ultracapacitor designs and/or the same design at several controlled charge and discharge duty cycles. Both the battery and the ultracapacitor are bi-directional and the energy stored in the battery could be transferred to the ultracapacitor and vice versa. Many cycles could be repeated until the system losses discharge the battery. The rating of the interface is

again 25 kW when the ultracapacitor, connected to the low voltage side of the interface, varies from 150 to 300 volts dc. The maximum power is limited to 25 kW by the rating of a single interface unit.

4.3 Battery to Inverter DC Link Interface

In this configuration, there is no ultracapacitor, only a low-voltage battery, the interface, and a high-voltage dc bus of an inverter-powered electric vehicle drive train. The block diagram is shown on Figure 6. The purpose of this configuration is to quantify the advantages of a low-voltage battery design. Advantages should accrue in reliability with less individual cells connected in series. There are other anticipated system advantages in designing batteries at a lower voltage level than is optimum for today's high power density inverters and ac type propulsion motors. The low voltage battery is connected to the low voltage input to the interface, and its design voltage range is between 150 and 300 volts. This set-up would be only a partial test of a compact electric vehicle as the propulsion power is limited to 25 kW by the rating of the single interface. Additional interface units could be paralleled to achieve higher power ratings (see Section 4.5). As mentioned previously, battery management controls are not provided under this contract.

4.4 Battery Interface in Parallel with an Ultracapacitor Interface

This configuration is shown on Figure 7. It requires two bi-directional interface circuits. In this configuration, an optimized low voltage battery design, in the range of 150 to 300 volts, is connected to the low voltage side of a 25 kW rated bi-directional interface, #1, and a 25 kW rated ultracapacitor rated at 150 to 300 volts dc is connected to the low voltage side of a bi-directional interface, #2. The two high-voltage (300 to 400 volts) sides of the interface are connected in parallel and supply the propulsion power to an inverter. The system as shown would be limited to a peak power of 50 kW by the rating of the two interface units. This system is considered to be the "ultimate" system as each component, battery, ultracapacitor and dc bus has its optimum voltage level and ratio for its intended application. Only one 25 kW interface is supplied by this contract, so implementation of this system is not possible.

4.5 Parallel Operation of Modular Electronic Interface Units

In several cases in the preceding sections, the power capability of the drive train was limited to a maximum of 25 kW by the rating of a single interface unit, per the work scope of the current contract. For conventional electric vehicles and certainly larger vehicles, for example, buses, the rating of 25 kW needs to be increased to provide the necessary propulsion power. The preferred approach for future higher power rated ultracapacitor interface development effort, rather than using ever more expensive higher current rated power switches and diodes, is to standardize on 25 kW as the basic interface rating. For these applications where higher power is required, additional 25 kW interface modules could be provided. Each modular interface module would contain a phase module consisting of two controlled switches (IGBT's with anti-parallel diodes) and an inductor, as shown in Figure 1. It is not necessary for each modular unit to be packaged in a separate enclosure; however, they may be singly packaged for modular power scaling and upgrading. Each enclosure could be comprised of multiple 25 kW modular power stages with interface to a single controller unit with slightly modified hardware and software, compared to

the original 25 kW unit that is being developed on this contract. This approach would allow the interface modules to be operated in a stagger-fired or sequential gating arrangement. Each interface would be provided with its own high voltage side, conventional dc capacitor and its own low-voltage side, series inductor. The high voltage side of an increased power modular unit is directly connected in parallel with the high voltage side of each respective modular unit. One approach for this increased power modular unit is to connect the multiple low voltage inputs (at each series inductor) in parallel and connect to a single ultracapacitor. A simplified circuit concept showing the power stages of three interface units is shown in Figure 8. With out-of-phase IGBT gating signals, the dc ripple current from the ultracapacitor will be reduced in magnitude, compared to the approach where the IGBT's are gated synchronously. Likewise, the ripple voltage on the conventional dc link filter capacitor will also be reduced in magnitude.

System efficiency improvements resulting from sequential gating of the IGBT's in a future modular high power unit are strongly dependent on the detailed electrical characteristics of the ultracapacitor as well as the characteristics of the electronics on the high voltage dc link.

4.6 Response Performance

Simulation results have shown that the response time from a -25 kW to a 25 kW power reference will be less than 0.1 s with less than 5% overshoot in power, voltage, and current. The simulation was done under nominal operating conditions; i.e., 150 - 300 V low side bus, 300 - 400 V high side bus, capacitance values from 10 - 100 F and typical cable lengths.

Additional simulations have shown that the interface will operate correctly in a steady-state mode down to 25 V on the low side bus but with a degradation in response times. This is due to the relatively high value of the inductor used. The design has optimized the inductance for nominal low-side voltages (150 - 300 V dc) and not the extended low-side design goal for operation with ultracapacitors less than 150 V dc minimum. The maximum change in inductor current is proportional to the applied voltage. When operating with low dc bus side voltages much less than nominal, the time it takes to decrease or increase the current in the inductor increases, and thus the longer it takes to change from one power level to another.

5.0 Interface Electronics External Input Controls

This section describes the four major signals that control the operation of the bi-directional interface.

5.1 Enable and Disable Signals (Start/Stop)

This logic signal commands the interface circuit to begin or cease operation. The required signals shall be a momentary contact closure. A separate start and stop signal will be employed. The interface starts up under closed loop control until the ultracapacitor voltage builds up to approximately 80% of the overvoltage limit setpoint to immediately allow for bi-directional power flow. Once the ultracapacitor voltage meets the 80% value, the control will respond to the analog power command. This is the normal means for starting and stopping the bi-directional interface. If both the start and stop signals are asserted simultaneously, the stop command will dominate. While the control is in the stop state, the system will isolate itself from both dc buses by opening internal high current contacts.

5.2 Bipolar Power Command Signal

The interface circuit operates in response to a bipolar analog signal that is proportional to dc input power command. A positive voltage signal (+ 10 volts) corresponds to 25 kW of power being extracted from the ultracapacitor or battery such as to discharge the ultracapacitor or low-voltage battery. A minus 10 volt signal corresponds to 25 kW of power being put into the ultracapacitor or low-voltage battery such as to charge the ultracapacitor or battery. This analog command signal ultimately controls the duty cycle of the switches in the interface circuit. Positive voltage corresponds to a step-up or boost operation; negative voltage corresponds to step-down or buck operation of the interface circuit. A zero voltage on the dc input power command represents zero power command; i.e., the ultracapacitor is not being charged or discharged. Suitable limits are provided to prevent excess voltage, current, power, and duty cycle levels.

5.3 Emergency Stop

This normally closed input signal bypasses the cpu software and in hardware directly removes contactor coil power and inhibits IGBT gating. This signal is meant to be used as a highly reliable form of fast shutdown and isolation during extreme system conditions and is not intended to be used as part of the normal start/stop control sequence.

5.4 Fault Annunciation

A single contact digital output to be monitored by the system controller signifying that the control is operating properly.

6.0 Protection

At present, six functions are configured for sensing and feedback to provide for the protection of the ultracapacitor, battery, or dc link. A protection fault disables and shuts down the interface as described in Section 2.4.

6.1 Overcurrent Protection

Hardware and software overcurrent protection is provided.

The IGBT modules are internally protected against instantaneous current overload and automatically disable themselves. In addition to the automatic disabling of the IGBT switch, a fault signal is communicated to the interface controller which sets a protection fault.

Current sensors are provided for both the input and output of the interface. When the measured and filtered (time averaged in software) current exceeds 220 A, the software will generate a protection fault.

6.2 Undervoltage Protection

Whenever the low side dc bus exceeds the voltage on the high side dc bus, uncontrolled current will flow through the interface. A protection fault will be declared whenever the voltage on the high side bus $>$ low voltage bus + 10.

6.3 Overvoltage Protection

Overvoltage protection can be scaled for operation of low voltage ultracapacitors in the dotted region of Figure 2.

6.4 Over Temperature Protection

For the INEL bench test, GE will specify to INEL a single electrically isolated temperature sensor that INEL shall mount on or within the ultracapacitor. Exceeding either user setpoint minimum or maximum temperatures will cause a protection fault. Overtemperature protection of the IGBT power modules is included in the GE interface design. Exceeding a minimum of 100°C in the IGBT power module will automatically disable the IGBT and the controller software will generate a protection fault. System reset after an occurrence of an IGBT overtemperature will not be allowed unless the IGBT temperature is less than 85°C.

6.5 Switchgear (DC Contactors)

A single pole, dc contactor is provided at the input and at the output of the interface. The opening command signal is based on overcurrent, overvoltage, watchdog time, external controller signals or an emergency shutdown. In normal operation both contactors will be closed, allowing the ultracapacitor and interface to be instantaneously ready to respond to the power command signal.

6.6 Emergency Shutdown

The emergency shutdown is initiated by the operator (local panel mounted mushroom button) and/or a user supplied isolated contact which will open the +12 V power to the contactor coils and disable the interface circuit IGBT gate drivers. Although only a single emergency shutdown (E -Stop) button is delivered with the hardware, additional remote E-Stop buttons or functions can be added for laboratory testing by connecting their respective contacts in series; i.e., a logical "AND" function.

7.0 Ultracapacitor Interface System I/O Block Diagram

Figure 9 shows a top-level functional block diagram of the ultracapacitor (UC) interface controller hardware. The lower right hand corner of each functional block shows the organization that has the design, fabrication, and testing responsibility for each subsystem. Arrows are shown on each functional interface to/from the GE-CRD hardware, including power, control signals, and temperature sensors, to indicate direction of control or functional flow; i.e., either Input or Output. A "Front Panel" function is also shown in this block diagram. This UC Electronic Interface controller design concept allows the system to be tested on a laboratory bench as either a stand-alone unit using standard laboratory equipment, or tested via a DOE-ID developed laboratory controller. For example, in the stand-alone mode, a function generator or digital voltage calibrator can supply the analog power command signal for charge or discharge tests of an ultracapacitor. Sufficient switches, push buttons, and indicators will be available on the front panel to perform normal startup, run and shutdown (either normal or emergency) sequencing with the ability to reset selected faults. The following section provides a preliminary description of the expected set-up, operation, and control of the UC interface system.

7.1 Ultracapacitor Interface System I/O Parameters, Adjustable Setpoints, and Limits

To increase the utility of the ultracapacitor interface unit to perform laboratory testing of ultracapacitors (or a low-voltage battery) with different ratings, a user friendly technique will allow certain parameters to be scaled or limited to less than their absolute maximum values. However, to protect the hardware, maximum limits for each adjustable parameter will be established by GE, and the operator will not be allowed to exceed these absolute maximum limits of current, voltage, power or temperature. Prior to each test, the operator will be able to set the desired parameters via a VT100 terminal, or equivalent, communicating over a RS232 link. Table I shows the list of adjustable parameters for the interface hardware developed under this contract.

Table I. Adjustable Parameters (setpoints) plus absolute limits

Adjustable Parameter (Setpoint) via VT100	Absolute Limits Software default
Set Ultracapacitor maximum Voltage during Test =	300 V dc max.
Set Ultracapacitor minimum Voltage during Test =	25 Vdc min/ 150 Vdc max 150V - default
Set Ultracapacitor maximum Current during Test =	167.7 A max
Set Ultracapacitor maximum Power during Test =	25 kW
Set Ultracapacitor minimum Temperature during Test =	-30°C min.
Set Ultracapacitor maximum Temperature during Test =	+85°max.

Note: Power and current limiters act on the measured absolute value of the above setpoints.

It is generally recommended to make changes to setpoints while the interface is in the stop state. However, changes may be made at any time.

The current value of the setpoints may be displayed on the VT100 terminal for verification by the operator at any time.

7.2 Input from Operator to GE UC Controller

The main control input required by the operator for the stand-alone mode of operation is the power command. A +10 V dc signal represents a maximum of 25 kW discharge of the UC, while a -10 V dc represents a maximum of 25 kW charge of the UC. However, as discussed in the previous section, if during the set-up procedure, the operator limited the maximum UC power to 5.0 kW, for example, then any value of power command in excess of ± 2.0 V dc will be interpreted by the UC controller as a ± 5 kW power command. A front panel with start and stop switches may be used for standalone operation. Operation of the GE UC Interface system with a DOE-ID laboratory controller will require wiring the start and stop contact inputs directly to the DOE-ID controller and disabling the front panel start and stop switches.

7.3 Input from UC Device to GE UC Controller

The only external sensor input from the UC device is the UC temperature sensor. The temperature probe will be selected by GE and is required to be electrically isolated from either terminal of the ultracapacitor. The expected temperature range for the temperature sensor is -30°C to $+85^{\circ}\text{C}$.

7.4 Output from GE UC Controller to DOE-ID Controller

An analog bipolar +10 V : -10 V power signal will be output which represents the measured power flowing through the UC interface. A digital contact (fault output) will also be provided. The fault contact will be closed whenever the control electronics are not powered or a protection fault has occurred and isolated the interface from the system. An operator initiated fault reset will be required to allow the interface to be placed back in service. The fault reset and a fault status will be controlled through the serial communication VT100 interface.

7.5 Summary of UC Controller I/O Signals

Table II shows the required list of signals and control parameters that will be available for control and monitoring uses.

Table II. Parameters, input monitored, or displayed during testing of the Interface Unit

Parameter	Format	Update rate (sec)
Analog Signals		
Monitor		
Capacitor Voltage	RS232	0.1
Capacitor Current	RS232	0.1
Capacitor Power	RS232	0.1
Output to DOE-ID Controller		
Capacitor Power	Analog,+/-10 V Isolated	0.1
Input to GE UC Interface		
Capacitor Power Command	Analog,+/-10 V Isolated	0.1
Digital Signals		
Monitor		
Low Voltage Limit within 25%	RS232	0.1
Over Voltage Limit within 90%	RS232	0.1
Fault Status - list of faults which are currently active in the interface, This fault list is queried by entering (typing) a fault query command.	RS232	
Output to DOE-ID Controller		
Interface Protection Fault	isolated contact closure	0.001
Input to GE-UC Controller		
Start (Momentary)	+12V	0.001
Stop (Momentary)	+12V	0.001
Emergency Stop (latched)	+12V	N/A
		Rev. 1 11/7/96

7.6 I/O Functional Description

The UC Interface will be supplied with the following types and quantities of I/O

- **Digital Inputs** – Six isolated optically coupled digital inputs rated for nominal +120 V@ 12 mA. Presently 2 of the inputs are used (Start, Stop). The remaining four outputs are spare.
- **Digital Outputs** – 2 Form C relay contact outputs rated 2 A @30 Vdc. One normally closed contact will be for the Interface Fault Annunciation and the other a spare.
- In addition to the 2 relay outputs, 4 optically isolated photo transistor outputs rated 300 mA @24 Vdc are provided. Two of these outputs are for internal relay (contactor) control, with the other two as spares.
- **Analog Inputs** – 2 isolated analog inputs rated +/-10 V, with 10K input resistance. One analog input will be designated as the power input, and the other a spare.
- **Analog Outputs** - 4 +/-10 V isolated analog outputs capable of driving loads up to 2K ohms. One analog output is designated as the capacitor power. Two outputs are reserved for diagnostics, with one spare.
- **Analog Isolation** – Both the analog outputs and inputs are powered by a common internal isolated power supply. The maximum common mode isolation voltage between the interface controller and the analog I/O is 500 V. All the analog inputs/outputs previously described share a common reference. It is important to note that the analog I/O is not intended to be connected to multiple devices which also do not share a common reference.
- **Emergency Stop** – This is a dedicated digital input which when opened immediately removes contactor power to the isolating contactors (see section 6.6) and inhibits IGBT gating. An optional isolated digital contact (normally closed) rated at 15 A @12 Vdc may be connected to the interface for remote emergency stops.

7.7 Input Control Power

The interface electronics requires a user supplied +12 Vdc @4 A continuous power input. During periods when dc isolating contactors are closed, a 100 ms 15 A surge will be drawn.

8.0 Environment

The interface circuit and associated control is fabricated only for laboratory test and evaluation.

8.1. Ambient Temperature Range

The ambient temperature range in the laboratory is assumed to be 10°C to 30°C.

8.2 Heat Sink Coolant Temperature Range

The maximum inlet water temperature is 30°C. The water will pass through the interface heat sink and freely discharge to a drain. Since water is the coolant, operation or storage below freezing conditions is not permitted. Greater reliability can be obtained when the inlet water temperature is below 30°C. Empirical data on the maximum temperature rise, recommended flow rate, and pressure drop will be available, and this data will be provided to DOE-ID during the CRD hardware test phase.

9.0 Packaging Requirements

Since the interface is to be operated in an indoor laboratory, there are no minimum packaging requirements. It is anticipated the unit may be packaged in a 19 or 25 inch relay rack/cabinet enclosure. The use of all or a part of the existing GE EV2000 inverter package will also be evaluated. Various connectors, for monitor, sensed parameters and power command will be provided on the front panel. In addition to the dc input and output a mutually agreed upon low voltage dc power supply (12 V) will be required for the control and logic power supplies, and contactor coil power. This control power will be isolated from the interface input and output voltage. The negative side of the control power supply will be referenced to the interface chassis ground.

10.0 Program Support

This section will be provided after the controls have been designed.

10.1 Power/Signal Description at Interface Connectors

To be determined.

10.2 Laboratory Test Safety Precautions/Warnings

To be determined.

Figure 1. Power circuit schematic.

Figure 2. Ultracapacitor or low-voltage battery operating limits.

Figure 4. Ultracapacitor to DC link interface block diagram.

Figure 5. Battery to ultracapacitor block diagram.

Figure 8. Three sequentially gated interface units (simplified power circuits).

Appendix A2: Ultracapacitor/Battery Electronic Interface Topology Selection

Preliminary design of the Ultracapacitor/Battery Electronic Interface focused on the circuit topology to be used for the deliverable hardware to meet the program objectives. Power semiconductor device technology, available during the original ultracapacitor system study¹, ("Ultracapacitor/Battery Interface Electronics for Electric Vehicle Drivelines," conducted by GE in 1992 and 1993 and documented in EG&G Final report EGG-EP-11039), recommended soft switch topology based on projected system efficiency and cost analysis performed in the paper study. Two events have occurred since the 1992-93 system study: (1) today's commercial IGBT power semiconductor device technology improvements allow reduced switching losses in hard switched circuits as compared to the devices available during the study, and (2) GE has conducted over \$2M in research contracts that developed and implemented "soft switched" converters using the GE patented Auxiliary Resonant Commutated Pole (ARCP) technique for applications with 3-phase ac output power. During recent hardware testing on these related soft switched technology contracts, GE engineers observed a drift in the midpoint of the split capacitors connected to the auxiliary circuit when these circuits are used in DC/DC applications. Although this mid-point drift is not perceived to be a problem for AC output power applications, additional circuitry (high frequency DC/DC converter) is required to correct this mid-point drift issue for applications with DC output. DC/DC converter applications, using soft switched topology, will have higher component cost and lower system efficiency than originally envisioned in the 1992-93 ultracapacitor/battery interface study.

GE requested a contract modification to use a hard-switch topology instead of a soft-switch topology. DOE granted a contract modification for hard-switched topology implementation of the deliverable unit.

Appendix B1: Ultracapacitor/Battery Electronic Interface User's Manual

Ultracapacitor Interface User's Manual

Revision 2

September 9, 1997

for

**Department of Energy
Idaho Operations Office
850 Energy Drive
Idaho Falls, Idaho 83401-1563**

Under Cooperative Agreement DE-FC07-96ID13406

Prepared By

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**General Electric Company
Corporate Research and Development
1 Research Circle
Schenectady, NY 12309**

Introduction

This manual describes the use and operation of the Ultracapacitor Interface (UCI) developed by GE. The term UCI shall be used to describe the Ultracapacitor/Battery Interface power electronics circuit and its associated controls and external interfaces. Detailed specifications for this equipment are found in the Ultracapacitor/Battery Interface Functional Specification.

Hardware and Front Panel

The UCI consists of a single unit containing the power electronics (contactors, IGBTs, etc.) and the digital controls. The inductor is mounted to the bottom of the heat sink. Several external interfaces are provided on the front panel for operation of the UCI circuit (see Figure 1). The "low" side DC power connection is located on the far right hand side of the panel (4-pin connector; 2 of 4 pins of connector utilized). The "high" side DC power connection is to the left of the low side connection and uses a slightly smaller 2-pin connector. Other controls on the front panel are the START, STOP, and E-STOP push buttons and a power ON/OFF switch. On the far left is a 9-pin RS-422 connector. A connection to a PC serial port or terminal is made with the use of an RS-422 to RS-232 adapter box. There are also connections for the 12 volt DC power and the analog input power command signal. Finally, there are LED indicators for the input power status, contactor closed condition, and fault status.

Figure 1 Ultracapacitor Interface Front Panel

Power Control Input

The power control input is a ± 10 V input that determines the power command to the UCI. $+10$ V corresponds to a 25 kW discharge of the capacitor or battery from the low side, while -10 V is a 25 kW charge of the capacitor/battery. The polarity of the low side current will be consistent with the polarity of the power. If the maximum power is set to a value less than 25 kW (e.g., 15 kW), then voltages larger than a certain value (e.g., ± 6 V) will be clamped to the maximum power setting.

System Operation

This section discusses the basic operation of the UCI system. Additional details are presented in the section on RS-232 control as they relate to specific commands.

When 12 volts is applied to the control power input and the front panel power switch is turned on, the serial port will print the following message: "Press <ESC> to abort application load in X sec." The operator should let the seconds count down to 0. The boot software then loads the ultracapacitor application software, and a prompt entitled "UCI>" appears. If the prompt does not appear after a couple of seconds, the operator should press <ENTER> to get the prompt. Specific commands that may now be executed are discussed in the RS-232 Control section. Occasionally the unit does not boot successfully after it has been running (i.e. warm start). If this occurs, wait a few minutes after shutting off the 12 volt power before turning power back on.

If the operator presses <ESC> during the seconds countdown, a prompt will appear at the terminal that says "BOOT>". The boot program can be used to download new software that GE may provide in the future. The command to download an executable is "DX". After entering this command, the operator should go to the Terminal Menu entitled Transfers, select Send Binary File..., enter the filename of the executable, and press OK. After the new executable is downloaded, the new software is downloaded by cycling the 12 volt power to the unit.

After booting, the system parameters and limits are all at their default value. The default mode for the UCI is Capacitor. The mode can be one of 3 possible values: (1) Resistor, (2) Capacitor (default), and (3) Battery. The Resistor mode can be used to test the UCI with a purely resistive load, and should not normally be used. The Capacitor mode assumes a Capacitor is connected to the low side of the interface. In this mode, pushing START causes the UCI to attempt to charge the capacitor up to 80% of the maximum voltage setpoint before entering the "RUN" state, at which point the UCI responds to the input power command. In this "CHARGE" state, the controller will provide a constant current of 50 A into the low side. The Battery mode assumes a Battery is connected to the low side of the interface. When START is pushed, the controller checks the voltage on the low side. If the voltage is above the minimum setpoint, the UCI enters the "RUN" state and responds to the input power command. Otherwise, a low side undervoltage fault occurs on the assumption that the battery is "dead."

Once the system is in the RUN state, the controller behaves similarly for any of the 3 modes. The system responds to the input power command by varying the switch duty cycle to provide the requested power. The operator should be aware of several limits in the controller that can affect the system. These limits are adjustable setpoints that can be displayed and modified as described in the RS-232 Control section below. The first limit is the power command limit discussed in the Power Control Input section. Any power command input beyond the limit will be clamped to the limit.

The next set of limits are upper and lower limits on the low side voltage in the system. During system operation, the power command will be scaled back if the actual voltage comes within 10 V of the setpoint limit. Between 10 and 0 volts from the limit, the actual requested power is $(\text{limit} - \text{low side voltage})/10 * \text{power command}$. For example, if the external power command is -20 kW and the low side voltage is now 2 V away from the upper setpoint, the actual requested power is only -4 kW. This feature allows the voltage to gradually approach the max and min setpoints. Regardless of the upper limit setpoint, there is also a similar scaleback of the power command as the low side voltage approaches the high side voltage. Once the low side is within 10 V of the high side, a fault condition

occurs. To avoid this condition, the power command scaleback occurs over a similar 10 volt range when the low side is between 25 and 15 volts of the high side voltage.

The final limit is a current limit. The control software contains an inner current loop and an outer power loop. If the requested power command results in a current command that would exceed the specified current limit, the actual current command is clamped to the limit. Of course, this in turns limits the actual power that is delivered.

The normal way to disable the UCI is to press the STOP button on the front panel. This opens up the main contactors and puts the system in the DISABLED state. Pressing START then initiates sequencing to return the unit to the RUN state. In an emergency situation or at the end of the day, the operator may press E-STOP. This creates a fault condition that disables further operation until E-STOP is released and faults are cleared. This also discharges some capacitors internal to the UCI. After pressing E-STOP, the operator should wait at least 1 minute before releasing the E-STOP.

RS-232 Control Interface

The 9-pin connection on the front panel supports an RS-232 interface to allow communication between a terminal or PC and the UCI control processor. Parameters of the link are 19,200 bps, 8-bit, 1 stop bit, and no parity. After the power up sequence discussed above, the operator may now enter commands via the keyboard to set or query system parameters. The following paragraphs discuss the commands available to the operator. All commands can be upper or lower case, and must be followed by <ENTER> to execute.

US – This command displays the current value of all system setpoints. There are six system setpoints, as described in Table I of the UC Functional Spec. The setpoints are: (1) Maximum voltage, (2) Minimum voltage, (3) Maximum current, (4) Maximum power, (5) Minimum temperature, and (6) Maximum temperature. Setpoints 1-4 all operate on the low side of the UCI.

Ux, where x=1-6 – These six commands allow the operator to change the value of the corresponding setpoint, within the range of allowed values for the system. For example, "U3" is entered to modify the maximum current.

UF – This command displays the current faults in the UCI. If the fault status LED on the front panel is red, this command displays the current fault condition(s). Faults remain set until they are specifically reset by the operator.

UR – This command attempts to reset any UCI faults. It then displays a list of the current faults in order to indicate any faults which could not be reset.

UM – This command allows the operator to set the UCI system mode. The mode that is selected determines how the controller operates when the START pushbutton is pushed. The mode can be one of three possible values: (1) Resistor, (2) Capacitor (default), and (3) Battery. See the System Operation section for a discussion of the three system modes.

TP – This command displays the current value of several system parameters, including high and low side voltage and current, calculated power, requested power, high and low voltage warning signals, and temperature feedbacks. The values are presented in a tabular form and will continuously update until the operator presses the <ESC> key.

The above commands are sufficient to satisfy the requirements in the UCI Functional Spec. There are also two other commands that were added to support testing.

UC – This command is a calibration function that provides offset nulling for the voltage input and power command input. Before executing this command, the operator must ensure that the high and low side voltage feedbacks are 0, and the voltage at the power command input is 0 V. Executing this command runs a 5 second test that calculates the average input over 5 seconds and applies this offset against all future readings as a correction.

Note: For circuit boards tested to date, the magnitude of these offsets is very small compared to the full-scale value of these inputs (tenths of a percent). However, there may be tests run at low voltage or power where it is desirable to reduce this small error with this calibration test.

UT – This command invokes the ultracapacitor “Signature” test. This test is a discharge-charge-discharge cycle of the capacitor connected to the low side. The operator is prompted to enter the power level for the test in watts, a charge time in seconds, and a discharge time in seconds. Upon confirmation of the entered parameters, the software will automatically run a test that discharges the capacitor at 15 kW for 45 seconds, and then charges and discharges the capacitor according to the specified parameters.

The operator must be aware of the power, voltage, and current limiting discussed earlier when running this test. While this test is executing, the system does not respond to the external power command input. Upon completion of the test, the system again responds to the external power command. As the test proceeds, the system software calculates and displays the low side voltage at three points: (1) after the initial discharge, (2) after the charge cycle, and (3) after the discharge cycle.

Appendix B2: Ultracapacitor/Battery Electronic Interface Parts List and Schematic Diagrams

Contract # DE-FC07-96ID13406, GE-Corporate Research and Development

R.D. King, Project Manager, 9/23/97

Reference Designation	Part #	Qty.	Manufacturer	Notes
IPM1,2	PM600DSA060	2	Powerex	Intelligent Pwr Module
K2,K3	EV250-2A	2	Kilovac	DC Contactor
LEM1,2	LA305-S	2	Lem	Current Sensor
R1	RH-25 15K Ohm 25 W	1	Dale	Newark #13F140 15K
R2	RH-50 3K Ohm 50 W	1	Dale	Newark #13F141 3K
MOV	V321DB40	1	Harris	Transient Voltage Suppressor
C2	GE 2.2uF 600V	3	GE	Newark # 46F1232
C1	GE 1000uF 450V	1	GE	Newark # 93F8736
PS1	VI-RJ0022-CYYY	1	Vicor	DC-DC Converter
CB/SW	JA1S-D3-A-0010-02E	1	Heinemann	10 Amp DC
K6,K7	PD5BA57	2	Kilovac	NC 12V Panel
K4,K5	PD5AA57	2	Kilovac	NO 12V Panel
R3,R4	39 Ohm	2		Drive Systems EV2000
C3	GE 3300 μ F	2		Capacitor
L1	200 μ H	1	GE CRD	Inductor
E-Stop	NC 16mm Mushroom	1	Square D	Newark # 50F4614
Start	SPDT/Mom Flush	1		Newark # 50F1476
Stop	SPDT/Mom Raised	1		Newark # 50F1477
J1	GTC06R-36-5P	1	Bendix	Connector
J2	GTC06R-32-5P	1	Bendix	Connector
BICC Assm.	SK-96-200995-01	1	GE-CRD	PC Brd Assembly
DSPx Assm.	SK-96-200203-02	1	GE-CRD	PC Brd Assembly, Mounted to BICC Assm.

CONTRACT NO.		GENERAL ELECTRIC CR&D	
APPROVALS		DRAWING TITLE	
DESIGNED	DATE	Ultra Cap Converter	
CHECKED	DATE	SIZE	REV
ISSUED	DATE	FSCM NO	DMG. NO.
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE:		SCALE	DESIGNER
		Mark Cardinal	SHEET 1

CONTRACT NO.		GENERAL ELECTRIC CR&D			
APPROVALS	DATE	DRAWING TITLE			
DRAWN G. Kilinski	DATE 11/11/71	UCap Conv User Terminal Board			
CHECKED		SIZE	FSCH NO	DWG. NO.	REV. B
ISSUED		SCALE	DESIGNER Gary Kilinski	SHEET 1	

UNLESS OTHERWISE SPECIFIED TOLERANCES ARE

Appendix B3: SAFT STH-STX Series Product Brochure

Ni-Cd

**High-power
nickel-cadmium
batteries for hybrid
electric vehicles**

STH-STX series

These series of advanced Ni-Cd batteries provides an ideal balance of mass, power and energy for vehicles combining in tandem a conventional combustion engine and electric motor to reduce the consumption of gasoline and minimize air pollution. They are also used as power backup batteries for trolley buses or light rail trains (LRT) when running without catenaries or skirting obstacles.

Application

Buses, trolley buses, trucks, light rail trains (LRT), automated guided vehicles (AGV), etc.

Advantages

- Low maintenance
- Reliability
- Permanent availability of power
- Low km/passenger cost ratio
- Adapted to extreme temperatures -20°C to +55°C
- Centralized water filling system
- Rapid recharge
- Fully recyclable

Technology

- Sintered positive electrode
- Plastic-bonded negative electrode

Electrical characteristics

Range from 16 to 190 Ah

Example :

	STH 800	STX 600*
Nominal voltage [V]	1.2	1.2
Rated capacity [Ah]	80	56

Mechanical characteristics

Typical weight [kg]	3.3	2
Dimensions [mm]	85x85x306	64x86x220
Volume [dm ³]	2.21	1.21
Cycle life at 5% DOD	150,000 cycles	

*Under development

SAFT

Typical discharge at +20°C

Available capacity versus end voltage and discharge duration

Cycle life at +20°C

SAFT

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