SAND97-2641C
SAND--97-2641C

MEMS: A NEW APPROACH TO MICRO-OPTICS

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CONF-971192--

ABSTRACT

Micro ElectroMechanical Systems (MEMS) and their fabrication technologies provide great opportunities for application to micro-optical systems (MOEMS). Implementing MOEMS technology ranges from simple, passive components to complicated, active systems. Here, an overview of polysilicon surface micromachining MEMS combined with optics is presented. Recent advancements to the technology, which may enhance its appeal for micro-optics applications are emphasized.

Of all the MEMS fabrication technologies, polysilicon surface micromachining technology has the greatest basis in and leverages the most the infrastructure for silicon integrated circuit fabrication. In that respect, it provides the potential for very large volume, inexpensive production of MOEMS. This paper highlights polysilicon surface micromachining technology in regards to its capability to provide both passive and active mechanical elements with quality optical elements.

INTRODUCTION

Since their inception, MEMS have been envisioned to impact numerous areas of our lives, including consumer products, communications, automotive, and medical applications. Some of these have successfully come to commercial fruition. To name just two examples, bulk micromachined pressure sensors[1] have progressed into automobiles and medicine as intake manifold and blood pressure sensors while surface micromachined accelerometers[2] have progressed as airbag deployment sensors. In the area of micro-optics, several years ago this author reviewed the status of microactuation as applied to micro-optical systems [3]. In that paper, several examples of micro-optics with MEMS produced by various fabrication technologies were presented. Since that time, several advancements have occurred with all types of MEMS fabrication technologies. For example, the well-established science of selectively etching to specific crystal planes in silicon, bulk silicon micromachining, continues to be refined. The very accurately defined and high quality (111) crystal planes typically exposed by bulk micromachining of silicon continue to be utilized for the accurate placement of optical components such as fiber optics and the production of quality mirror surfaces [4,5]. In some cases, bulk micromachining is being utilized as the base platform to create more complicated optical systems such as a Silicon-Micro-Optical-Bench[6].

The remainder of this paper contains a process section which provides an overview of polysilicon surface-micromachining and stresses the current enhancements to that technology. In the past couple of years, considerable progress has occurred in terms of fabrication complexity available to designers and significant improvements to manufacturing. The last section provides overview examples of polysilicon surface-micromachining technology applied to optical applications, again with emphasis on the benefits of the latest enhancements to the basic technology. From the perspective of a person specializing in optics these applications may appear relatively crude, however, they clearly illustrate the promising utility of the MEMS technology as applied to optics.

POLYSILICON SURFACE MICROMACHINING

Two key process developments in polysilicon surface micromachining have rapidly propelled the technology forward, leading to renewed excitement in its application. The first is related to the understanding of the device surfaces. It is well known that as the surface-to-volume ratio increases, surface phenomena begin to become significant or even dominate the behavior of the device. Within MEMS, polysilicon surface-micromachined structures fall into this latter category[7]. The tendency for the surfaces attract to each other leading to adhesion of the structures to themselves or the substrate is known as stiction and is a common term to a micromachinist[8]. This latter topic has considerable literature devoted to it including special issues [9] and workshops [10]. The second development is the introduction of topography planarization by chemical mechanical polishing. This has significant impact on the manufacturability devices and allows ready extension of the number of independently definable layers available to the designer. This topic will be discussed in more detail below. The point being that rapid progress is occurring, and many issues of repeatability and reliability are successfully being addressed allowing the consideration of significantly more complex devices and the commercialization of others.

DISCLAIMER

The Basic Technology

To clarify nomenclature, we count the initial electrical interconnect layer plus the N mechanically active polysilicon layers and designate the process as a (N+1) level polysilicon surface-micromachining technology. This is consistent with nomenclature used for other externally available polysilicon surface-micromachining processes [11]. At Sandia, we have a baseline 4-level process which has recently been extended to a 5-level process [12], significantly enhancing our ability to create complex micro-structures (see Figure 1). Examples of batch-fabricated devices defined in the 4-level process can be found elsewhere [13]. The basic 4-level process is referred to as the Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT)[13].

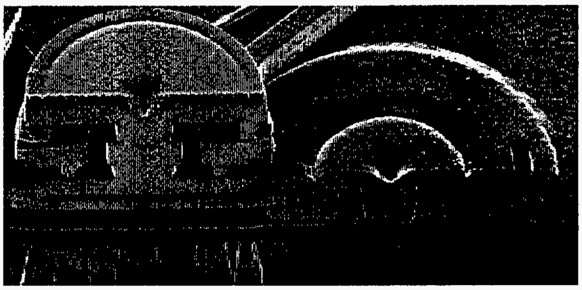


Figure 1. This SEM cross-section was formed by focused ion beam (FIB) milling through a 5-level device area. The polysilicon layers are the light films, while the dark spaces are where the sacrificial oxide films existed prior to the release etch. Nominal thickness of mechanical polysilicon layers and sacrificial oxide layers range 1-2.5 microns.

An (N+1)-level polysilicon surface-micromachining technology has, as its basic process module, the repetitive cycle of deposition and definition of two primary films, a sacrificial silicon dioxide film and a structural polycrystalline silicon film. Details of rudimentary polysilicon surface micromachining process are described by Howe[14], while details of the Sandia 4-level polysilicon surface micromachining technology are described by Garcia and Sniegowski[15]. The deposition, photolithography, and etch processes are based on those used in standard IC fabrication, but modified for thicker, mechanically-optimized films. Thus low-pressure chemical vapor deposition (LPCVD) of polysilicon and silicon dioxide films, and reactive ion etch for film definition are used. A 5-level process in essence repeats this base sequence 5 times. Key advantages to polysilicon surface-micromachining are that the process is a batch-fabrication technology which does not require piece-part assembly, and that it utilizes the IC infrastructure which is capable of large-scale production. Completion of the fabrication cycle entails a final release step which removes all sacrificial films to provide hundreds to thousands of ready-to-operate devices.

Chemical Mechanical Polishing (CMP)

The recent addition of chemical-mechanical polishing (CMP) planarization to polysilicon surface-micromachining technology is a major process enhancement from both the process and design perspectives [16]. Known primarily for its global planarization use in sub-micron circuit technology[17], CMP interestingly was first used in the MEMS field to improve the optical quality of polysilicon surface-micromachined mirror devices by smoothing the polysilicon film surface[18].

However, the benefits of CMP for surface-micromachining are four-fold. First, from the optical perspective, it can be used to polish surfaces. Second, mechanically, it eliminates potential film-to-film interference. Third, it eliminates several manufacturing issues related to photolithography and film definition which allows the practical extension to additional levels of polysilicon. Fourth, CMP enables an innovative approach to the monolithic integration of electronics and surface micromachining [19], which eventually may impact MOEMS as it has MEMS sensors[2].

Multi-Layer Technology

Although extension to additional design layers has considerable development and production costs associated with it, the benefits to a 5-level process have significantly outweighed these costs. The primary benefits can be summarized as affecting the surface-to-volume ratio (i.e., stiffer structures), increasing device robustness and reliability, and allowing much greater design freedom.

The use of thin films (1-4 µm) has often been cited as a major limitation to polysilicon surface-micromachining. Stacking polysilicon levels provides this desirable increase in film thickness. The image in Figure 2 illustrates the use of film stacking to create a central truss on an electrostatic comb-drive which is orders-of-magnitude stiffer than if it were comprised of a single level. This additional stiffness directly impacts reliability in the sense that the additional stiffness is useful in overcoming the adverse effects of surface forces (stiction).

Robustness and reliability are also affected through the inclusion of additional mechanical constraints for protection during operation and handling, e.g., shock environments.

The gain in design freedom is left to be illustrated through the examples provided in the last section.

In addition to the above points, the 5th layer continues to display an extremely low film-stress gradient, which prevents film curl in released structures. One of our polysilicon film processes exhibits a film curl having ≤150 nanometer out-of-plane deflection at the tip of a singly-clamped cantilever beam 1000 microns long. This measurement is obtained with an interferometric technique[20]. Film distortion at this extremely low level is very acceptable in optical mirror applications. Further, net in-plane stress is at the limit of our current stress diagnostic structures which detect film stress at the tens of megaPascal level [21]. This implies that structures having extremely large in-plane dimensions, such as the gears in Figure 3, continue to be viable in the 5th level of polysilicon. This is critical to many micromechanical sensor and actuator elements.

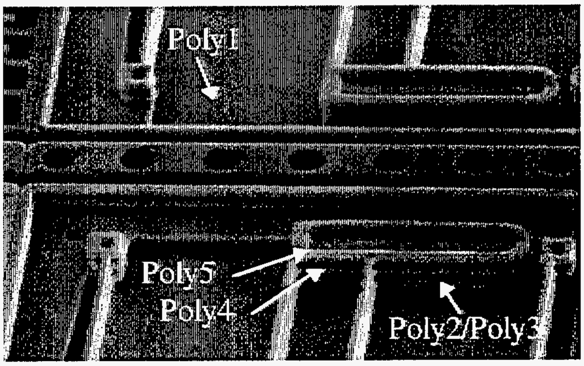


Figure 2. The image is a close-up view of the elastic elements supporting the comb drives. The poly layers are numbered from 1, the ground poly, to Poly5, the uppermost, for a total of 5-levels. One sees that the effective thickness of these elements is greatly enhanced with the additional layer. The total device height above the substrate is 12.5 μm.

SURFACE-MICROMACHINED OPTICS

The following examples, which are only a small sample of the literature, were chosen to illustrate the state-of-the-art and potential utility of polysilicon surface-micromachining technology. They illustrate several key points of the technology. These points include the possibility of large arrays, the absence of required assembly, and the inclusion of other mechanical operations as part of the system-on-a-chip. The first example consists of a large array of individually addressable mirrors, while a second is a micro version of a common optical tool, the optical bench. A third illustrates a combination of a mechanical element, a lock, and an optical element.

Micromirror Devices

A little over 2 decades ago, Texas Instruments began work on a micromirror device which eventually matured into their Digital Mirror Device (DMD) [22]. Because of this and other successes, micromirror devices are possibly the most widely recognized micromechanical optical device. In the case of polysilicon surface-micromachining, the combination of CMP and additional polysilicon layers has eliminated a number of engineering compromises which designers have been facing. Namely, CMP has eliminated the undesirable topography due to underlying layers which can lead to less than desirable optical mirror surfaces.

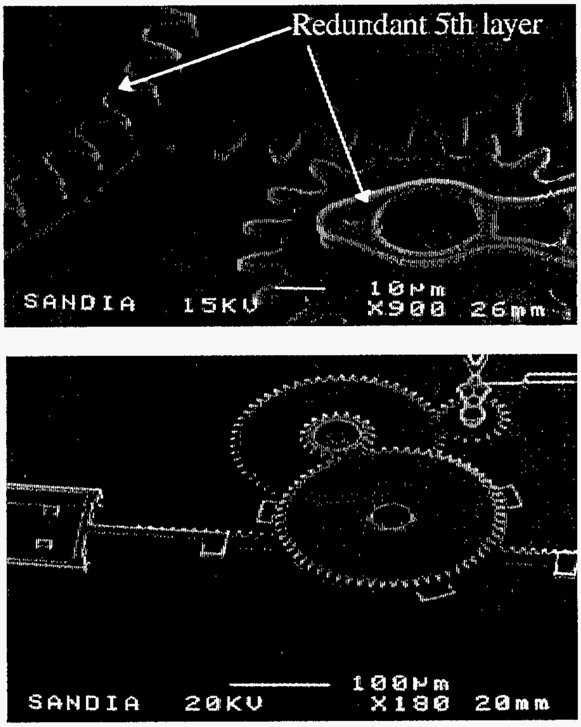


Figure 3. Two SEM images of parts of a geared microactuation mechanism. The top image is a close-up of the torque conversion unit which shows multi-level gears and specifically the redundant top gear layer which demonstrates the 5-level process. The lower is a linear geared-rack and part of a fold-up mirror.

Further, the additional layers, specifically the SUMMiT process, has allowed greater than 98% use of available surface area as mirror surface (optical fill-factor). The work of Michalicek, Comtois, and Barron with micromirror designs in the SUMMiT process [23] illustrates these advantages as seen in Figure 4. The multi-layer technology allows address lines, support posts, and support flexures to exist directly beneath the active mirror element leading to the high fill-factor. CMP planarization effectively removes all traces of the earlier film topography to produce unblemished mirror surfaces.

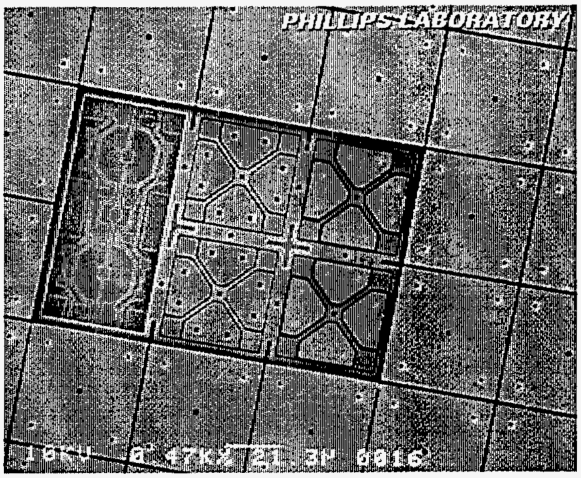


Figure 4. SEM image of an Axial-Rotation Micromirror Device where six mirror elements are shown with the upper layers removed to illustrate the design by process layers. Surrounding the six uncovered elements is the normal field of individually addressable micromirror devices which illustrates the current fill-factor (>98%). (Courtesy of USAF Phillips Laboratory)

Current designs now operate at reasonably low voltages (<15V), however, the next generation of micromirror devices from these researchers will be based on flexureless elements which uses a pin-joint for its fulcrum [24], potentially permitting operation under very low applied voltages (<5V). This further exploits and requires the use of at least a 4-layer process. One focus of their future work is directed towards a micromirror array for the correction of image phase aberration due to atmospheric turbulence.

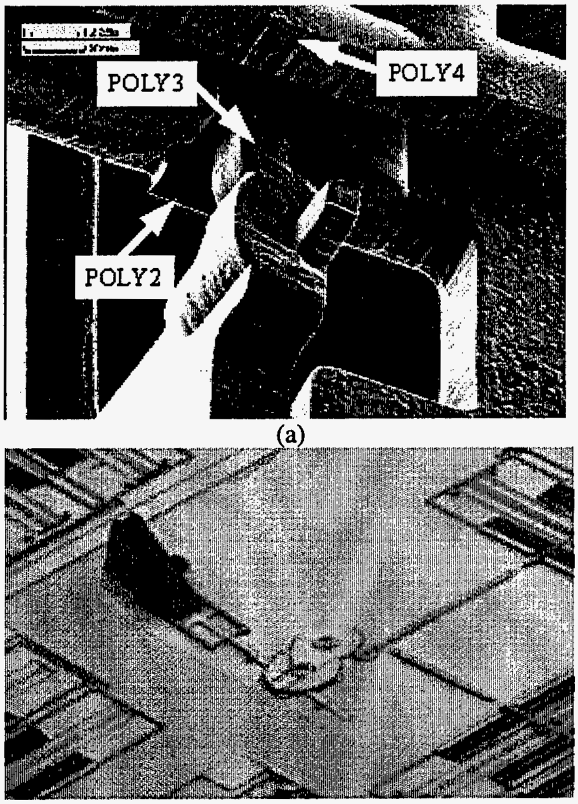
3-Dimensional Structures

These last examples make use of a common mechanical element known as a hinged joint. Pister et al [25] fabricated some of the first hinged joint structures in polysilicon surface micromachining. Since then several variations of the hinged joint have been used by numerous researchers to create 3-dimensional structures from the basically planar, 2-dimensional surface-micromachining technology by folding the 2-dimensional construction pieces into a 3-dimensional object. An example of a hinged joint and pop-up mirror with actuator, designed at Sandia, is shown in Figure 5.

In order to have structures fabricated in the fully assembled state, there must be enough 'looseness' built into the parts to allow them to be fully defined and released in the final step. The consequence of this looseness is backlash in gears and joints. For precise positioning of elements, this backlash must be taken into account.

Pister and colleagues have continued to successfully use folding hinges to produce numerous 3-dimensional objects from the thin films of surface micromachining. These structures include both mechanical structures for articulated devices and optical elements such as pop-up mirrors[26].

Also, researchers at the University of California - Los Angeles have made use of the folding hinges in the 3-layer process known as Multi-User MEMS Process (MUMPS) [11] to produce free-space micro-optical bench components on a chip[27]. As in conventional macro optical bench systems, the free-space micro-optical bench includes passive optical elements (lenses, gratings, beamsplitters, filters, and others), micropositioners (translation stages or rotation stages), and active optoelectronic components (photodetectors and laser or LED sources).



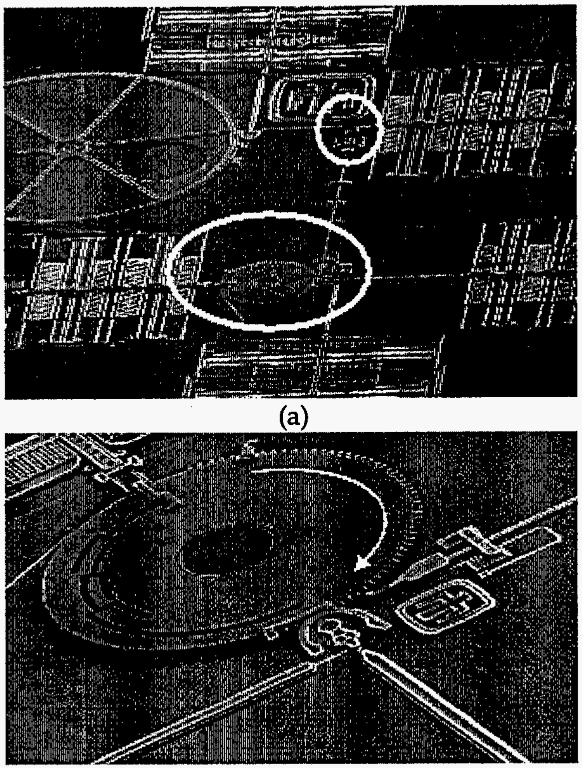
(a)

(b)

Figure 5. (a) SEM image of a hinge joint which allows two large plate areas to be folded. Note the looseness of the pin on the left plate where it goes through the retainer on the right plate. (b) Hinges allow a microengine with transimission to force a rack to fold, creating a pop-up mirror. (Sandia National Laboratory)

Sandia MOEMS

With regards to efforts at Sandia, the final example depicts the primary MOEMS being developed. This is one of our most advanced micromechanical systems to date, a complex proof-of-concept batch-fabricated assembly that, upon transmitting the proper electrical code to a mechanical lock, permits the operation of a micro-optical shutter. It is fabricated in the 4-level SUMMiT process.



(a)

(b)

Figure 6. (a) SEM image of a microlock and latch (circled elements) and an optical shutter wheel in the upper left quadrant. (b) Closer view of the pin-in-maze discriminator which deciphers the input signal to allow the unlocking of the shutter wheel.

Figure 6a is an overview SEM image which shows the lock elements (circled) and the shutter wheel in the upper left corner. The lock consists of a pin-in-maze discriminator [28] in which the pin must be actuated by the correct sequence of signals to negotiate the maze (see Figure 6b). If, and only if, this sequence is correct does the discriminator wheel rotate enough to unlatch and enable rotation of the shutter wheel to permit transmission of a laser signal through the substrate. The entire operation, from input of the lock sequence to the rotation of the shutter wheel, occurs in less than 100 milliseconds. Successful operation of this device with a Vertical Cavity Surface Emitting Laser (VCSEL) mounted to the backside of the wafer has also been demonstrated.

The primary goal of this assemblage was to demonstrate that the necessary level of complex interactions can be realized with surface micromachined technology. Although this combined set of functions does not possess the details of a fieldable mechanical lock, it successfully demonstrates that full-up devices will be possible. The next generation system consists of two sets of 24 bit locks, enabling gear units, and pop-up mirrors. The intent is to redirect an optical signal that comes up through the substrate over some distance and then back down through the substrate. This will be accomplished once the two pop-up mirrors are unlocked and enabled[29].

SUMMARY

In summary, recent advances in the basic technology of polysilicon surface-micromachining will allow researchers to continue to push forward with new and exciting designs for optical devices and systems. Incorporation of a key process technique for planarization of process-induced topography, chemical mechanical polishing, has removed several process difficulties which has enhanced the manufacturability, reliability, and robustness of polysilicon surface-micromachined systems. In turn, this has allowed additional layers of polysilicon to be added, up to a total of 5-levels. The increased design freedom is apparent with the elimination of engineering compromises as seen in the example of micromirror arrays designed and fabricated in the 4-level SUMMiT. Combinations of mechanical elements such as a lock used to disable/enable an optical shutter are also readily realized in this technology.

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ACKNOWLEDGMENT

The process development engineers, operators, and technicians of the Microelectronics Development Laboratory under the direction of J. F. Jakubczak and H. Stewart are acknowledged for their contributions to the process development and fabrication of these devices. Sandia designs are by M. S. Rodgers. M. A. Michalicek and J. H. Comtois of the USAF Phillips Laboratory provided SEM images of their micromirror devices.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

M98004024

Report Number (14) SAND--97-2641C

CONF-971192--

Publ. Date (11) 199710

Sponsor Code (18) DOE/DP, XF

UC Category (19) UC-700, DOE/ER

DOE